STiH237

HD satellite STB processor with integrated demodulator and low power standby controller

Data brief

Features

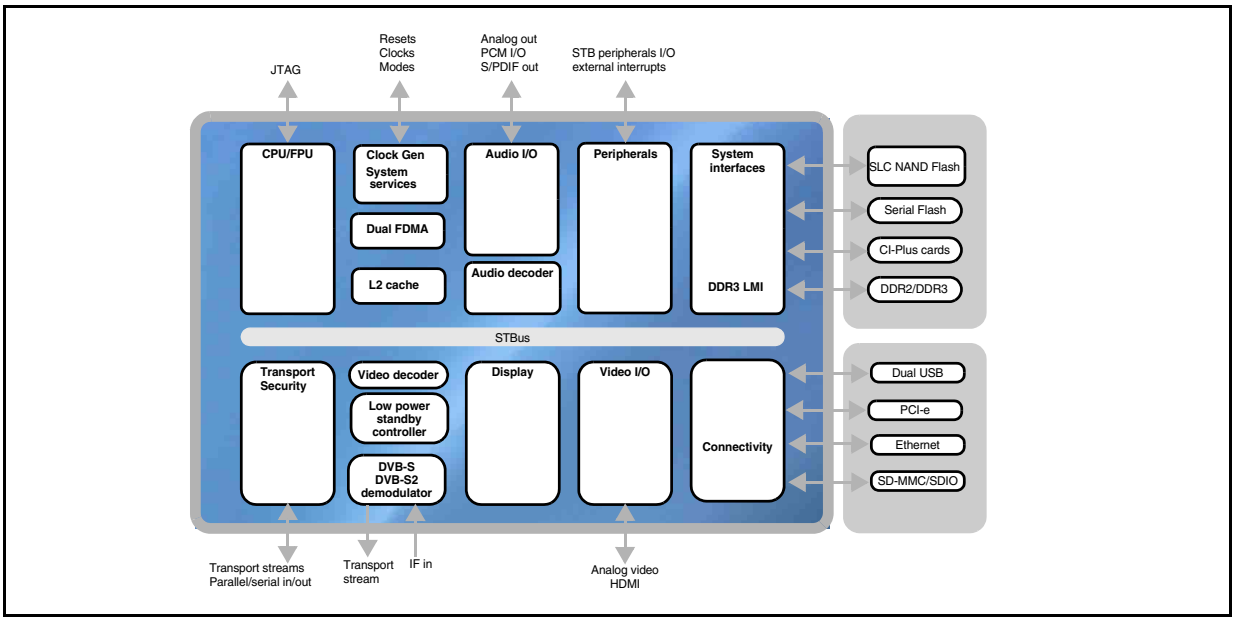
- ST40 applications CPU with 256 KB L2 cache
- 16-bit LMI supporting DDR2/DDR3
- Decoding of H264, MPEG2, VC-1 and AVS HD video streams
- 3DTV decoding and display compatible with HDMI 1.4a
- Extensive connectivity (2 × USB 2.0 ports; Ethernet MII/RMII/TMII port; SD/MMC card port; PCI-e)
- Secure boot from SLC NAND Flash or Serial NOR Flash; eMMC booting option
- Low-power process and architecture
- Integrated low power standby controller
- High-quality video resizing and de-interlacing
- Integrated Ethernet PHY
- Targets two layer PCBs for cost-effective zapper STB applications
- Integrates DVB-S/DVB-S2 single stream demodulation and FEC

Description

The STiH237 uses the latest process technology to provide a cost-effective, feature rich, highly integrated SoC for set-top boxes (STBs). It is targeted at the advanced decoding STB market across satellite networks, and is suitable for operator markets (with advanced security) and retail markets worldwide.

The STiH237 provides a solution for operators and manufacturers to specify a range of cost-effective, high performance zapper STBs, with content delivery possible using broadcast or broadband networks, or both (hybrid STBs).

The STiH237 integrates a high performance satellite receiver supporting DVB compliant reception, channel demodulation, and forward error correction (FEC). The single stream demodulator is compatible with DVB-S2 (QPSK/8PSK), DVB-S (QPSK) and legacy DirecTV^{TM} transmission standards.



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1 Introduction

The STiH237 offers current users of ST's growing family of advanced decoding ICs enhancements in performance and features, enabling operators to offer consumers new multimedia-rich services and viewing experiences, including new 3DTV features. Faster DDR3 memory is also supported, and the applications CPU benefits from an L2 cache. The STiH237 keeps pace with the latest advanced security requirements of the main CA vendors, and an integrated standby controller enables the STiH237 to target stringent low power regulations.

Features	Benefits
ST40 applications CPU, with 32KI and 32KD L1 caches and 256K L2 cache.	High performance processing for applications and middleware.
Integrated low power standby controller within its own power island.	Secure hibernation to, and fast resume from, very low power passive standby mode, targeting STB standby power < 0.5 W.
Latest generation of ST's Delta video decoder, coupled with a High Quality Video Display Pipeline (HQVDP).	Decoding of advanced high definition standards (MPEG2, H264, VC-1, AVS) plus the performance and flexibility for web-based content decoding such as Flash®, DivX™, MJPEG and Real®, without impacting applications CPU performance.
Dual USB 2.0 hosts, Ethernet MAC with MII/RMII/TMII interfaces, PCI-e, SD-MMC/SDIO interface.	Extensive high speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, Ethernet, home network controllers (such as MoCA®, Wi-Fi), DOCSIS® modem and memory cards.
NOCS1.0/1.1/1.2/3.0, NSK2.0 and DVB-CSA3 ready.	Fully compliant with the latest advanced security requirements of CA vendors.
Integrated DVB-S/DVB-S2 demodulation/FEC	Highly integrated STB solution reducing component count and manufacturing BOM.
Ball compatible with other STiH2xx family variants.	Single platform versatility across all networks (satellite, cable, terrestrial, and IP).

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
28-Feb-2012	1	Initial release.

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