NCP1032

Low Power PWM Controller with On-Chip Power Switch and Startup Circuits for Telecom Systems

The NCP1032 is a miniature high−voltage monolithic switching converter with on−chip power switch and startup circuits. It incorporates in a single IC all the active power control logic and protection circuitry required to implement, with minimal external components several switching regulator applications, such as a secondary side bias supply or a low power DC−DC converter. This converter is ideally suited for 24 V and 48 V telecom and medical isolated power supply applications. The NCP1032 can be configured in any single−ended topology such as forward or flyback converter. The NCP1032 is targeted for applications requiring up to 3 W.

The internal error amplifier allows the NCP1032 to be easily configured for secondary or primary side regulation operation in isolated and non−isolated configurations. The fixed frequency oscillator is optimized for operation up to 1 MHz and is capable of external frequency synchronization, providing additional design flexibility. In addition, the NCP1032 incorporates undervoltage and overvoltage line detectors, programmable cycle−by−cycle current limit, internal soft−start, and thermal shutdown to protect the controller under fault conditions.

Features

- On Chip High 200 V Power Switch Circuit and Startup Circuit
- Internal Startup Regulator with Auxiliary Winding Override
- Programmable Oscillator Frequency Operation up to 1 MHz
- External Frequency Synchronization Capability
- Frequency Fold−down Under Fault Conditions
- Trimmed ± 2% Internal Reference
- Programmable Cycle−by−Cycle Current Limit
- Internal Soft−Start
- Active Leading Edge Blanking Circuit
- Line Under and Over Voltage Protection
- Over Temperature Protection
- These are Pb−Free Devices

Typical Applications

- POE (Power Over Ethernet)/PD. Refer to Application Note AND8247
- Secondary Side Bias Supply for Isolated DC−DC Converters
- Stand Alone Low Power DC−DC Converter
- Low Power Bias Supply
- Low Power Boost Converter
- Medical Isolated Power Supplies
- Bias Supply for Telecom Systems. Refer to App Note AND8119/D

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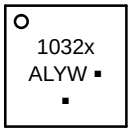
MARKING DIAGRAMS

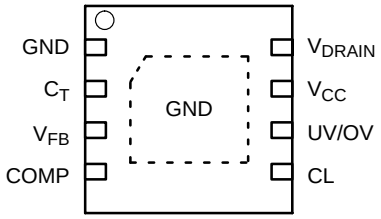
WDFN8
MN SUFFIX
CASE 511BH



1032 = Specific Device Marking
x = A or B
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



WDFN8 (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

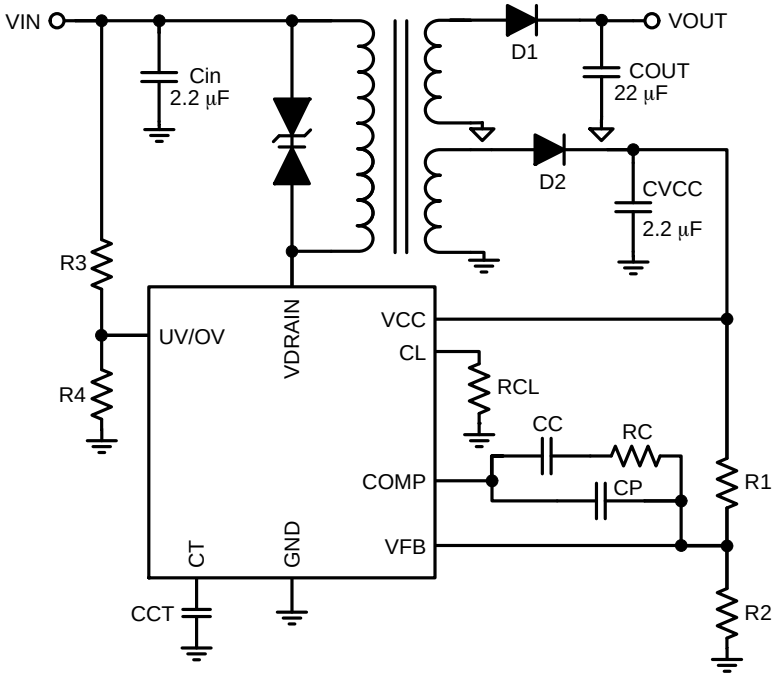


Figure 1. Typical Application – Dual Output Auxiliary Regulated Isolated Flyback

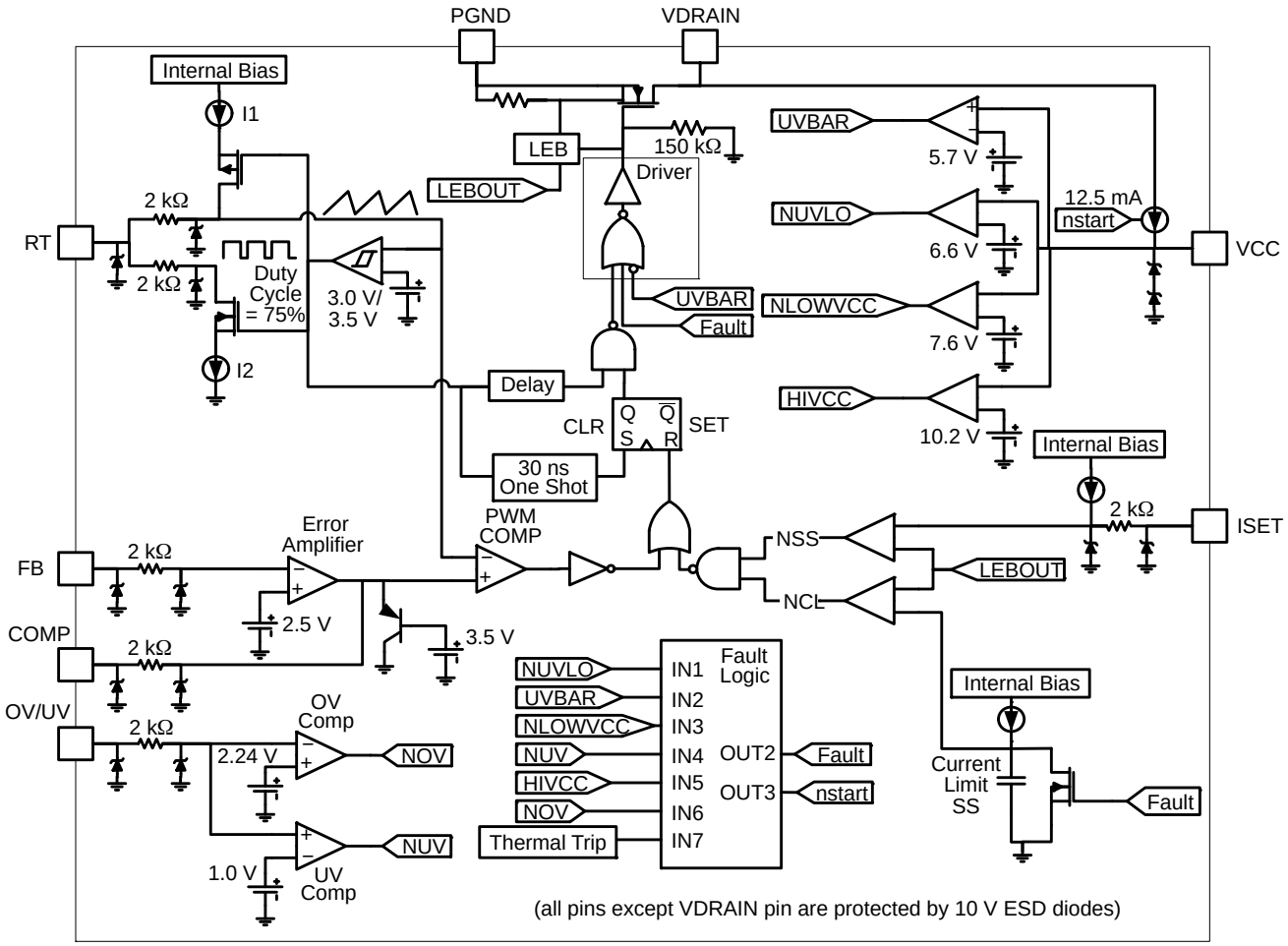


Figure 2. NCP1032 Simplified Block Diagram

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Name	Function	Description
1	GND	IC Ground	Ground reference pin for the circuit.
2	C_T	Oscillator Frequency Selection	An external capacitor connected to this pin sets the oscillator frequency up to 1 MHz. The oscillator can be synchronized to a higher frequency by charging or discharging CT to trip the internal 3.0 V/3.5 V comparators. If a fault condition exists, the power switch is disabled and the frequency is reduced.
3	V_{FB}	Feedback Signal Input	The regulated voltage is scaled down to 2.5 V by means of a resistor divider. Regulation is achieved by comparing the scaled voltage to an internal 2.5 V reference.
4	COMP	Error Amplifier Compensation	The output of the internal error amplifier. External compensation network between COMP and VFB pin is required for stable operation.
5	CL	Current Limit Threshold Selection	A resistor R_{CL} connected between this pin and ground sets the peak current value of the current limit. If the CL pin is left open, the current limit value is set to its initial maximum value of approximately 12 mA (C_{LIM_MAX}). Programmable current limit threshold, together with internal soft−start feature effectively limits the primary transformer high current peaks during startup phase.
6	UV/OV	Input Line Undervoltage and Overvoltage Shutdown	Input line voltage is scaled down using an external resistor divider. The minimum operating Vin voltage is achieved when the voltage on UV/OV pin reaches UV threshold 1.0 V. The maximum operating voltage is then limited by 2.4 V on UV/OV pin. A device version without OV protection feature is available, see ordering information section.
7	V_{CC}	Powers the Internal Circuitry	Supplies power to the internal control circuitry. Connect an external capacitor for energy storage during startup. The Vcc voltage should not exceed 16 V during operation.
8	V_{DRAIN}	Drain Connection	Connects the power switch and startup circuit to the primary transformer windings.
EP	EP	Thermal Flag	This is the thermal flag for the IC and should be soldered to the ground plane.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch and Startup Circuits Voltage	BVdss	−0.3 to +200	V
VCC Power Supply Voltage	V_{CC}	−0.3 to +16	V
Power Supply Voltage on all Pins, except VDRAIN and VCC	V_{IO}	−0.3 to +10	V
Drain Current Peak During Transformer Saturation	$I_{DS(pk)}$	1.0	A
Thermal Resistance Junction−to−Air –W DFN8 3x3, case 511BH (100 sq mm, 2oz) (Note 4) (500 sq mm, 2oz) (Note 4) (100 sq mm,2oz,) (Note 5)	$R_{\theta JA}$	 109 64 44	°C/W
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature Range	T_{STG}	−60 to +150	°C
ESD Capability, Human Body Model Pins 1−7 (Note 1)		4.0	kV
ESD Capability, Machine Model Pins 1−7 (Note 1)		400	V
Pin 8 is connected to the high voltage startup and power switch which is protected to the maximum drain voltage		200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ± 200 V per JEDEC standard: JESD22−A115.
2. This device contains latch−up protection and it exceeds ± 100 mA per JEDEC standard: JESD78 class II
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A
4. EIA JEDEC 51.3, single layer PCB with added heat spreader
5. EIA JEDEC 51.7, four layer PCB with added heat spreader

Table 3. ELECTRICAL CHARACTERISTICS
(For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, V_{DRAIN} = 48 V, V_{CC} = 12 V, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY SECTION AND VCC MANAGEMENT						
V_{CC_ON}	Vcc Voltage at Which the Switcher Starts Operation	V_{CC} Increasing	9.9	10.2	10.5	V
V_{CC_MIN}	Minimum Operating VCC After Turn on at Which HV Current Source Restarts	V_{CC} Decreasing	7.40	7.55	7.7	V
V_{CC_RST}	Vcc Undervoltage Lockout Voltage	V_{CC} Decreasing, $V_{FB} = V_{COMP}$	6.75	6.95	7.15	V
I_{CC1}	Internal IC Consumption Power Switch Enabled	MOSFET is switching at 300 kHz	2.0	2.9	4.0	mA
I_{CC2}	Internal IC Consumption Power Switch Disabled	No Fault condition, V_{FB} = 2.7 V	−	2.0	2.5	mA
I_{CC3}	Internal IC Consumption Power Switch Disabled	Fault condition, V_{FB} = 2.7 V, $V_{UV/OV}$ < 1.0 V	−	0.75	1.5	mA
POWER SWITCH CIRCUIT						
R_{DSON}	Power Switch Circuit On−State Resistance	I_D = 100 mA T_J = 25°C T_J = 125°C	 − −	 4.2 4.9	 5.1 8.0	Ω
BVdss	Power Switch Circuit and Startup Breakdown Voltage	I_{DS_OFF} = 100 μA, V_{UV_OV} < 1.0 V Tj = 25°C	200	−	−	V
I_{DS_OFF}	Power Switch Circuit and Startup Circuit Off−State Leakage Current	V_{DRAIN} = 200 V, V_{UV_OV} < 1.0 V T_J = 25°C T_J = −40°C to 125°C	 − −	 20 20	 25 30	μA
t_R	Switching Characteristics − Rise Time	V_{DS} = 48 V, R_L = 480 Ω, Time (10%−90%)	−	7	−	ns
t_f	Switching Characteristics − Fall Time	V_{DS} = 48 V, R_L = 480 Ω, Time (90%−10%)	−	10	−	ns
INTERNAL STARTUP CURRENT SOURCE						
I_{START1}	HV Current Source	Vcc = 0 V, Tj = 25°C Tj = −40°C to 125°C	 10.0 9.0	 12.0 −	 14.0 15.0	mA
I_{START2}	HV Current Source	Vcc = V_{CC_ON} − 0.2 V Tj = 25°C Tj = −40°C to 125°C	 9.0 8.0	 11.0 −	 13.0 16.0	mA
V_{start_min}	Minimum Startup Voltage	I_{START2} = 0.5 mA, Vcc = V_{CC_ON} − 0.2 V, Tj = 25°C	−	16.3	−	V
ERROR AMPLIFIER						
V_{REF}	Reference Voltage	$V_{COMP} = V_{FB}$, Follower Mode T_J = 25°C T_J = −40°C to 125°C	 2.45 2.40	 2.5 2.5	 2.55 2.60	V
REG_{LINE}	Line Regulation	V_{CC} = 8 V to 16 V, T_J = 25°C	−	1.0	3.0	mV
I_{VFB}	Input Bias Current	V_{FB} = 2.3 V	−	70	150	nA
I_{SRC}	COMP Source Current	V_{FB} = 2.3 V	80	95	125	μA
I_{SNK}	COMP Sink Current	V_{FB} = 2.7 V	500	700	900	μA
V_{C_MAX}	COMP Maximum Voltage	I_{SRC} = 0 μA, V_{FB} = 2.3 V	3.95	4.17	4.5	V
V_{C_MIN}	COMP Minimum Voltage	I_{SNK} = 0 μA, V_{FB} = 2.7 V	−	91	200	mV
A_{VOL}	Open Loop Voltage Gain	(Note 6)	−	80	−	dB
GBW	Gain Bandwidth Product	(Note 6)	−	1.0	−	MHz

Table 3. ELECTRICAL CHARACTERISTICS
(For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, V_{DRAIN} = 48 V, V_{CC} = 12 V, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CURRENT LIMIT AND PWM COMPARATOR						
C_{LIM_MAX}	Max Current Limit Threshold	CL pin Floating, T_J = 25°C, (di/dt = 0.5 A/μs)	420	512	600	mA
C_{LIM_MIN}	Min Current Limit Threshold	R_{CL} = 20 kΩ, T_J = 25°C, (di/dt = 0.1 A/μs)	−	57	−	mA
T_{PLH}	Propagation Delay	from Current Limit Detection to the Drain OFF State (Note 6)	−	100	−	ns
T_{ON_MIN}	Min On Time Pulse Width	FSW = 300 kHz (Note 6)	−	240	−	ns
T_{ss}	Soft−Start Duration	(Note 6)	−	2.0	−	ms
LINE UNDER/OVERVOLTAGE PROTECTIONS						
V_{uv}	Undervoltage Lockout Threshold	V_{FB} = $V_{COMP,}$ Vin decreasing	0.95	1.067	1.18	V
V_{UV_hys}	Undervoltage Lockout Hysteresis		−	70	−	mV
Iuv	Input Bias Current	V_{FB} = 2.3 V	−	0	1	μA
V_{OV}	Overvoltage Lockout Threshold	V_{FB} = $V_{COMP,}$ Vin increasing (Note 7)	2.3	2.41	2.5	V
V_{ov_hys}	Overvoltage Lockout Hysteresis		−	158	−	mV
TEMPERATURE MANAGEMENT						
TSD	Thermal Shutdown	(Note 6)		175		°C
	Hysteresis in Shutdown	(Note 6)		20		°C
INTERNAL OSCILLATOR						
f_{OSC1}	Oscillation Frequency, 300 kHz	C_T = 560 pF (Note 9) T_J = 25°C T_J = −40°C to 125°C	 275 270	 300 −	 325 335	kHz
f_{OSC2}	Oscillation Frequency, 960 kHz	C_T = 100 pF, T_J = 25°C	−	960	−	kHz
I_{CT_C}	Timing Charge Current	V_{CT} = 3.25 V	−	172	−	μA
I_{CT_D}	Timing Discharge Current	V_{CT} = 3.25 V		517		μA
V_{R_pk}	Oscillator Ramp Peak Voltage		−	3.492	−	V
V_{R_VLY}	Oscillator Ramp Valley		−	2.992	−	V
DC_{MAx}	Maximum Duty Cycle		70	76.5	80	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by design and characterized
7. The OV/UV option is disabled on the NCP1032B version
8. Oscillator frequency can be externally synchronized to the maximum frequency of the device

TYPICAL OPERATING CHARACTERISTICS – Dual Output Isolated Flyback Converter

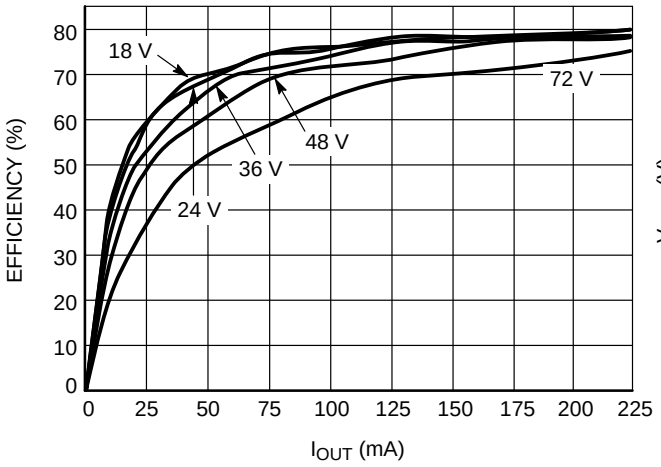


Figure 3. Efficiency vs. I_{OUT} at V_{IN} = 24, 36, 48 and 72 V, T1 = CoilCraft B0226−EL

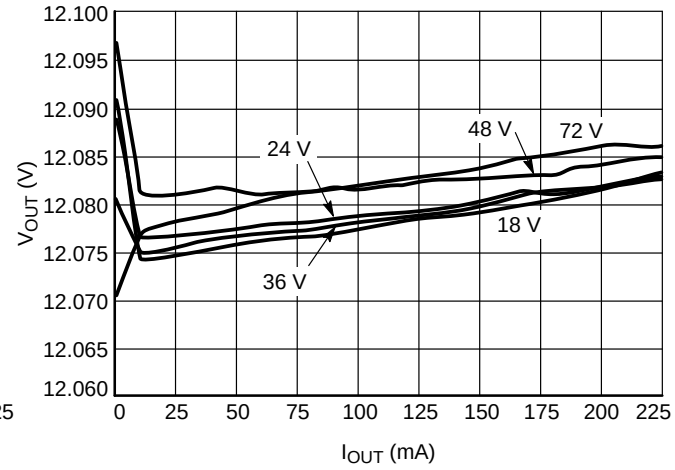


Figure 4. V_{CC} Pin Load Regulation at V_{IN} = 24, 36, 48 and 72 V

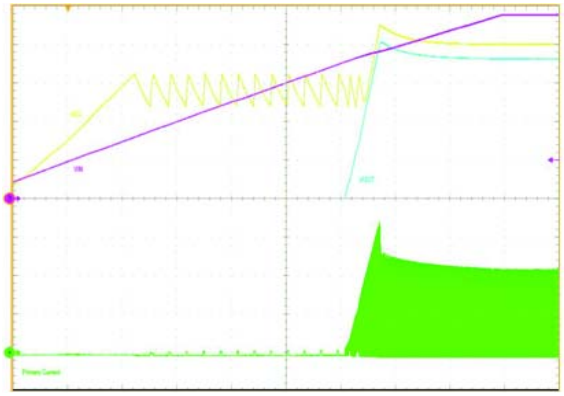


Figure 5. Startup Sequence, R_{CL} Open, Output Load = 80 Ω (I_{OUT} = 150 mA), 1 V_{CC} 3.0 V/ div DC, 2 V_{OUT} 3.0 V/div DC, 3 V_{IN} 10.0 V/ div DC, 4 I_{PRI} 100 mA/div DC, T = 20 ms/div

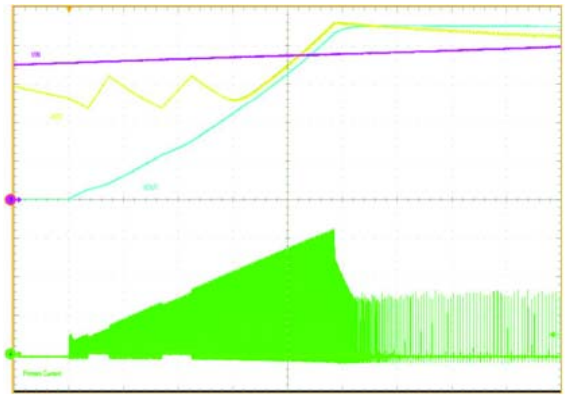


Figure 6. Soft−Start, R_{CL} open, Output No Load 1 V_{CC} 3.0 V/div DC, 2 V_{OUT} 3.0 V/div DC, 3 VIN 10.0 V/div DC, 4 I_{PRI} 100 mA/div DC, T = 500 μs/div

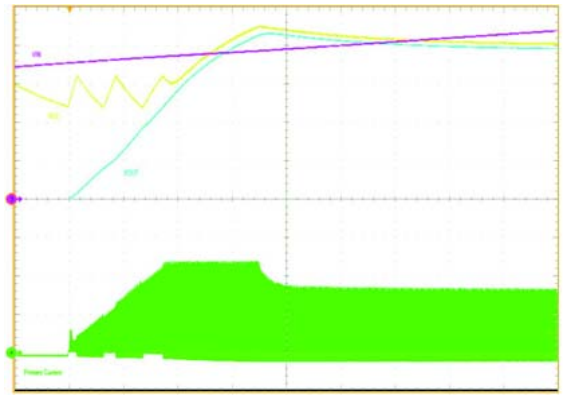


Figure 7. Soft−Start, R_{CL} = 32 kΩ (C_{LIM} = 250 mA), Output Load = 240 Ω (I_{OUT} = 50 mA), 1 V_{CC} 3.0 V/div DC, 2 V_{OUT} 3.0 V/div DC, 3 V_{IN} 10.0 V/div DC, 4 I_{PRI} 100 mA/div DC, T = 1.0 ms/div

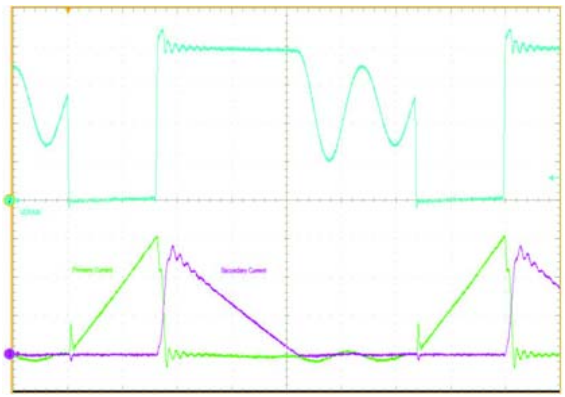


Figure 8. Discontinuous Conduction Mode (DCM), I_{OUT} = 150 mA, 2 V_{DRAIN} 20 V/div DC, 3 I_{SEC} 30 mA/div DC, 4 I_{PRI} 100 mA/div, DC, T = 500 ns/div

TYPICAL OPERATING CHARACTERISTICS

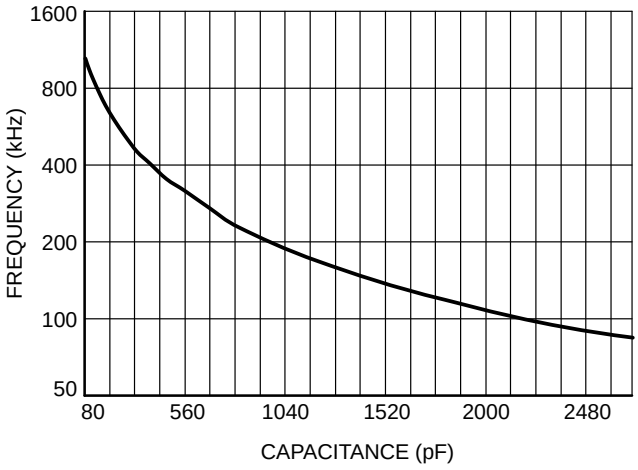


Figure 9. Frequency vs. Timing Capacitor C_T at 25°C

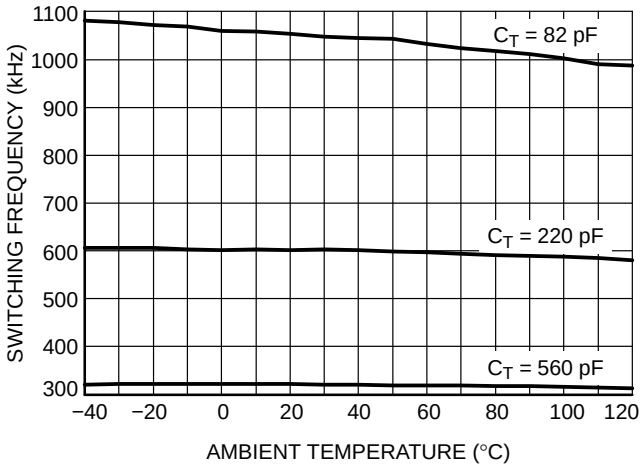


Figure 10. Oscillator Frequency vs. Junction Temperature

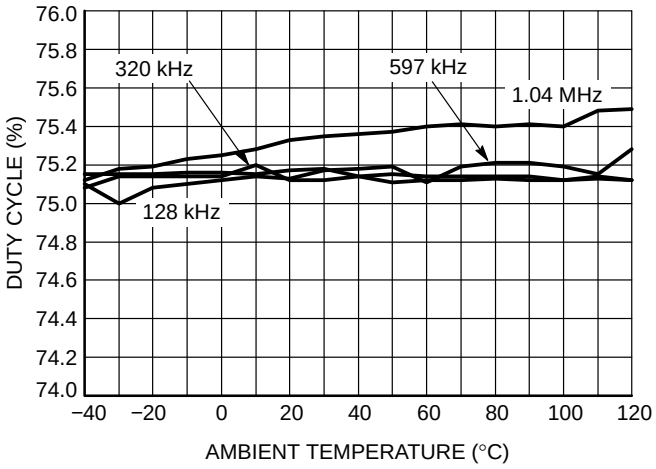


Figure 11. Maximum Duty Ratio vs. Temperature

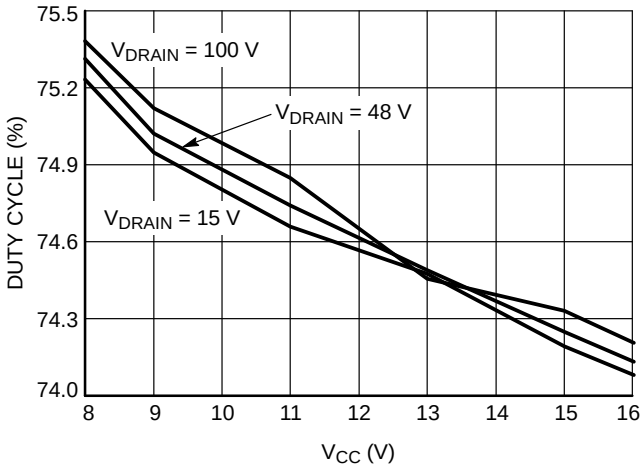


Figure 12. Maximum Duty Ratio vs. VCC Voltage

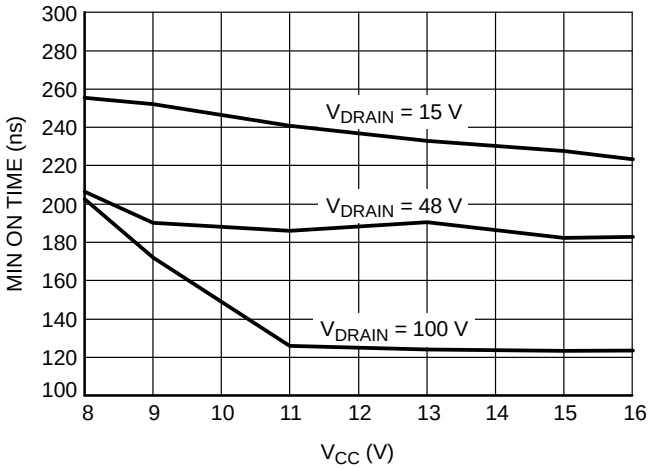


Figure 13. Minimum On Time vs. VCC

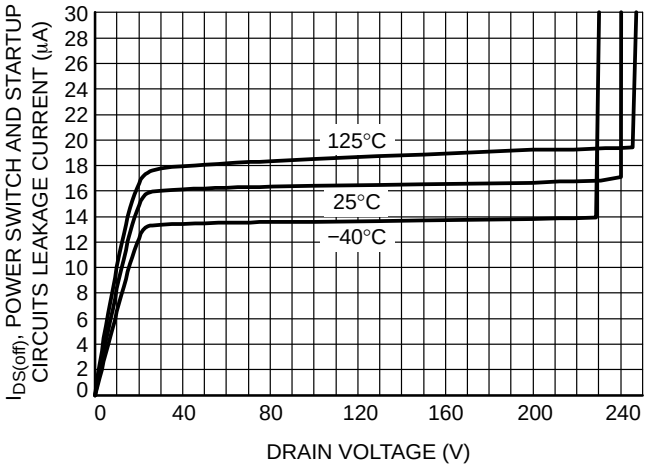


Figure 14. Power Switch Circuit and Startup Circuit Leakage Current vs. Drain Voltage

TYPICAL OPERATING CHARACTERISTICS

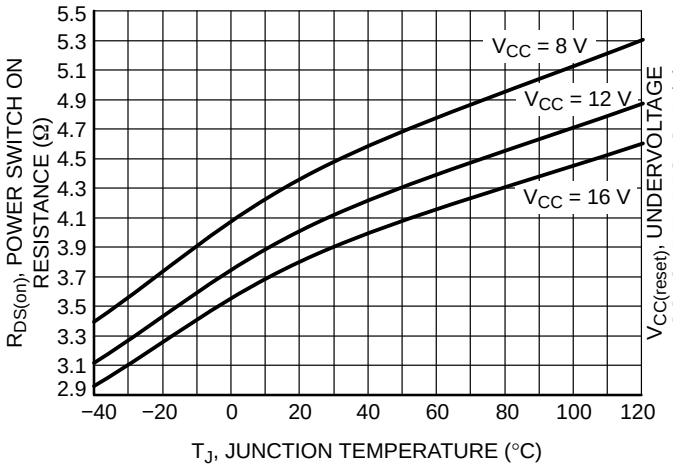


Figure 15. Power Switch R_{DSON} vs. Junction Temperature

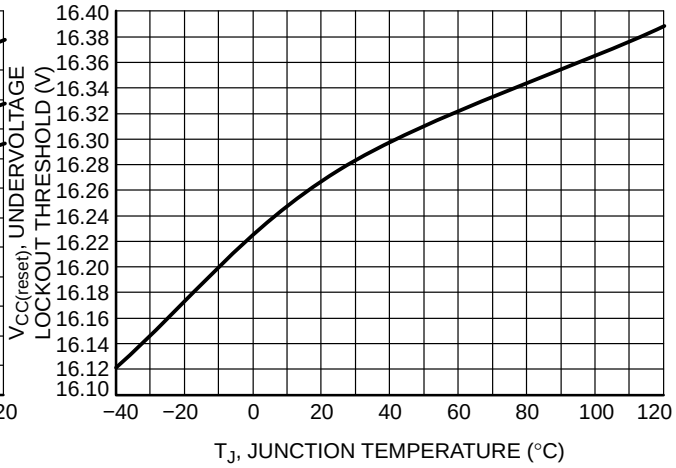


Figure 16. Vdrain Startup Threshold over Temperature

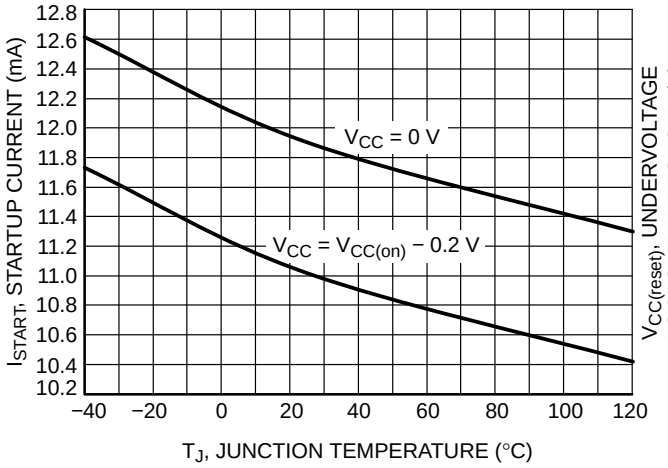


Figure 17. Startup Current vs. Junction Temperature

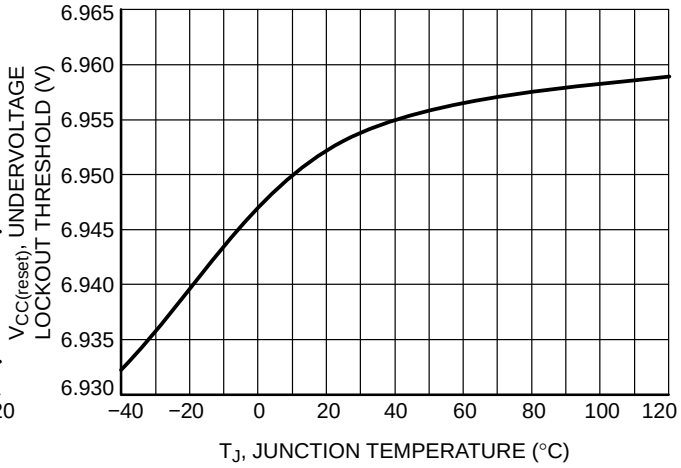


Figure 18. Undervoltage Lockout Threshold vs. Junction Temperature

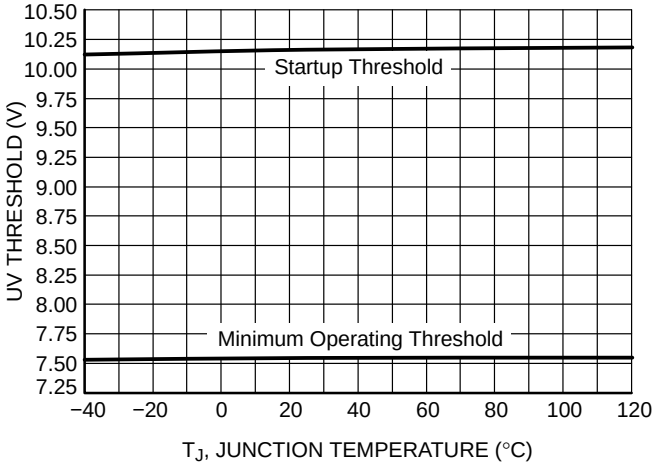


Figure 19. Supply Voltage Thresholds vs. Junction Temperature

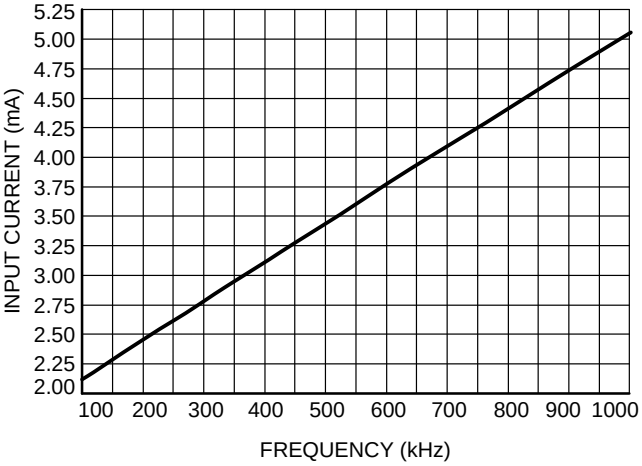


Figure 20. VCC Input Current at 12 V with an 18 V applied Drain voltage 25°C VS Oscillator Frequency

TYPICAL OPERATING CHARACTERISTICS

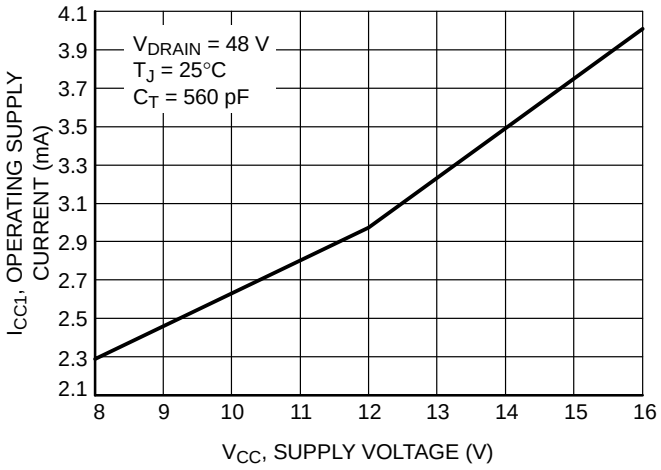


Figure 21. Operating Supply Current vs. Supply Voltage at 320 kHz

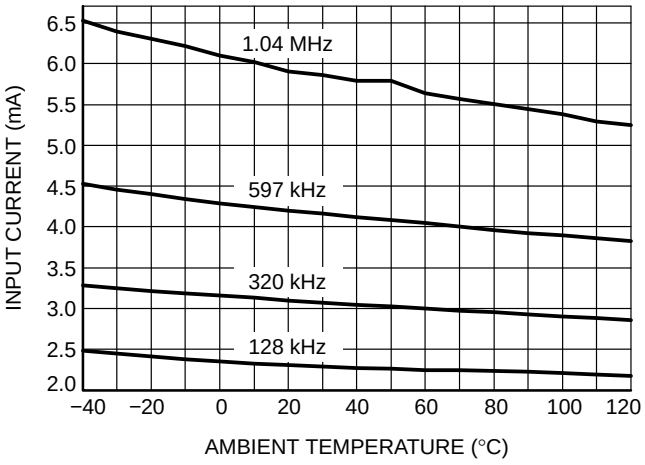


Figure 22. VCC Input Current vs. Temperature over Frequency span VDrain = 48 V

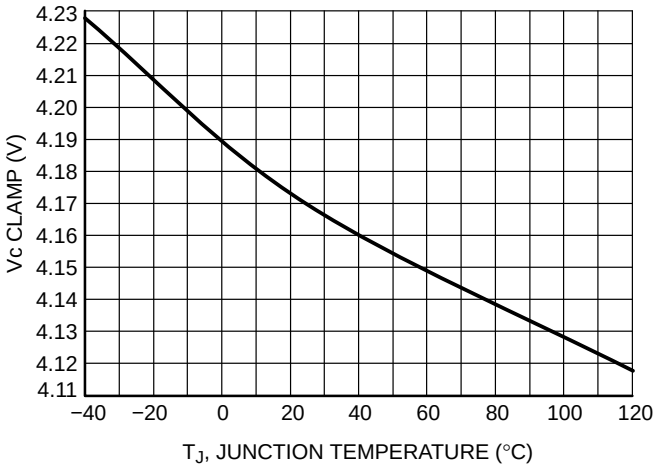


Figure 23. COMP Clamp Voltage vs. Junction Temperature

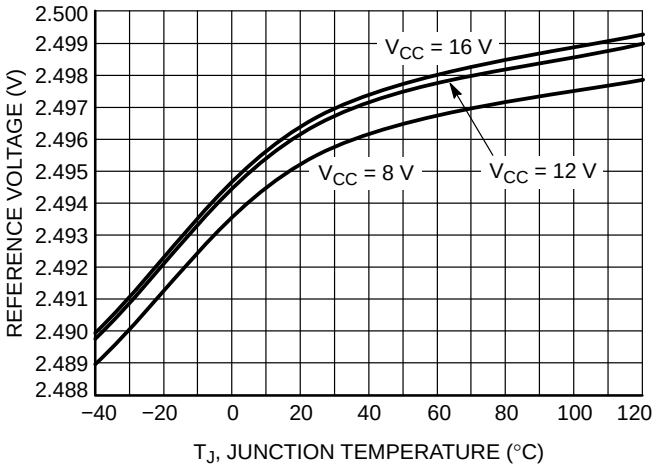


Figure 24. Reference Voltage vs. Junction Temperature

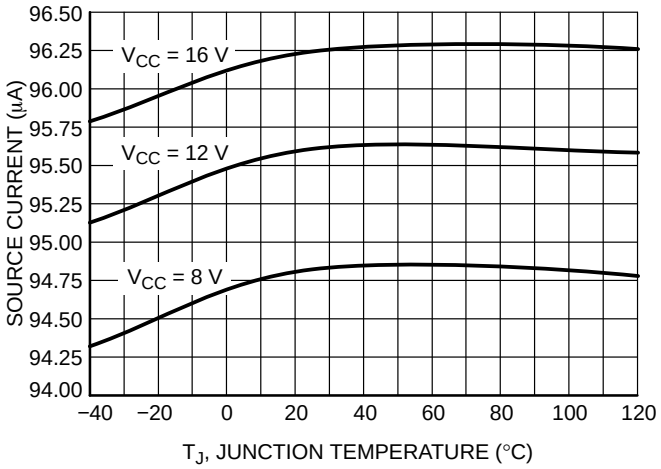


Figure 25. COMP Source Current vs. Junction Temperature

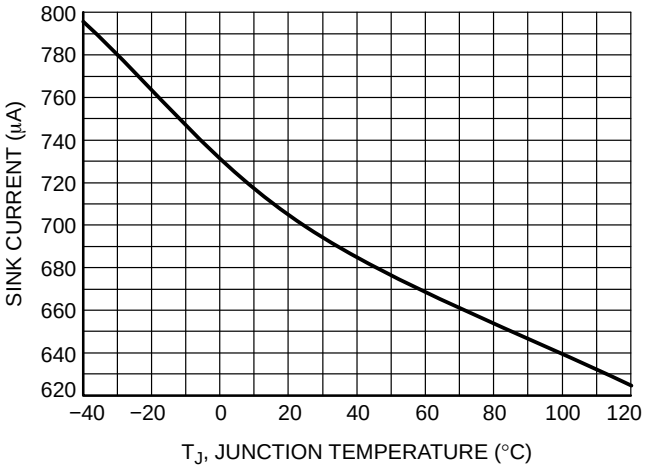


Figure 26. COMP Sink Current vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS

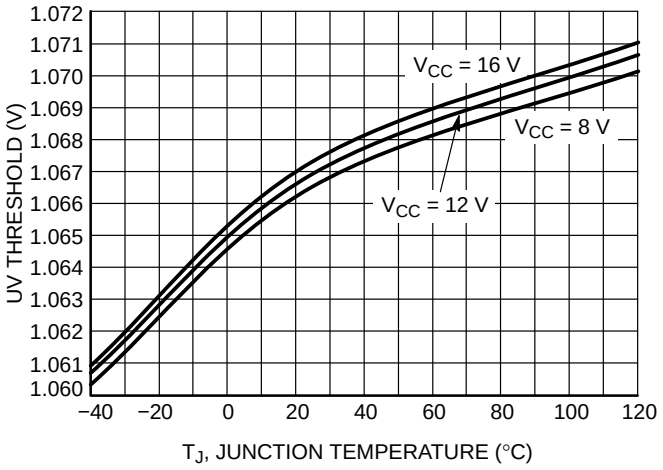


Figure 27. Undervoltage Threshold vs. Junction Temperature

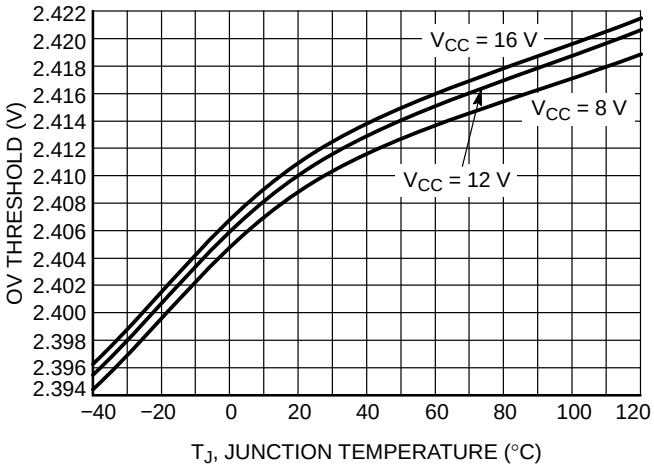


Figure 28. Overvoltage Threshold vs. Junction Temperature

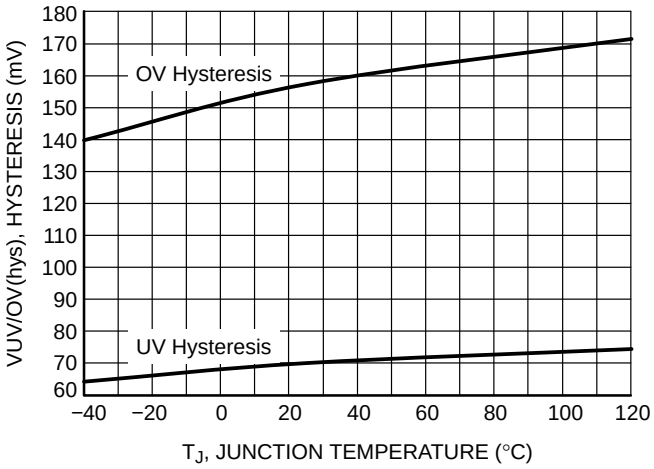


Figure 29. Under/Overvoltage Hysteresis vs. Junction Temperature

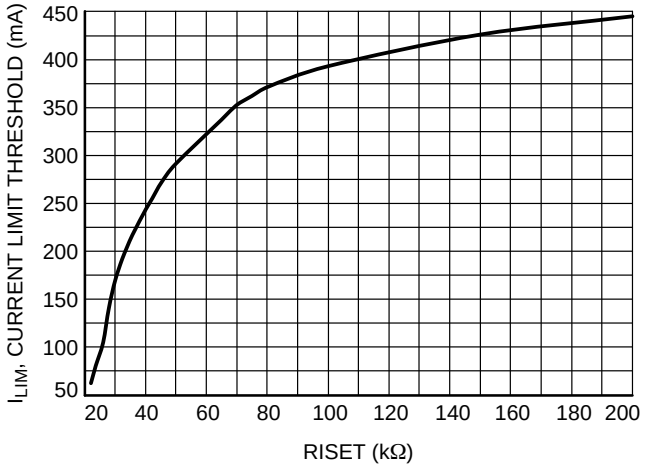


Figure 30. Current Limit Threshold vs. R_{CL}, Current Slew Rate = 0.5 A/μs

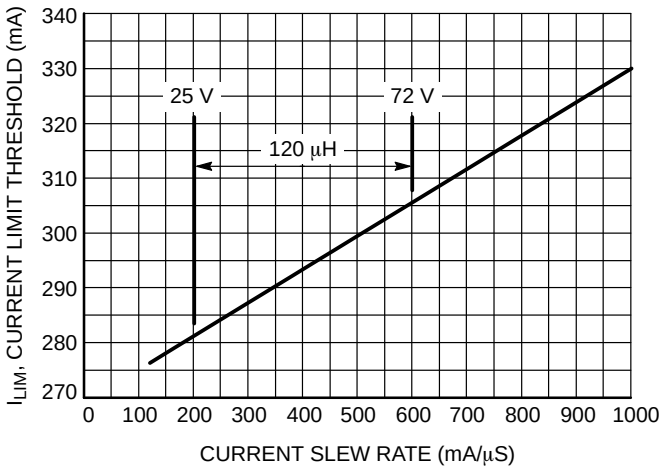


Figure 31. Current Limit Threshold vs. Current Slew Rate

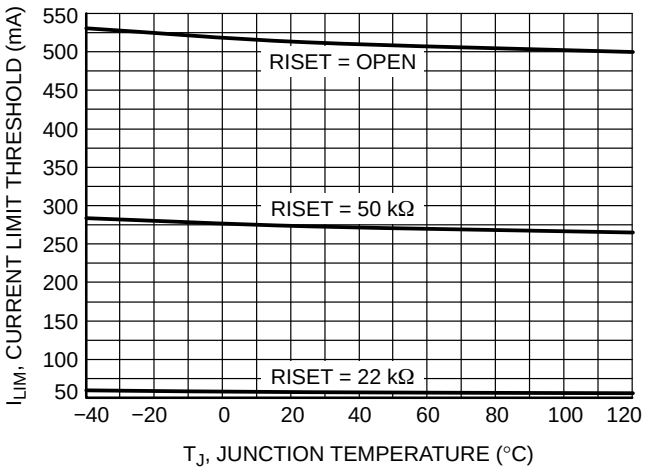


Figure 32. Current Limit Threshold vs. T_J, Current Slew RISET = Open = 0.5 A/μs, RISET = 55 kΩ = 0.3 A/μs, RISET = 22 kΩ = 0.1 A/μs

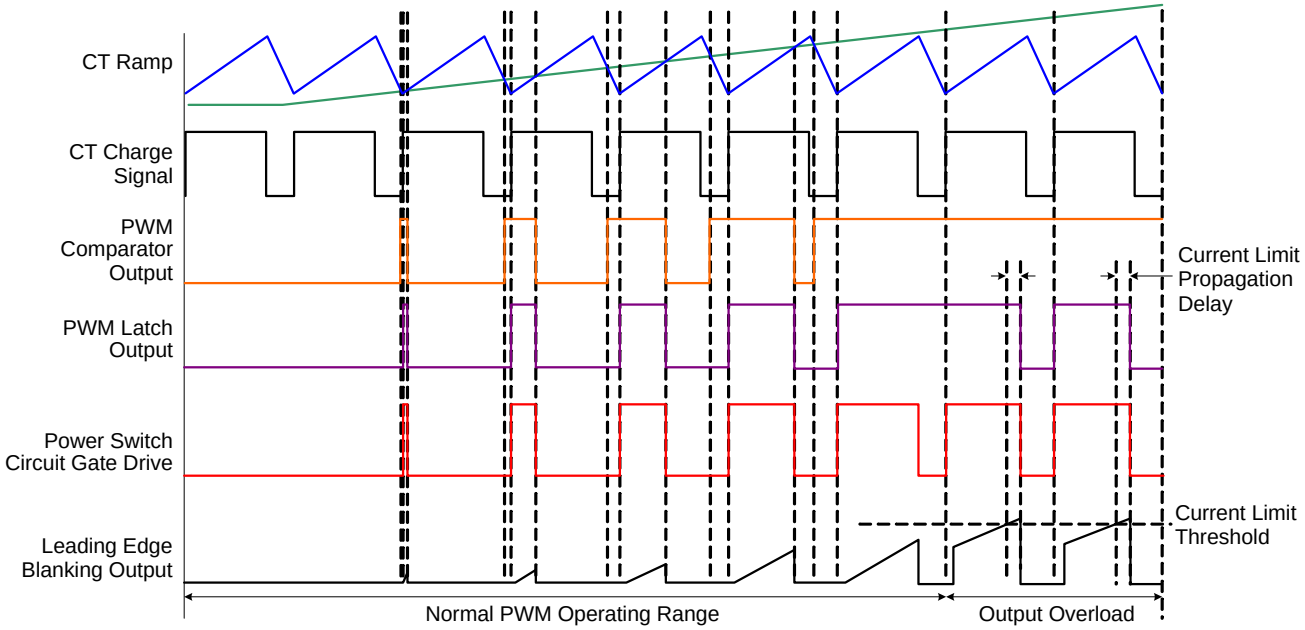


Figure 33. Pulse Width Modulation Timing Diagram

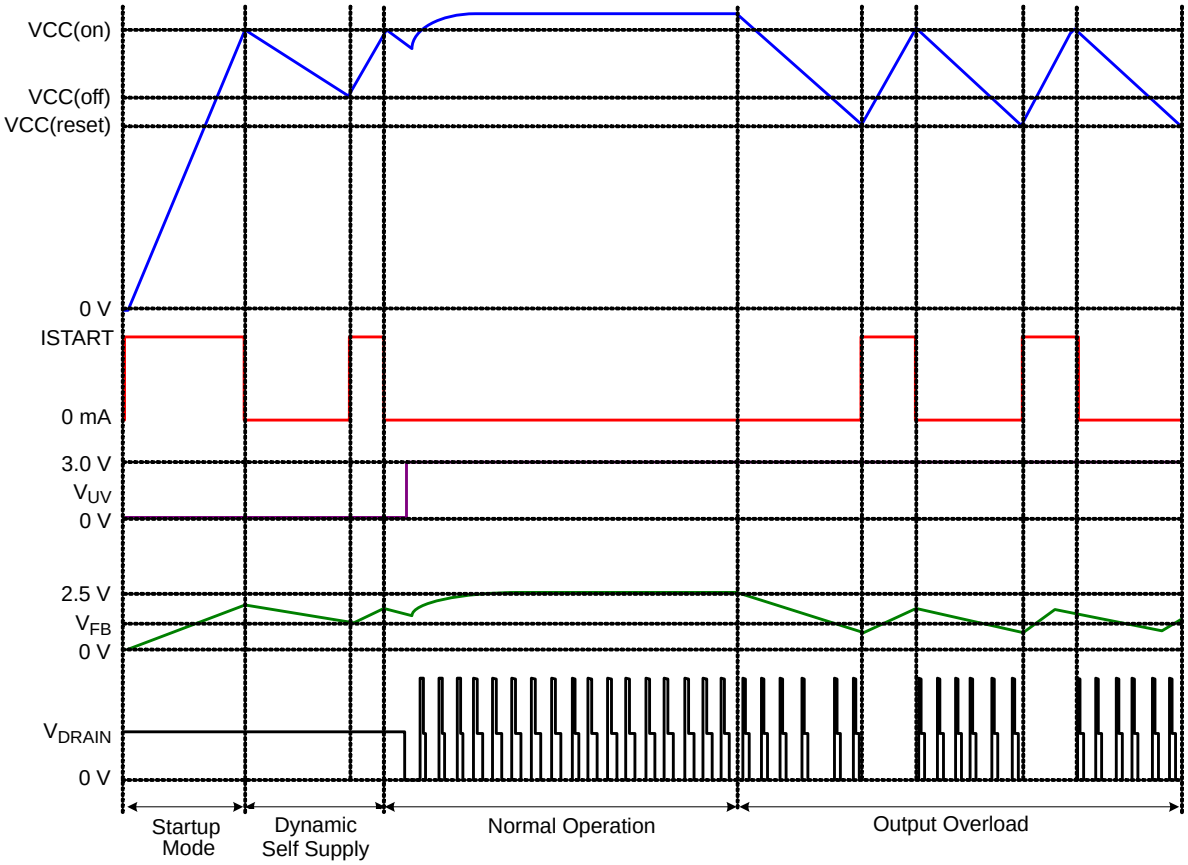


Figure 34. Auxiliary Winding Operation with Output Overload Timing Diagram

Introduction

The NCP1032 is a monolithic voltage−mode switching regulator designed for isolated and non−isolated bias supply applications. The internal startup circuit and the MOSFET are rated at 200 V, making them ideal for 24 V through 48 V telecom and 42 V automotive applications. In addition, the NCP1032 can operate from an existing 12 V supply. The regulator is optimized for operation up to 1 MHz.

The NCP1032 device incorporates all of the active power, control logic, protection circuitry, and power switch in a single IC. The compact design allows the designer to use minimal external components on several switching regulator applications, such as a secondary side bias supply or a low power DC−DC converter.

The NCP1032 is available in the space saving WDFN8 3 x 3 mm package and is targeted for applications requiring up to 3 W.

The NCP1032 has an extensive set of features including programmable cycle−by−cycle current limit, internal soft−start, input line under and over voltage detection comparators with hysteresis, regulator output undervoltage lockout with hysteresis and over temperature protection providing protection during fault conditions. A description of each of the functional blocks is given below and the functional block diagram is shown in Figure 2.

Startup Supply Circuit and Undervoltage Lockout

The NCP1032 contains an internal 200 V startup regulator that eliminates the need for external startup components. The startup regulator consists of a 12 mA (typical) current source that supplies power from the input line (VDRAIN) pin to charge the capacitor on the V_{CC} pin (C_{VCC}). The act of charging the C_{VCC} capacitor until it reaches 10.2 V while holding the power switch off is called Startup Mode (SM). Once the current source charges the V_{CC} voltage to 10.2 V (typical) the startup circuit is disabled and if no faults are present, the power switch circuit is enabled. The internal control circuitry will draw its current from the energy held by the C_{VCC} capacitor. The startup regulator turns on again once V_{CC} reaches 7.55 V. The charging of the C_{VCC} capacitor to 10.2 V by the current source and the discharging by the control circuitry to 7.55 V will be henceforth referred to as Dynamic Self Supply (DSS).

If V_{CC} falls below 7.55 V while switching, the device enters a Restart Mode (RM). While in the RM the C_{VCC} capacitor is allowed to discharge to 6.95 V while the power switch is enabled. Once the 6.95 V threshold is reached, the power switch circuit is disabled, and the startup regulator is enabled to charge the C_{VCC} capacitor. The power switch is enabled again once the V_{CC} voltage reaches 10.2 V. Therefore, the external C_{VCC} capacitor must be sized such that a voltage greater than 6.95 V is maintained on the V_{CC} pin while the converter output reaches regulation. The output is delayed 0.4 ms (T_{SS_Delay}) from the released undervoltage lockout to the first switching pulse. The soft−start time T_{SS} is fixed at 2 ms to ramp the current from its minimum value to its maximum value. The soft−start time is load and RCL dependent and can be computed in the soft−start section. The designer must evaluate the current draw of the regulator at the desired switching frequency over the V_{CC} and temperature operating range shown in Figures 20 − 22. C_{VCC} is calculated using the following equation:

$$C_{VCC} = \frac{I_{CC} \times \left(T_{SS\_Delay} + T_{SS}\right)}{V_{CC\_ON} - V_{CC\_MIN}} \rightarrow \quad \text{(eq. 1)}$$

$$2.95\ \mu F = \frac{4.0\ mA \times \left(0.4\ ms + 2.0\ ms\right)}{10.2\ V - 6.95\ V}$$

I_{CC} includes the NCP1032 bias current (I_{CC1_MAX}) and any additional current used to bias the feedback (if used). Assuming an I_{CC1_MAX} of 3.5 mA plus a 0.5 mA bias current for the feedback sensing resistors (if used), and Tss of 2 ms, C_{VCC} is calculated at 2.95 μF and should be rounded up to ensure design margin to 3.3 μF. Please note that if the feedback sensing resistors are connected to the V_{CC} pin (isolated main output topology) and C_{VCC} is increased to match C_{OUT}, the transient response of the converter will suffer. The poor transient response is due to the imbalanced capacitance to current ratio. The auxiliary winding has a significantly greater capacitance to current ratio than the output winding, taking it longer for C_{VCC} to follow C_{OUT} during a transient condition.

After initial startup, the V_{CC} pin should be biased above V_{CC_min} using an auxiliary winding. This will prevent the startup regulator from turning on during normal operation, reducing device power dissipation. A load should not be directly connected to the V_{CC} pin. A load greater than 12 mA will override the startup circuit possibly damaging the part. The maximum voltage rating of the startup circuit is 200 V. Power dissipation should be observed to avoid exceeding the maximum power dissipation of the package. Figure 35 shows the recommended configuration for a non−isolated flyback converter.

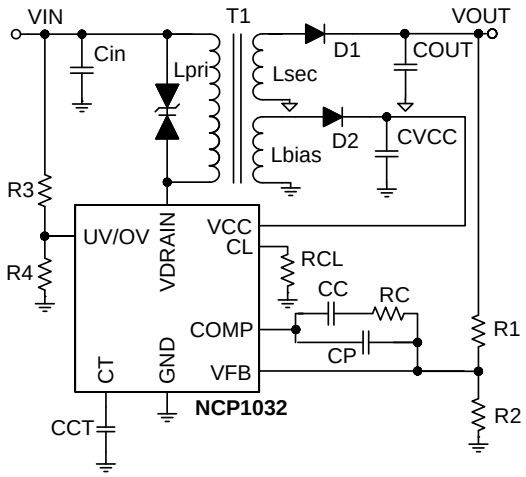


Figure 35. Non−Isolated Bias Supply Configuration

Soft−Start

The NCP1032 features an internal soft−start which reduces power−on stress and also contributes to the lower output overshoot. Once the V_{CC_ON} threshold is reached and there are no fault conditions, the power switch is enabled and the cycle−by−cycle current limit is ramped up slowly to the current limit threshold set by the CL pin. If the CL pin is open, the current limit will be set to its maximum value and the soft−start time will be 2 ms as shown in Figure 36. The equation below can be used to calculate the soft−start time for all other current limit set values.

$$TSSR = \frac{Set_{Current} - Min_{Current}}{Max_{Current} - Min_{Current}} \times T_{SS} \rightarrow \quad \text{(eq. 2)}$$

$$1.07\ ms = \frac{300\ mA - 57\ mA}{512\ mA - 57\ mA} \times 2\ ms$$

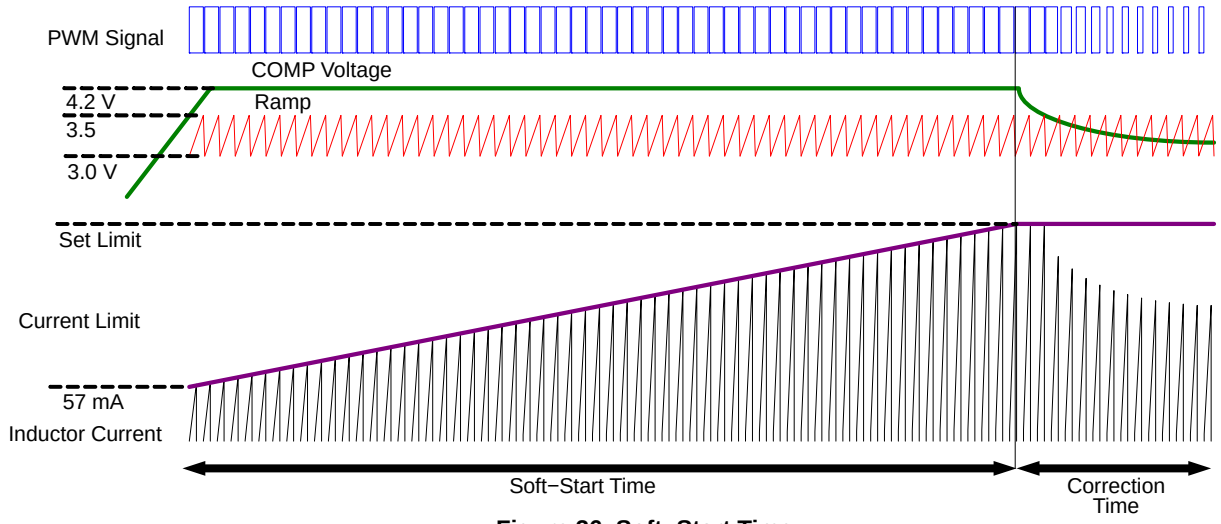


Figure 36. Soft−Start Time

The compensation of the converter must be manipulated to minimize the overshoot of the output voltage during startup, details are in the compensation section.

Line Under and Over Voltage Detectors

The NCP1032 incorporates Vin input line under voltage (UV) and over voltage (OV) shutdown circuits. If the UV/OV pin is set below 1.0 V or above 2.4 V thresholds the power switch will stop switching and the part will use DSS until the problem is corrected. The comparators incorporate typical voltage hysteresis of 70 mV (UV) and 158 mV (OV) to prevent noise from inadvertently triggering the shutdown circuit. The UV/OV sense pin can be biased using an external resistor divider from the input line as shown in Figure 37. The UV/OV pin should be bypassed using a 1 nF capacitor to prevent triggering the UV/OV circuit during normal switching operation.

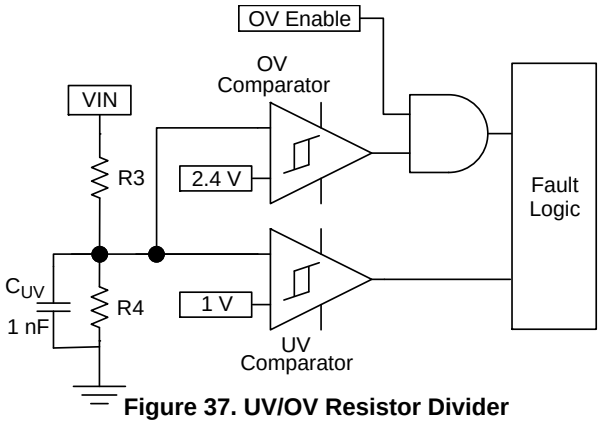


Figure 37. UV/OV Resistor Divider from the Input Line

The resistive network impedance must not be too high to keep good voltage accuracy and not too low to minimize power losses. A 200 kΩ to 1.2 MΩ range is recommended for the high side resistor R3. If the designer wanted to set the undervoltage threshold to 32 V, the resistor divider should be designed according to the following equation:

$$R4 = \frac{V_{UV} \times R3}{V_{IN\_UV} - V_{UV}} \rightarrow \quad \text{(eq. 3)}$$

$$34.49\ k\Omega = \frac{1.067 \times 1\ M\Omega}{32\ V - 1.067} \approx 34.0\ k\Omega\ (R96\ Value)$$

The OV threshold monitored at the UV/OV pin is 2.41 times higher than the UV threshold, leading to an OV threshold of 73.3 V for the calculated R96 value. Designers can quickly set the OV/UV thresholds by referencing Figure 38.

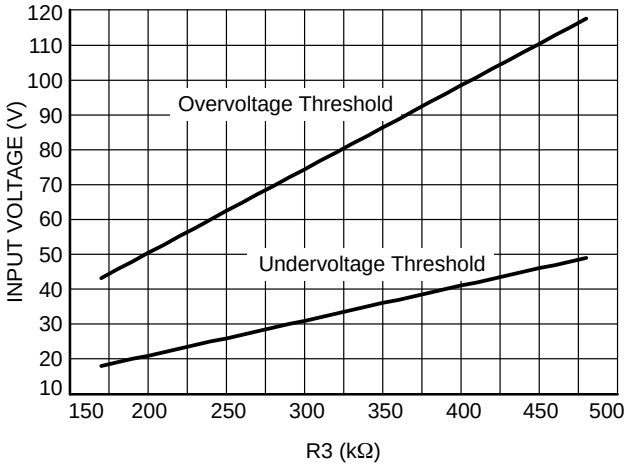


Figure 38. UV/OV Resistor Divider Thresholds with R4 Set to 10 k

The UV/OV pin can also be used to implement a remote enable/disable function. If an external transistor pulls the UV/OV pin below 1.0 V (or above 2.4 V) the converter will be disabled and no switching is allowed. A device version is available without the OV protection feature, see the ordering information section.

Error Amplifier

The internal error amplifier (EA) regulates the output voltage of the bias supply. The scaled signal is fed into the feedback pin (VFB) which is the inverting input of the error amplifier. It compares a scaled voltage signal to an internal trimmed 2.5 V reference connected to its non−inverting input.

The output of the error amplifier is internally connected to a PWM comparator and also available externally through the COMP pin for frequency compensation. To insure normal operation, the EA compensation should be selected such that the EA frequency response crosses 0 dB below 80 kHz.

The error amplifier feedback bias current is less than 200 nA over the operating range. The output source and sink currents are typically 95 μA and 700 μA, respectively.

Under load transient conditions, COMP may need to move from the bottom to the top of the C_T ramp. A large current is required to complete the COMP swing if small resistors or large capacitors are used to implement the compensation network. In which case, the COMP swing will be limited by the EA source current. Optimum transient responses are obtained if the compensation components allow the COMP pin to swing across its operating range in 1 cycle.

Oscillator, Voltage Feed Forward, and Sync Capability

The oscillator is optimized for operation up to 1 MHz and its frequency is set by the external timing capacitor (C_T) connected to the C_T pin. The oscillator has two modes of operation: free running and synchronized (sync). While in free running mode, an internal current source sequentially charges and discharges C_T generating a voltage ramp between 3.0 V and 3.5 V. Under normal operating conditions, the charge (I_{CT_C}) and discharge (I_{CT_D}) currents are typically 172 μA and 515 μA, respectively. The charge/discharge current ratio of 1:3 discharges C_T in 25% of the total period. The power switch is disabled while C_T is discharging, guaranteeing a maximum duty cycle of 75% as shown in Figure 39.

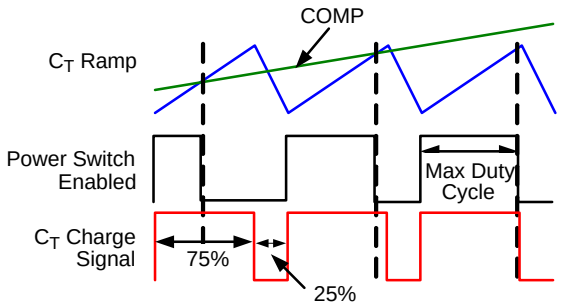


Figure 39. Auxiliary Winding Operation with Output Overload Timing Diagram

The oscillator frequency should be set no more than 25% below the target sync frequency to maintain an adequate voltage ramp and provide good noise immunity. A possible circuit to synchronize the oscillator is shown in Figure 40.

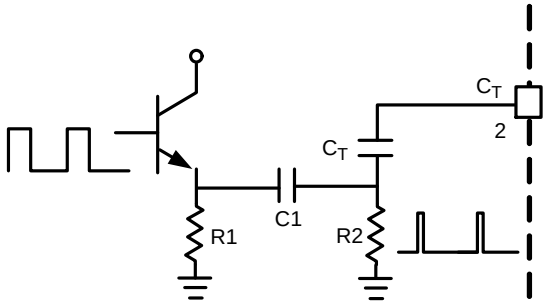


Figure 40. External Frequency Synchronization Circuit

Voltage feed forward can be implemented by connecting a resistor from the input voltage to the C_T pin. RFF supplies a current that allows the input voltage to modify the maximum duty cycle rather than the standard 75% maximum. If the designer wanted to implement a fixed lower duty cycle, a resistor can be tied to a fixed voltage source such as V_{AUX} or a voltage reference. If voltage feed forward is used, the frequency can shift dramatically depending on the value of the resistor.

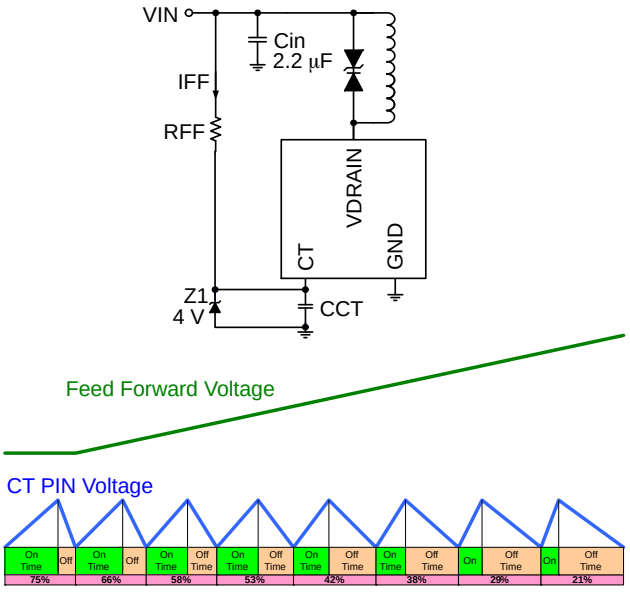


Figure 41. Voltage Feed Forward

$$R_{VFF} = \frac{VIN_{MIN} - Ramp}{I_{CT\_D} - D_{MAX} \times \left(I_{CT\_C} + I_{CT\_D}\right)} \rightarrow \quad \text{(eq. 4)}$$

$$320\ k\Omega = \frac{32\ V - 3.25\ V}{517\ \mu A - 62\% \times \left(172\ \mu A + 517\ \mu A\right)}$$

PWM Comparator and Latch

The Pulse Width Modulator (PWM) comparator compares the error amplifier output (COMP) to the C_T ramp and generates a proportional duty cycle. The power switch is disabled while COMP voltage is below the C_T ramp signal. Once COMP reaches the ramp signal, the power switch is enabled. If COMP is at the bottom of the C_T ramp, the converter operates at minimum duty cycle. While COMP increases, the duty cycle increases until COMP reaches the peak of the C_T ramp, at which point the controller operates at maximum duty cycle.

The C_T charge signal is filtered through a one shot pulse generator to set the PWM latch and enable switching at the beginning of each period. Switching is allowed while the C_T ramp is below COMP and a current limit fault is not present.

The pulse width modulation technique is seen in Figure 39.

The PWM comparator and latch propagation delay are less than 200 ns. If the system is designed to operate with a minimum on time less than 200 ns (no or light load), the converter will skip pulses. Skipping pulses is usually not a problem, unless operating at a frequency close to the audible range. Skipping pulses is more likely when operating at high frequencies during high input voltage and minimum load conditions.

A 2 kΩ series resistor is included for ESD protection between the internal EA output and the COMP pin. Under normal operation, a 220 mV offset is observed between the C_T ramp and the COMP crossing points. The series resistor does not interact with the error amplifier transfer function.

Programmable Current Limit

The power switch circuit incorporates SENSEFET® technology to monitor the drain current. A sense voltage is generated by driving a sense element, R_{SENSE}, with a current proportional to the drain current. The sense voltage is compared to an externally programmable reference voltage on the non−inverting input of the current limit comparator. If the sense voltage exceeds the setup reference level, the comparator resets the PWM latch and the switching cycle is terminated. The reference level threshold is programmable by a resistor (R_{CL}) connected to the CL pin shown in Figure 42.

By limiting the peak current to the needs of the application, the transformer sizing can be scaled appropriately to the specific requirements which allows the PCB footprint to be minimized. The NCP1032 maximum drain current limit thresholds are 512 mA.

$$R_{CL} = 114 \times \ln(Rset) - 142 \quad Rset < 42.2\ k\Omega \quad \text{(eq. 5)}$$

$$R_{CL} = 309 \times \ln(Rset) - 893 \quad 200\ k\Omega > Rset > 42.2\ k\Omega$$

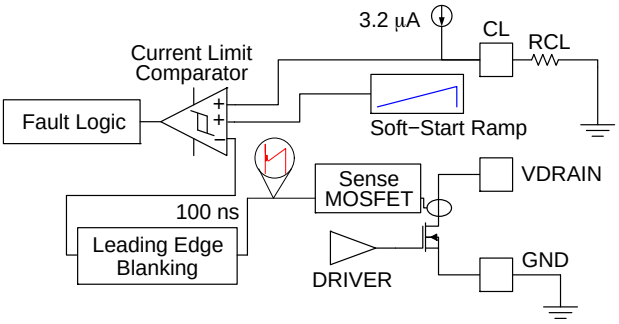


Figure 42. Current Limit Threshold and Propagation Delay

The propagation delay is measured from the time an overcurrent fault appears at power switch circuit drain, to the start of the turn−off transition as shown in Figure 43. The current limit propagation delay time is typ. 100 ns. The propagation must be accounted for when designing the power supply, as it will result in a constant power output through the transformer when the output is shorted. The constant power can cause the transformer to rise in temperature permanently damaging the magnetics. This can be mitigated by placing a 10 Ω resistor in series with the output rectification diode.

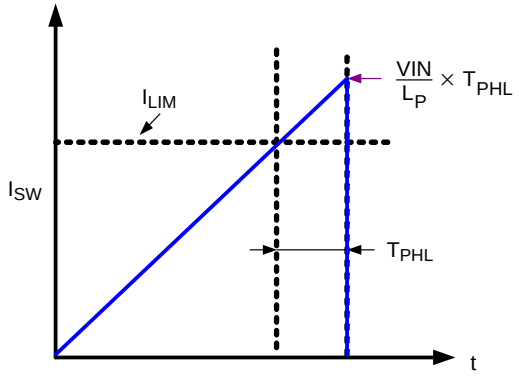


Figure 43. Current Limit Threshold and Propagation Delay

Adaptive Leading Edge Blanking

Each time the power switch circuit is turned on, a narrow voltage spike appears across R_{SENSE}. The spike is due to the power switch circuit gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The spike can cause a premature reset of the PWM latch. A proprietary active Leading Edge Blanking (LEB) circuit masks the current signal to prevent the voltage spike from resetting the PWM latch. The active LEB masks the current signal until the power switch turn on transition is complete. The adaptive LEB period provides better current limit control compared to a fixed blanking period.

Power Switch Circuit Protection

The NCP1032 monolithically integrates a 200 V power switch with control logic circuitry. The power switch is designed to directly drive the converter transformer. The gate drive is tailored to control switching transitions and help limit electromagnetic interference (EMI).

For a Flyback topology a large transient voltage spike appears at the transformers primary side after the power switch turns off. These spikes are a function of the transformer leakage inductance (L_{LP}) on either the primary or secondary side. A circuit is needed to clamp the leakage spike, limiting the voltage drain excursion to a safe value. The operating V_{DRAIN_MAX} is 200 V as depicted in Figure 44. Two such circuits are the passive RCD network or a zener clamp as depicted in Figure 45 and Figure 46.

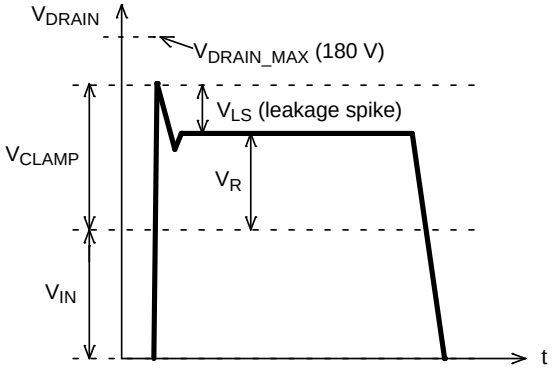


Figure 44. Power Switch Waveforms with Clamping

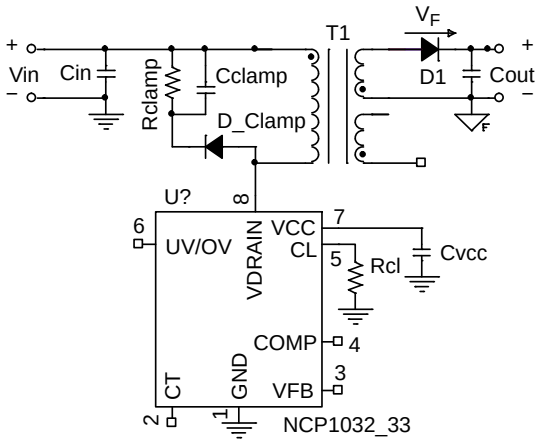


Figure 45. Passive RCD Clamp Network

The passive RCD network is the most standard circuitry and the formula below is used to calculate R_{CLAMP} and C_{CLAMP}.

$$R_{CLAMP} = \frac{2 \times V_{CLAMP} \times \left(V_{CLAMP} - (V_{OUT} + V_F) \times N\right)}{L_{LP} \times I_{PEAK}{}^2 \times F_{SW}}$$

$$C_{CLAMP} = \frac{V_{CLAMP}}{V_{LS} \times F_{SW} \times R_{CLAMP}} \quad \text{(eq. 6)}$$

The voltage leakage spike (V_{LS}) is usually selected 50 to 70% above the reflected value $V_R = N \times (V_{OUT} + V_F)$ and ($V_{IN} + V_{CLAMP}$) must be below the operating $V_{DRAIN−MAX}$ which is 200 V. The diode used for the clamping circuit needs to be at minimum fast or ultrafast recovery and an MURA110 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. The worse case occurs when I_{PEAK} and V_{IN} are at the maximum.

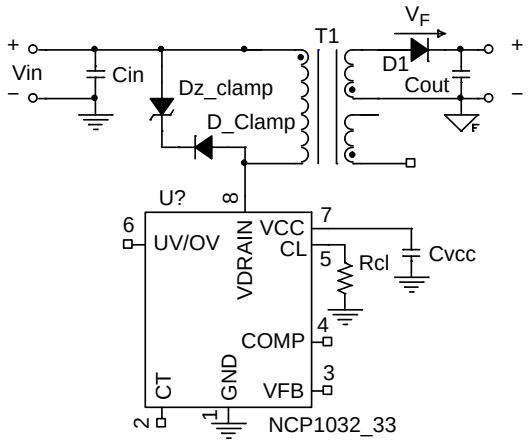


Figure 46. Zener Clamp Network

The zener diode is probably the most expensive but offers the best protection and a very precise clamping level. Select the zener voltage to set V_{LS} level between 10 to 15 V above the reflected voltage V_R so VZener = V_{LS} + V_R. The zener diode must be able to handle the voltage rating and power dissipation during the switch turn−off time. For the NCP1032, a 0.5 W zener diode, like the MMSZ47T1 is suitable.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at 165°C, the power switch circuit is disabled. Once the junction temperature falls below 145°C, the NCP1032 is allowed to resume normal operation. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heat sinking.

Application Considerations

Typical Applications

A 12 V / 3 W bias supply for 36 V to 75 V telecom systems, 1500 V isolation DC−DC converters. The NCP1032 is configured in Flyback topology and operates in Discontinuous Conduction Mode (DCM) to offer a low−cost, high efficiency solution. The circuit schematic is shown in Figure 47. Transformer T1 is available as a CoilCraft B0226−EL. Capacitor C_{CT} sets the switching frequency at approximately 300 kHz.

Output voltage regulation and overall efficiency are shown in Figure 3 and Figure 4 on page 6. The resistor divider formed by R3 and R4 sets the undervoltage lockout threshold at about 32 V.

Application Note AND8119/D describes the design of this bias supply system.

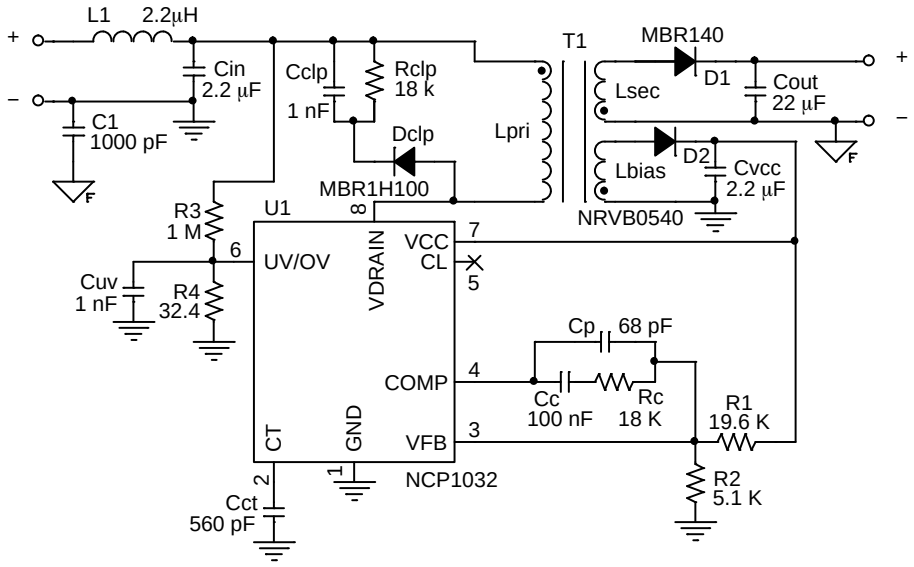


Figure 47. 48 V to Isolated 12 V / 3 W Bias Supply Schematic

Layout Recommendations

To prevent EMI problems high current copper traces which have high frequency switching should be optimized. Therefore, use short and wide traces for power current paths and for power ground traces especially transformer trace connections (primary and secondary). When power is transferred from input to output, there is a period of time when the power switch is on, referred to as “on time,” and a period of time when the switch is off, referred to as “off time.” When the power switch is on, the input voltage is applied across the primary side of the transformer and current increases in the primary inductance. Further, when the power switch is on the output current is supplied from the output capacitance. When the power switch is off, current on the primary side conducts through the clamp or snubber circuit. On the secondary side current is conducting through the rectification diode, providing power to the output and replenishing energy in the output capacitances as shown in Figure 48. Electromagnetic radiation is minimized by keeping VDRAIN leads, output diode, and output bypass capacitor leads as short as possible. It is important to minimize the area of the VDRAIN nodes and used the ground plane under the switcher circuitry to prevent interplane coupling and minimize cross−talk to sensitive signals and ICs. The exposed pad of the package must be connected to the ground plane of the board which is important for EMI and thermal management. Finally, it is always good practice to keep sensitive traces such as feedback connection (VFB and COMP) as far away from switched signal connections (VDRAIN) as possible. Figure 48 shows an example of an optimized PCB layout.

Thermal Considerations

Careful attention must be paid to the internal power dissipation of the NCP1032. Power dissipation is a function of efficiency and output power. As output power requirements increase, proper component selection includes adjusting RDSON, forward voltage of diodes, and enlarging packages. For example, if a transformer’s size were increased to lower the DCR or/and increase the inductance efficiency will improve at heavier loads. The exposed thermal pad is designed to be soldered to the ground plane used as a heat sink. The ground plane size should be maximized and connected to the internal and bottom copper ground planes with thermal vias placed directly under the package to spread heat generated by the NCP1032 as depicted Figure 48.

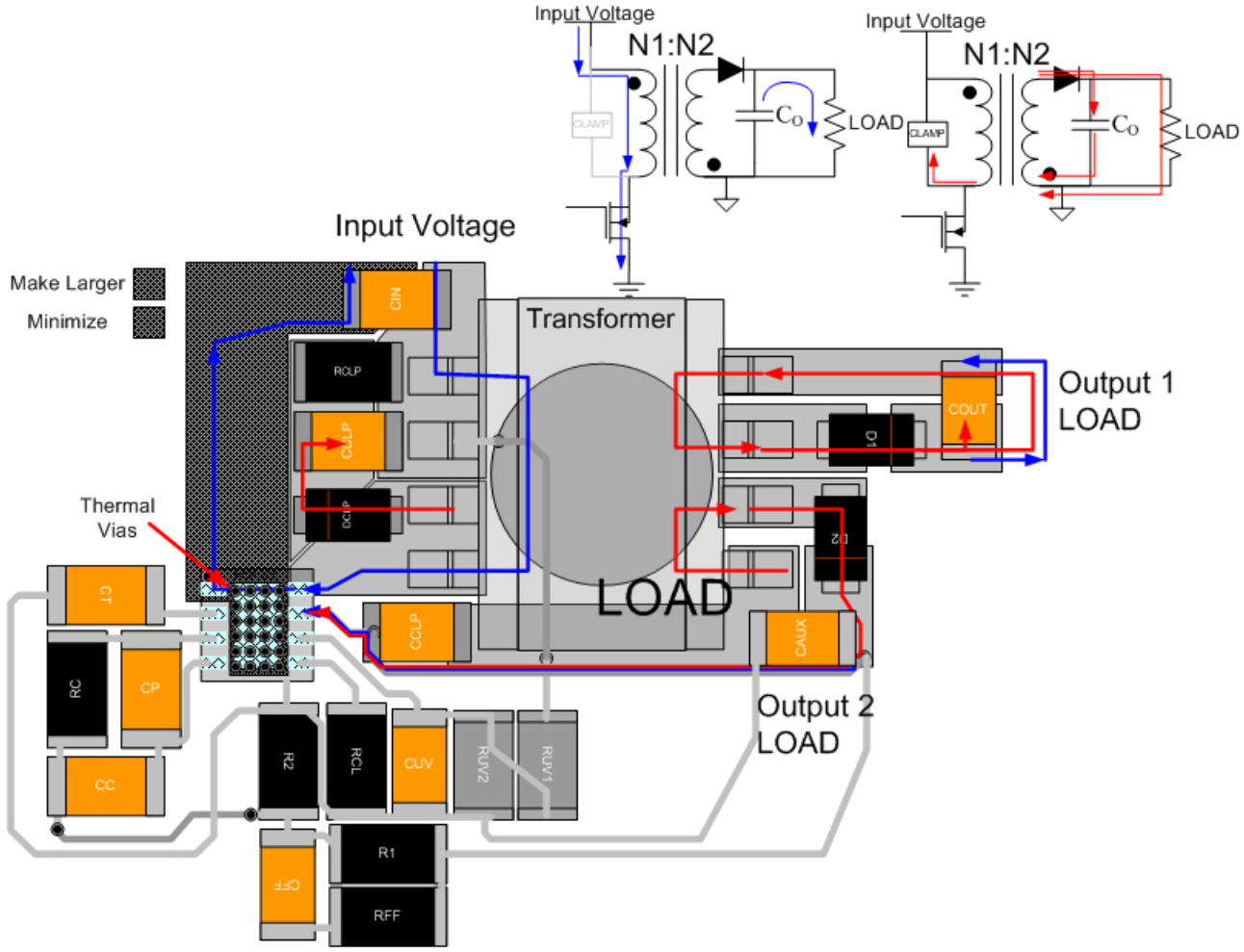


Figure 48. Recommended PCB Layout

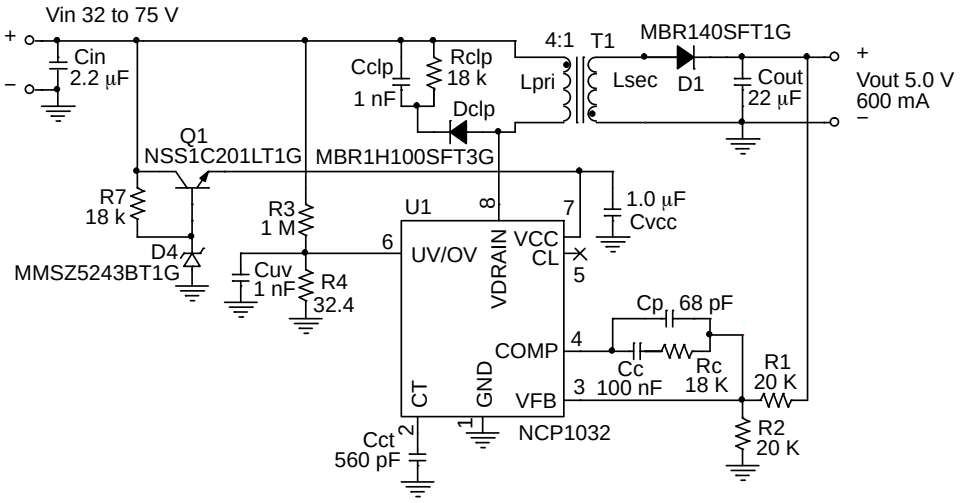


Figure 49. 48 V to 5.0 V DC−DC Converter Without Auxiliary Winding

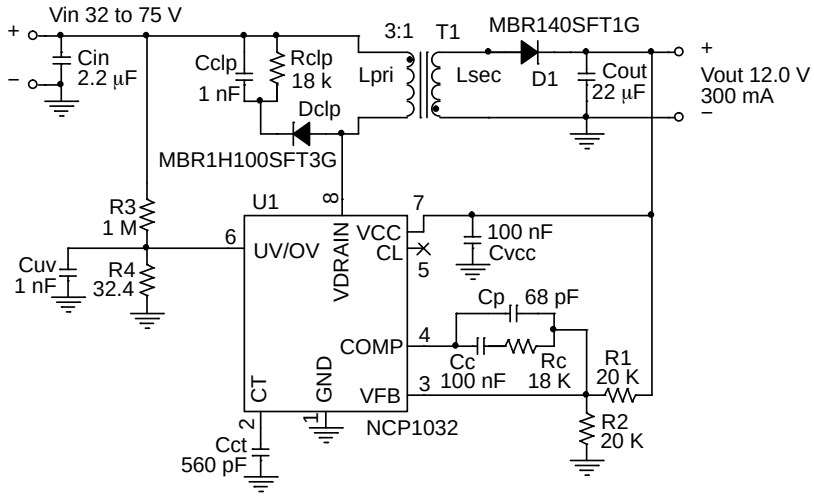


Figure 50. 48 V to 12.0 V DC−DC Converter Without Auxiliary Winding

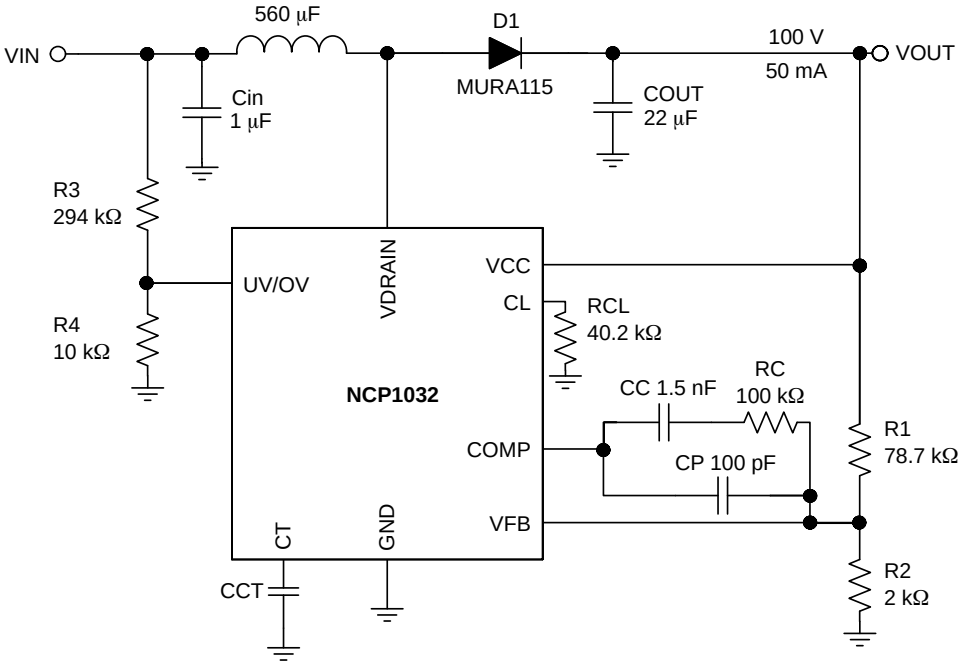


Figure 51. Typical Application Circuit Boost Circuit Configuration

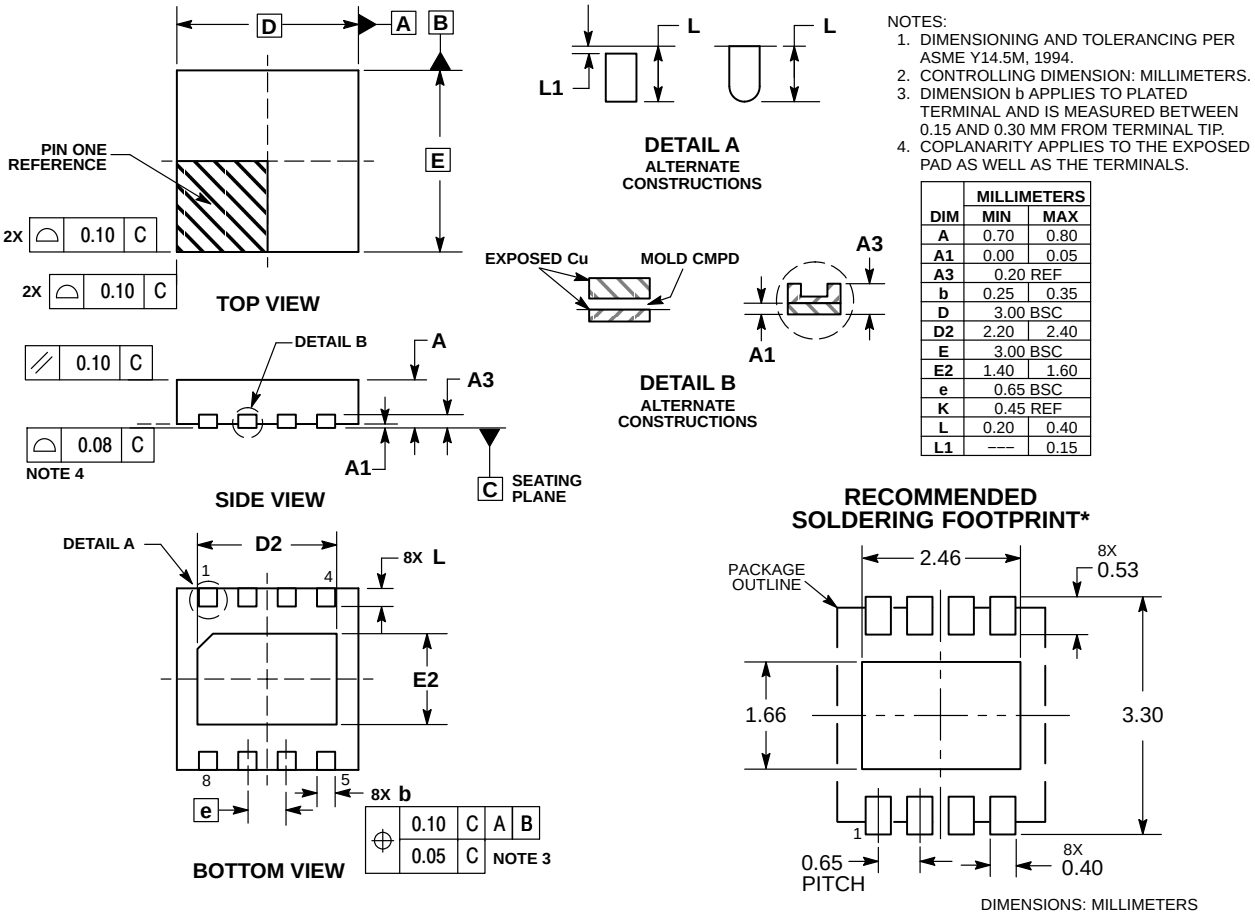
ORDERING INFORMATION

Device	OV Protection	Marking	Package	Shipping†
NCP1032AMNTXG	Enable	1032A	WDFN8 3x3 (Pb−Free)	3,000 / Tape & Reel
NCP1032BMNTXG	Disable	1032B	WDFN8 3x3 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WDFN8 3x3, 0.65P
CASE 511BH
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.20	2.40
E	3.00 BSC	
E2	1.40	1.60
e	0.65 BSC	
K	0.45 REF	
L	0.20	0.40
L1	−−−	0.15

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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