NIPPON PRECISION CIRCUITS INC.

SM5852CS

Dynamic Range Compression LSI

OVERVIEW

The SM5852CS is a digital signal processor IC that performs dynamic range compression for use in digital audio reproduction equipment. It is designed for use with a 44.1 kHz sampling frequency.

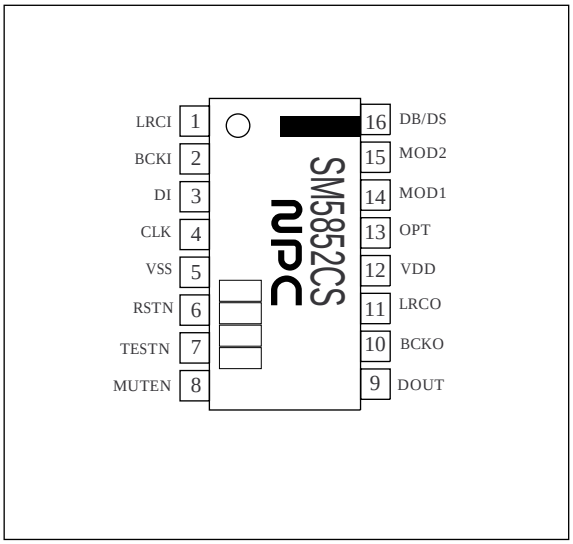
FEATURES

- 2-channel processing
- 6 input-level dependent dynamic gain characteristics
- Dynamic range compression bypass mode
- 2 attack time settings
- Soft muting function
- Serial input/output interface
  2s complement, MSB first, 16-bit
- 384fs system clock
- 23 × 23-bit multiplier/30-bit high-precision accumulator
- TTL-compatible input/output
- 3.2 to 5.5 V operating voltage range
- 16-pin SOP
- Molybdenum-gate CMOS

ORDERING INFOMATION

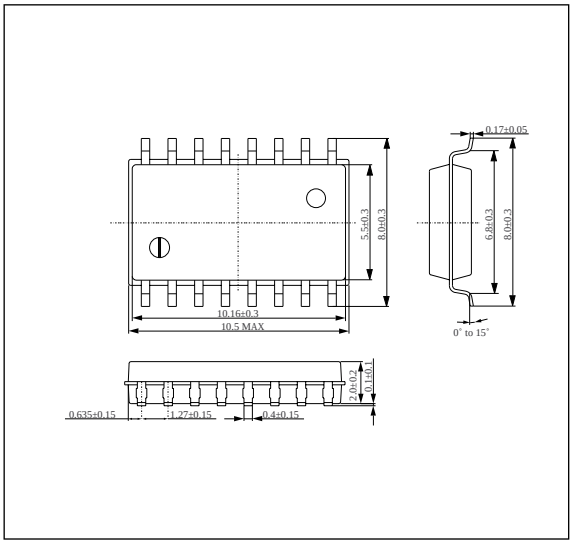
Device	Package
SM5852CS	16pin SOP

PINOUT

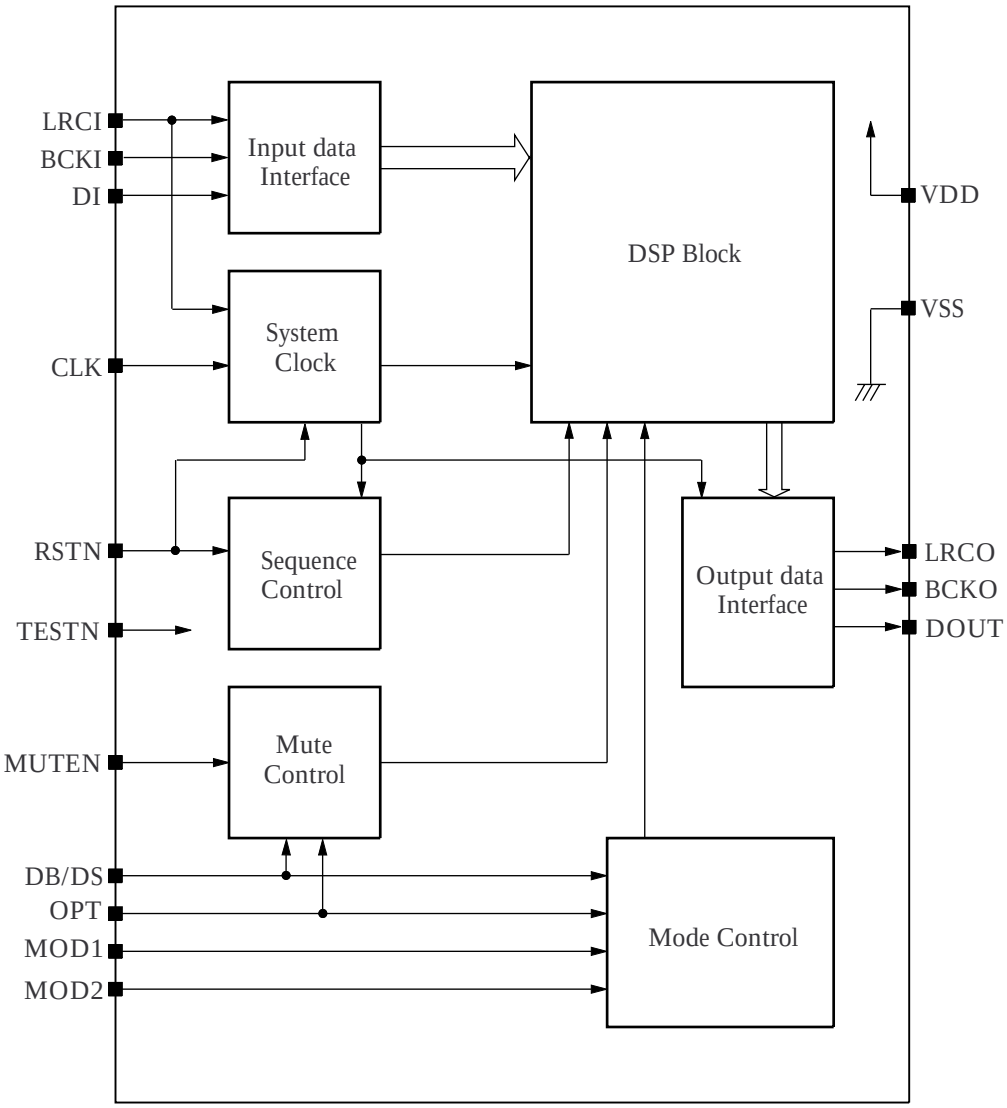


PACKAGE DIMENSIONS

16-pin SOP (Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O[1]	Description
1	LRCI	Ip	Input data sample rate (fs) clock input
2	BCKI	Ip	Bit clock input
3	DI	Ip	Serial data input
4	CLK	I	Clock input
5	VSS	–	Ground
6	RSTN	Ip	System reset initialization. Reset when LOW.
7	TESTN	Ip	Test mode input. Testing when LOW.
8	MUTEN	Ip	Mute input. Muting when LOW.
9	DOUT	O	Serial data output
10	BCKO	O	Bit clock output
11	LRCO	O	Output data sample rate (fs) clock output
12	VDD	–	3.2 to 5.5 V supply
13	OPT	Ip	Attack time switch input. Attack-1 when HIGH, and attack-2 when LOW.
14	MOD1	Ip	Gain characteristics switch inputs.
15	MOD2	Ip	
16	DB/DS	Ip	

DB/DS	MOD2	MOD1	Compression mode
LOW	LOW	LOW	6
LOW	LOW	HIGH	5
LOW	HIGH	LOW	4
LOW	HIGH	HIGH	Off
HIGH	LOW	LOW	3
HIGH	LOW	HIGH	2
HIGH	HIGH	LOW	1
HIGH	HIGH	HIGH	Off

1. Ip = Input pin with pull-up resistor. Accordingly, they can be left open for HIGH-level input.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.3 to 7.0	V
Input voltage	V_{IN}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature	T_{stg}		–40 to 125	°C
Power dissipation	P_D		250	mW
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		3.2 to 5.5	V
Operating temperature	T_{opr}		–35 to 85	°C

DC Characteristics

Standard voltage: V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –35 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption[1]	I_{DD}	V_{DD} = 5.0 V	–	16	23	mA
Input voltage for all inputs	V_{IH}		2.4	–	–	V
	V_{IL}		–	–	0.5	V
Output voltage for all outputs	V_{OH}	I_{OH} = –0.4 mA	2.5	–	–	V
	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
Input leakage current for all inputs	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA
CLK input leakage current	I_{LL}	V_{IN} = 0 V	–	–	1.0	µA
Input current for all inputs except CLK	I_{IL}	V_{IN} = 0 V	–	–	20	µA

1. f_{CLK} = 384fs = 16.9344 MHz, no output load, input data conformance with NPC test pattern

Low voltage: V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption[1]	I_{DD}	V_{DD} = 3.4 V	–	7	10	mA
Input voltage for all inputs	V_{IH}		2.4	–	–	V
	V_{IL}		–	–	0.5	V
Output voltage for all outputs	V_{OH}	I_{OH} = –0.2 mA	2.5	–	–	V
	V_{OL}	I_{OL} = 0.8 mA	–	–	0.4	V
Input leakage current for all inputs	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA
CLK input leakage current	I_{LL}	V_{IN} = 0 V	–	–	1.0	µA
Input current for all inputs except CLK	I_{IL}	V_{IN} = 0 V	–	–	12	µA

1. f_{CLK} = 384fs = 16.9344 MHz, no output load, input data conformance with NPC test pattern

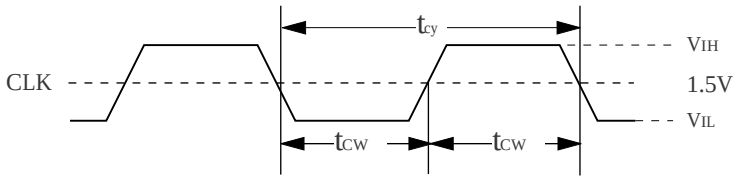
AC Characteristics

Standard voltage: V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –35 to 85 °C

Low voltage: V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

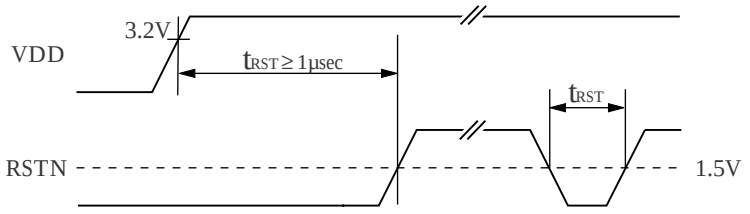
CLK (384fs)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock pulsewidth	t_{CW}		24	–	500	ns
Clock cycle time	t_{CY}		55	59	1000	ns



RSTN

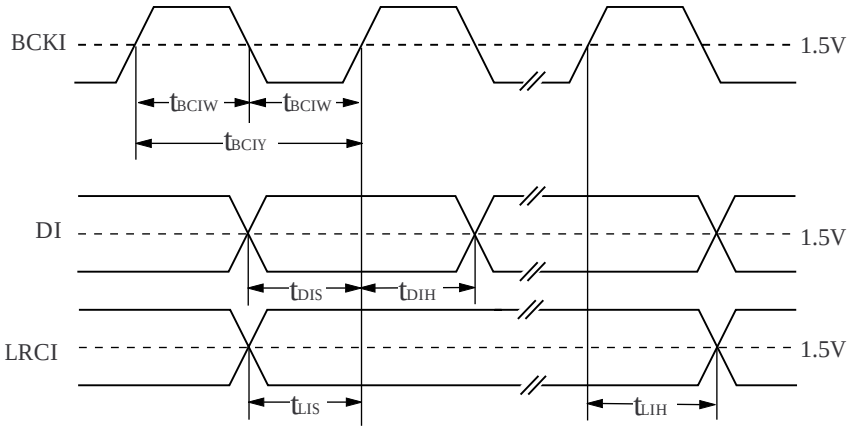
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reset LOW-level pulsewidth	t_{RST}	At power-ON	1	–	–	µs
		At all other times	50	–	1000	ns



RSTN should be set LOW at power-ON and after reacquiring synchronization. Note that if RSTN is LOW for longer than 1 µs, a through-current flows in the internal dynamic circuits because the internal clock is stopped. The through-current has no rated value, so the reset pulse should be kept as short as possible at all times other than at power-ON.

Serial input timing

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKI pulsewidth	t_{BCIW}		100	–	–	ns
BCKI cycle time	t_{BCIY}		200	–	–	ns
DI setup time	t_{DIS}		75	–	–	ns
DI hold time	t_{DIH}		75	–	–	ns
LRCI setup time	t_{LIS}		75	–	–	ns
LRCI hold time	t_{LIH}		75	–	–	ns



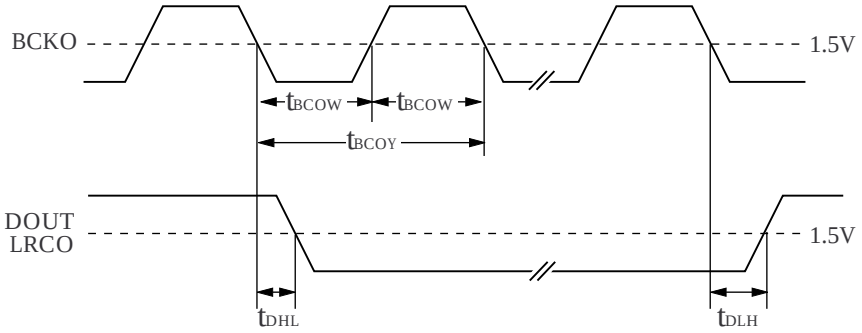
DB/DS, OPT

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Minimum pulsewidth	t_W		2/fs	–	–	ns

When DB/DS or OPT change state, the input level must be constant for a minimum of 2/fs (2 × LRCI cycle time). Input levels of duration less than 2/fs may be ignored.

Serial output timing

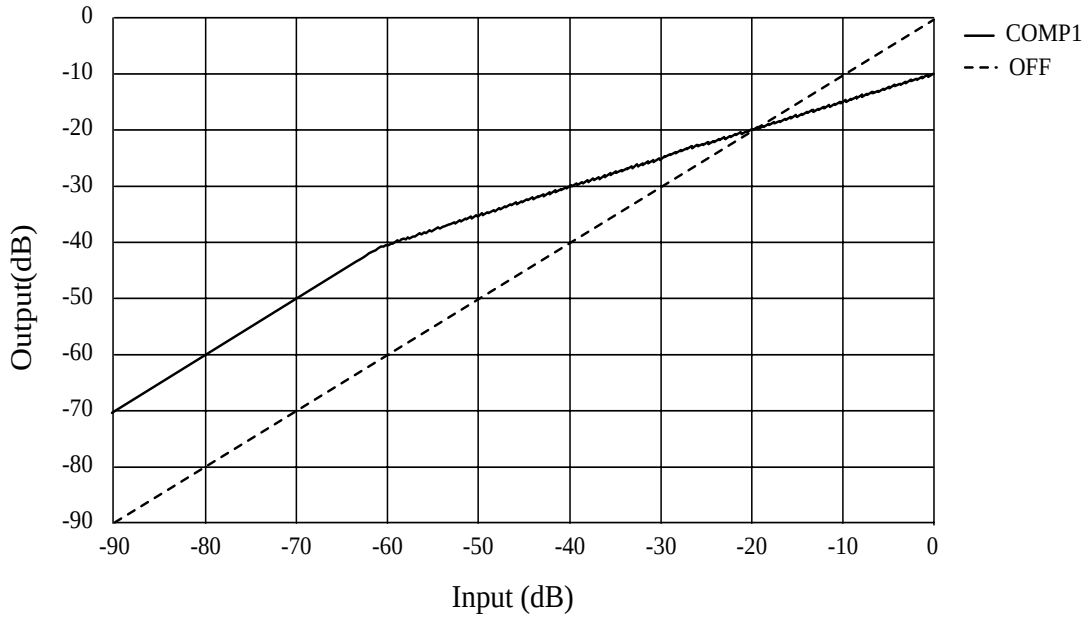
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKO pulsewidth	t_{BCOW}	15 pF load	180	1/96fs	–	ns
BCKO cycle time	t_{BCOY}	15 pF load	400	1/48fs	–	ns
DOUT, LRCO output delay time	t_{DHL}	15 pF load	–20	–	60	ns
	t_{DLH}	15 pF load	–20	–	60	ns



Dynamic Compression Characteristics

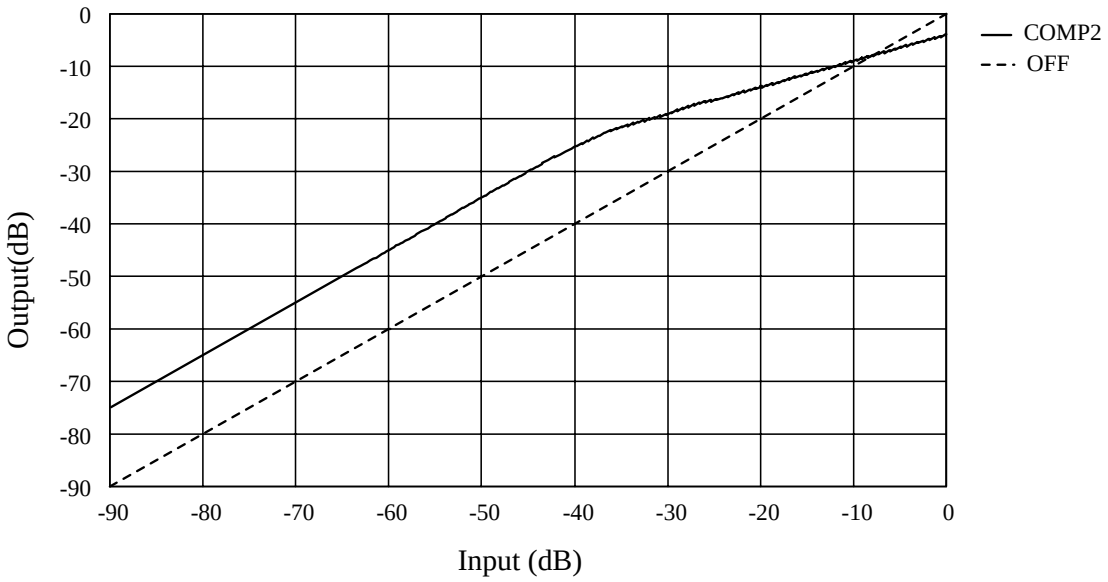
Compression mode 1 (DB/DS = HIGH, MOD2 = HIGH, MOD1 = LOW)

Compression	Compression ratio	Input level	Output level
Mode 1	30 dB	≤ –60 dB	+20 dB linear relative to input
		–60 to 0 dB	–40 to –10 dB



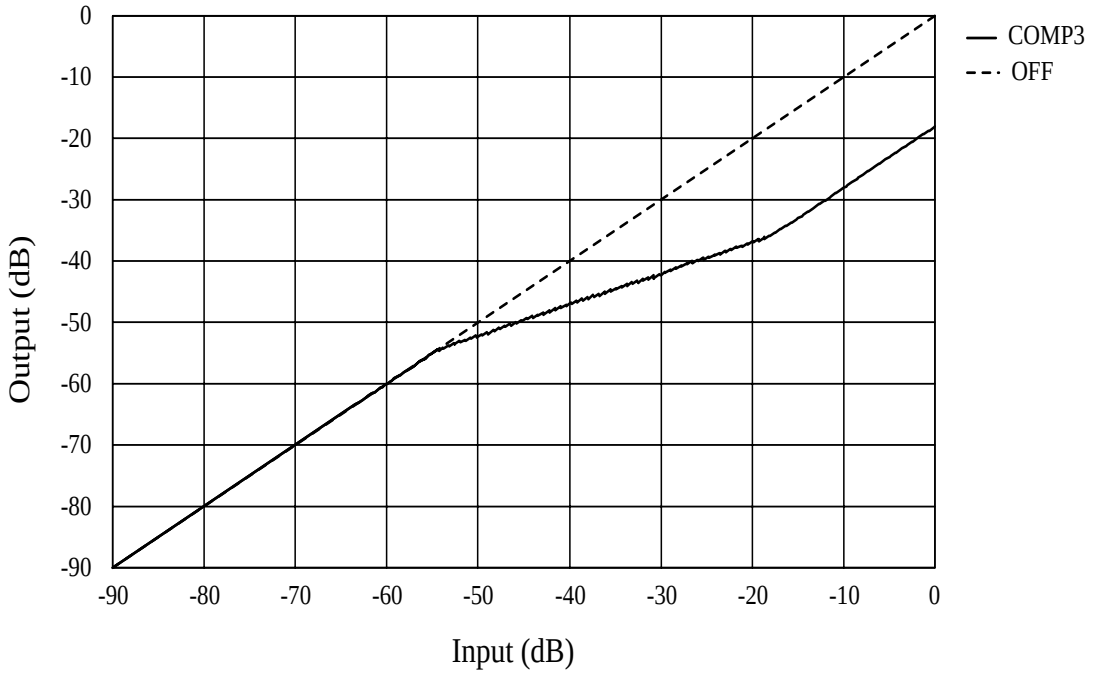
Compression mode 2 (DB/DS = HIGH, MOD2 = LOW, MOD1 = HIGH)

Compression	Compression ratio	Input level	Output level
Mode 2	19 dB	≤ –38 dB	+15 dB linear relative to input
		–38 to 0 dB	–23 to –4 dB



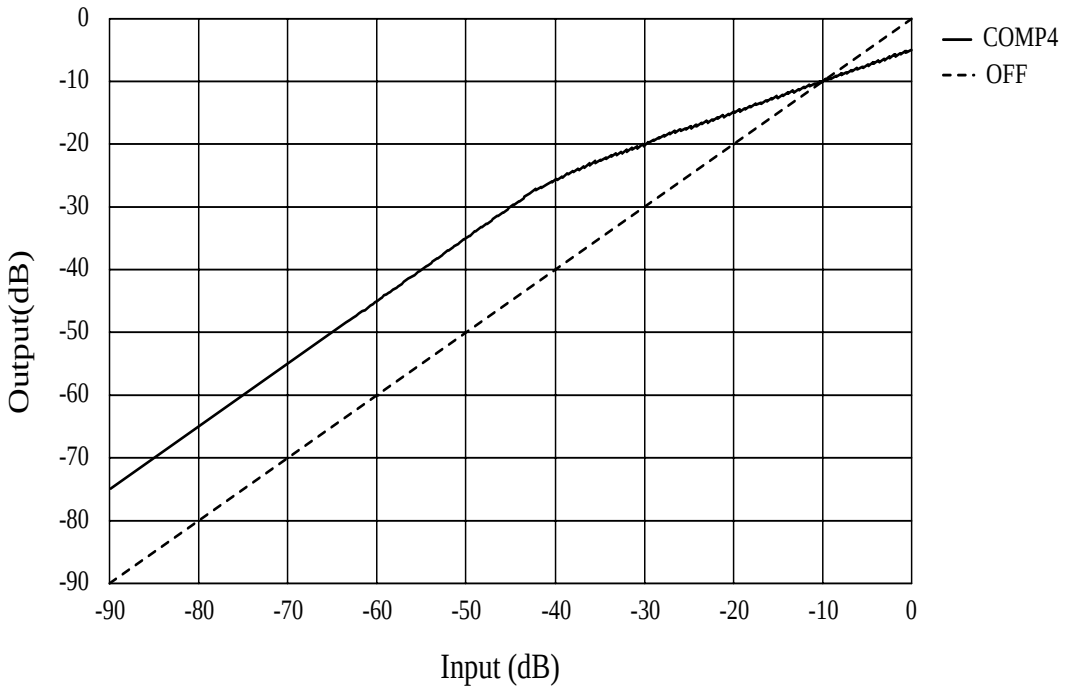
Compression mode 3 (DB/DS = HIGH, MOD2 = LOW, MOD1 = LOW)

Compression	Compression ratio	Input level	Output level
Mode 3	18 dB	≤ –54 dB	+0 dB linear relative to input
		–54 to –18 dB	–54 to –36 dB
		–18 to 0 dB	–36 to –18 dB



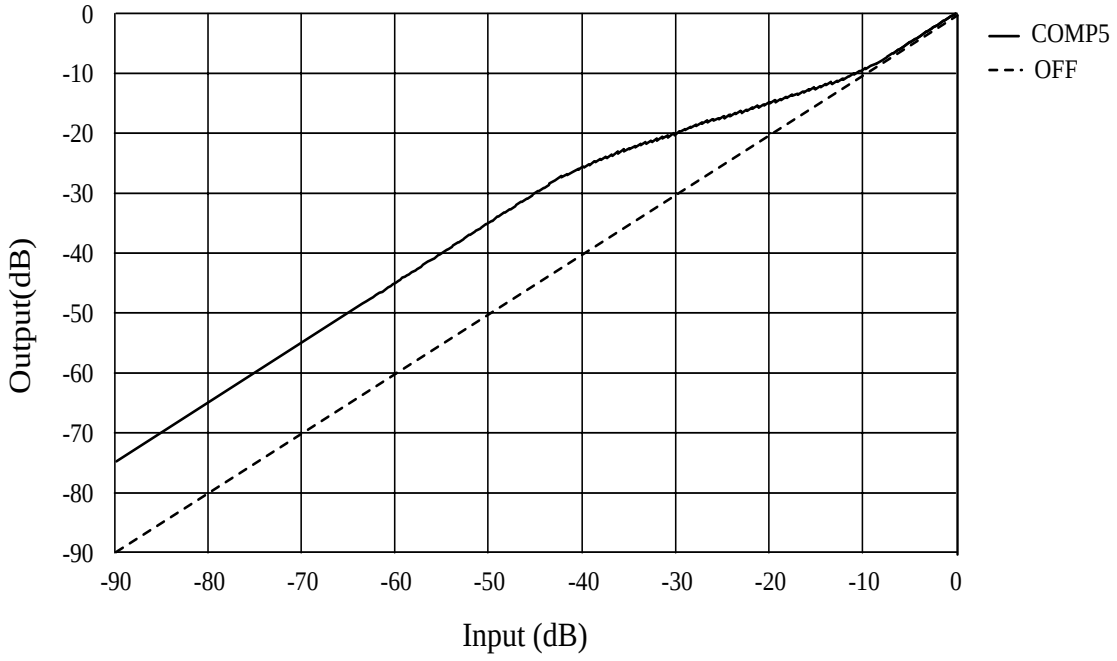
Compression mode 4 (DB/DS = LOW, MOD2 = HIGH, MOD1 = LOW)

Compression	Compression ratio	Input level	Output level
Mode 4	20 dB	≤ –40 dB	+15 dB linear relative to input
		–40 to 0 dB	–25 to –5 dB



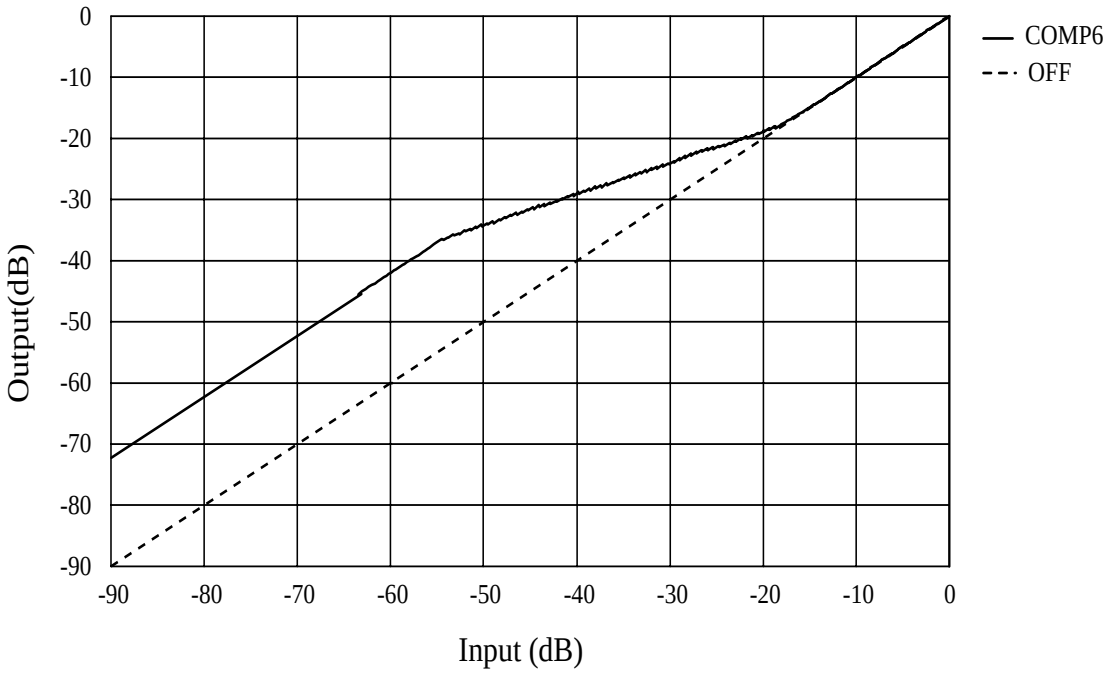
Compression mode 5 (DB/DS = LOW, MOD2 = LOW, MOD1 = HIGH)

Compression	Compression ratio	Input level	Output level
Mode 5	15 dB	≤ –40 dB	+15 dB linear relative to input
		–40 to –10 dB	–25 to –10 dB
		–10 to 0 dB	+0 dB linear relative to input



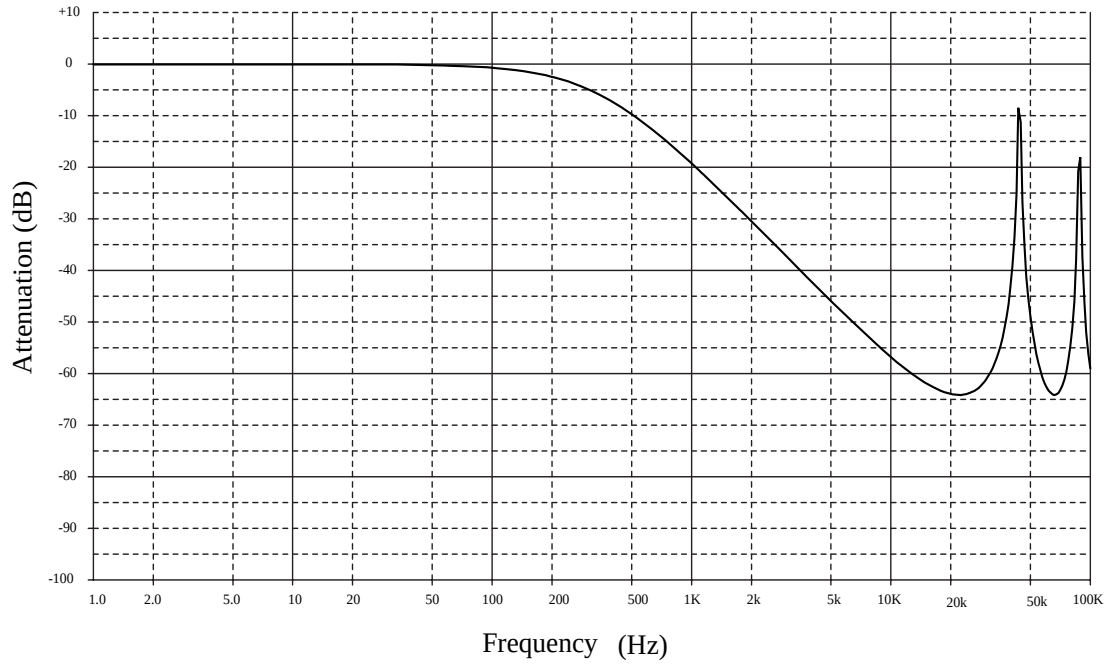
Compression mode 6 (DB/DS = LOW, MOD2 = LOW, MOD1 = LOW)

Compression	Compression ratio	Input level	Output level
Mode 6	18 dB	≤ –54 dB	+18 dB linear relative to input
		–54 to –18 dB	–36 to –18 dB
		–18 to 0 dB	+0 dB linear relative to input

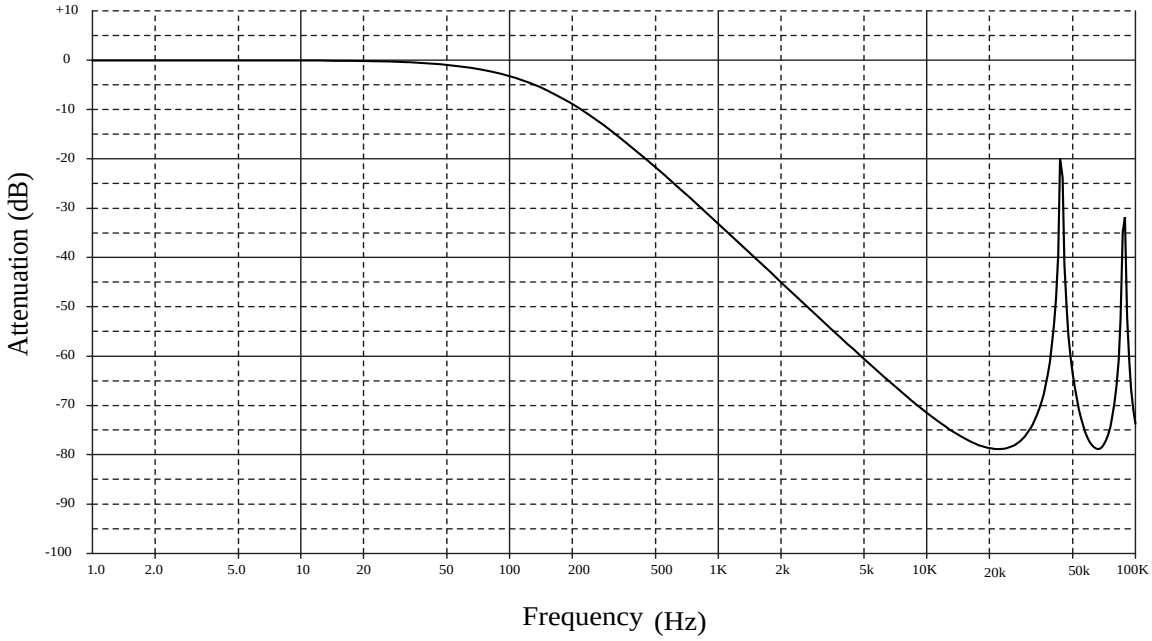


Filter Characteristics

Attack-1 filter



Attack-2 filter



FUNCTIONAL DESCRIPTION

Dynamic Range Compression

Dynamic range compression varies the effective amplification of the input as a function of the input signal level. The mode control block selects one of 6 dynamic range compression characteristics according the states of DB/DS, MOD1 and MOD2. Also, dynamic range compression can be turned OFF, bypassing all processing.

DB/DS	MOD2	MOD1	Compression mode
LOW	LOW	LOW	6
LOW	LOW	HIGH	5
LOW	HIGH	LOW	4
LOW	HIGH	HIGH	Off
HIGH	LOW	LOW	3
HIGH	LOW	HIGH	2
HIGH	HIGH	LOW	1
HIGH	HIGH	HIGH	Off

Attack Time Selection

The input interface block incorporates a peak hold circuit to determine the input level. The peak hold circuit has a time constant of τ = 250 ms, and the peak hold output is attenuated and then compared with the next input level. Therefore, the dynamic range compression recovery time constant is effectively τ = 250 ms.

The attack time coefficient of the input signal, to pass through the selected attack time LPF, is determined by the input level.

Two attack time low-pass filter characteristics are available, selected by the state of OPT.

- OPT = HIGH, Attack-1 characteristics, f_C = 350 Hz, 2nd-order LPF (Q = 0.5)
- OPT = LOW, Attack-2 characteristics, f_C = 150 Hz, 2nd-order LPF (Q = 0.5)

The attack time is the time required by the circuit to return to the set value after a sudden increase in the input. The recovery time is the time required by the circuit to return to the set value after a sudden decrease in the input.

Soft Muting

Soft muting is active when MUTEN is LOW. When MUTEN is LOW, the attenuation changes smoothly from 0 to −∞ dB in 1024/fs, or approximately 23.2 ms.

When MUTEN goes HIGH, soft muting is released and the attenuation changes smoothly from −∞ to 0 dB, again taking approximately 23.2 ms.

Also, if a MUTEN transition occurs while the attenuation is changing, the attenuation then changes smoothly in the direction specified by the new level of MUTEN.

DB/DS, OPT Switching Shock Noise

The soft muting function is also activated to eliminate switching shock noise when DB/DS or OPT change state. When DB/DS or OPT change state, the attenuation changes to −∞ dB, the internal circuit settings are activated and then soft muting is released. Therefore, a maximum time of approximately 46.4 ms is required to change the compression mode. Of course, if the attenuation is already −∞ dB after soft muting using MUTEN, then no time is required to change compression mode.

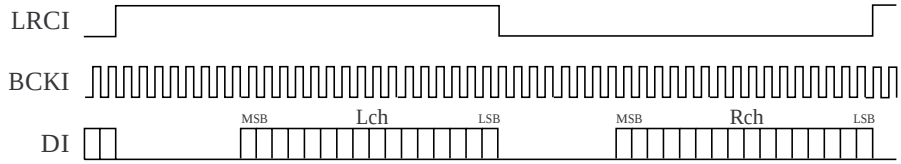
Reset Initialization

RSTN should be set LOW at power-ON and after reacquiring synchronization. Note that if RSTN is LOW for longer than 1 µs, a through-current flows in the LSI's internal dynamic circuits because the internal clock is stopped. The through-current has no rated value, so the reset pulse should be kept as short as possible at all times other than at power-ON.

When RSTN goes from LOW to HIGH, initialization hold is released and the initialization routine first resets the internal data over an interval of 4fs. During the initialization routine, the output data is forcibly muted so that there is no output signal.

INPUT/OUTPUT TIMING

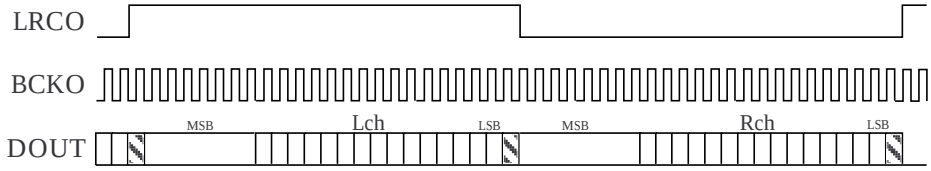
Input Timing



There must be a minimum of 16 BCKI clock cycles to read in a single word of data.

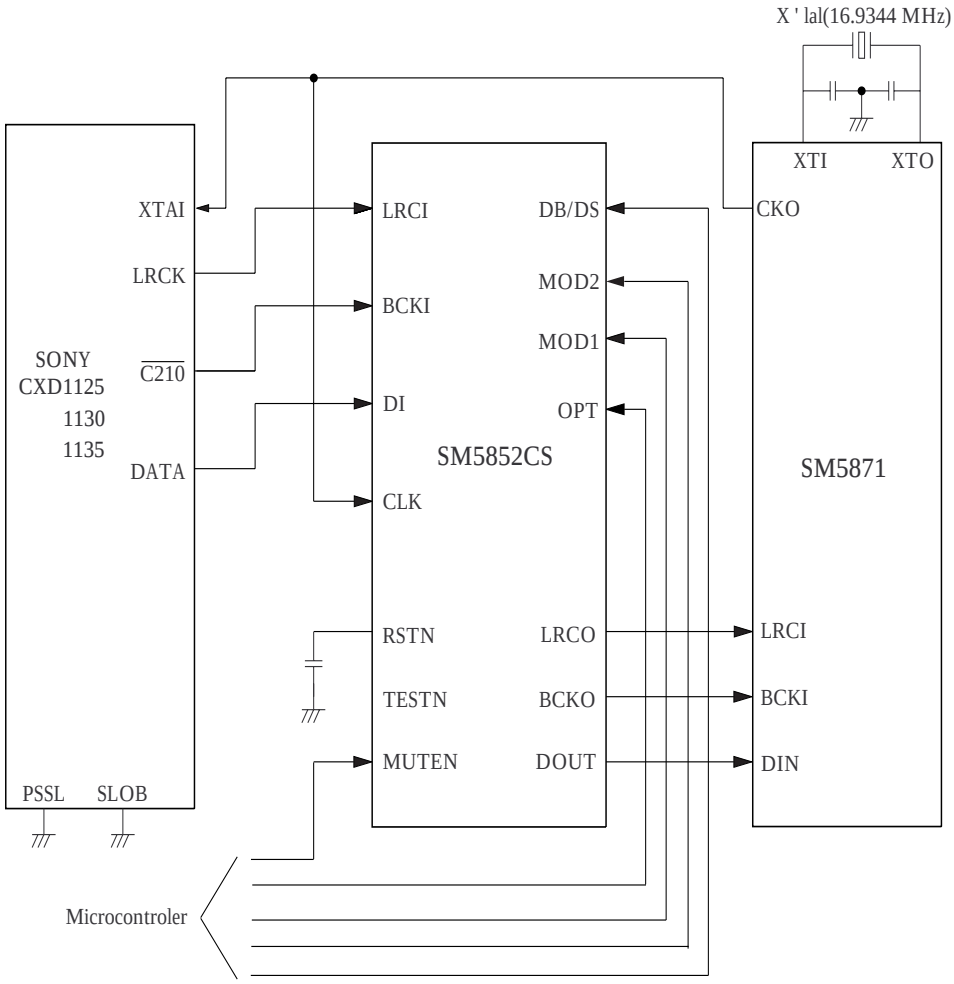
Data on DI is input in sync with the falling edge of BCKI in 16-bit serial, MSB first, 2s complement format.

Output Timing



Shaded areas represent intervals of invalid data.

APPLICATON CIRCUIT



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NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, 2-chome Fukuzumi
Koto-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

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