3A 5V 1MHz Synchronous Buck Converter

Features

- **High Efficiency up to 95%**
- **Adjustable Output Voltage from 0.6V to V_{VIN}**
- **Integrated 75mΩ High Side / 55mΩ Low Side MOSFETs**
- **Low Dropout Operation: 100% Duty Cycle**
- **Mode Selection**
  - APW8805A : Force PWM
- **Stable with Low ESR Ceramic Capacitors**
- **Power-On-Reset Detection on VCC and VIN**
- **Integrated Soft-Start and Soft-Stop**
- **Over-Temperature Protection**
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **High/ Low Side Current Limit**
- **Power Good Indication**
- **Enable/Shutdown Function**
- **Current-Mode Operation with Internal Compensation**
- **Small TDFN3x3-10 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

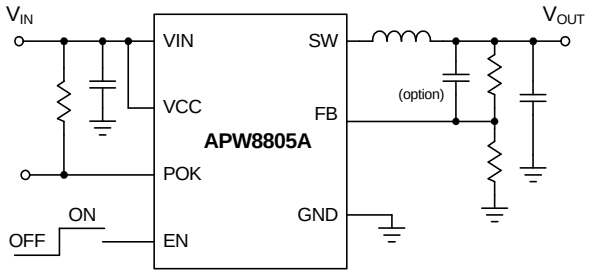
APW8805A is a 3A synchronous buck converter with integrated 75mΩ high side and 55mΩ low side power MOSFETs. The APW8805A, design with a current-mode control scheme, can convert wide input voltage of 2.6V to 6V to the output voltage adjustable from 0.6V to 6V to provide excellent output voltage regulation.

The APW8805A is equipped with force PWM mode opeation.

The APW8805A is also equipped with Power-on-reset, soft-start, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package.

This device, available TDFN3x3-10, provides a very compact system solution external components and PCB area.

Simplified Application Circuit



Applications

- **Notebook Computer & UMPC**
- **LCD Monitor/TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Portable Instrument**

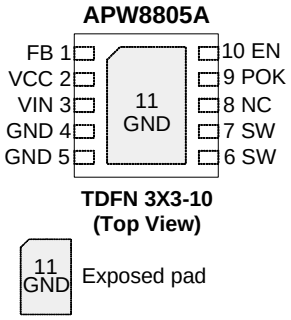
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW8805A □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN3x3-10 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8805A QB : APW 8805A XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VIN}, V_{VCC}	Input Supply Voltage	-0.3 ~ 6.5	V
V_{SW}	SW to GND Voltage	-1 ~V_{VCC}+0.3	V
	POK, FB, EN to GND Voltage	-0.3 ~ 6.5	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TDFN3x3-10	50	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3) TDFN3x3-10	10	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P or TDFN3x3-10 is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the SOP-8P or TDFN3x3-10 package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{VCC}	Control and Driver Supply Voltage	2.6~ 6	V
V_{VIN}	Input Supply Voltage	2~6	V
V_{OUT}	Converter Output Voltage	0.6~6	V
L	Inductance	1~2.2	µH
I_{OUT}	Converter Output Current	0~3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{VCC}=V_{VIN}=5V, V_{OUT}=3.3V, T_A=25°C.

Symbo	Parameter	Test Conditions	APW8805A			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Supply Current	V_{FB}=0.7V	-	460	-	µA
I_{VCC_SDH}	VCC Shutdown Supply Current	EN=GND	-	-	1	µA
POWER-ON-RESET (POR)						
	VCC POR Voltage Threshold	V_{VCC} Rising	2.3	2.4	2.5	V
	VCC POR Hysteresis		-	0.2	-	V
	VIN POR Voltage Threshold		1.5	1.7	1.9	V
	VIN POR Hysteresis		-	0.2	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.8	-	V
		All temperature	-1	-	+1	%
	Output Accuracy	I_{OUT}=10mA~3A, V_{VCC}=2.6~5V	-1.5	-	+1.5	%

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Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{VCC}=V_{VIN}=5V, V_{OUT}=3.3V, T_A=25°C.

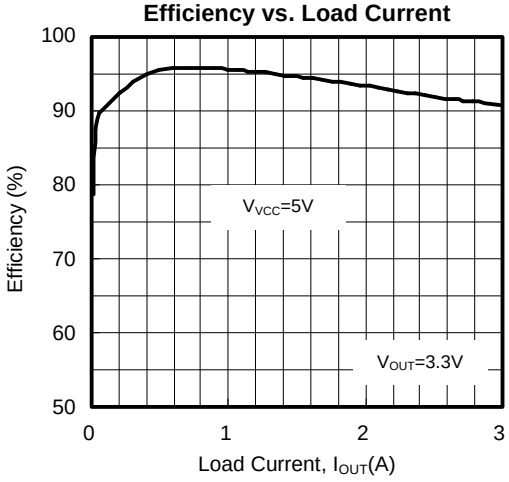
Symbo	Parameter	Test Conditions	APW8805A			Unit
			Min.	Typ.	Max.	
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency		0.85	1	1.15	MHz
	Maximum Converter's Duty	V_{FB}=0.7V	-	100	-	%
	Minimum on Time		-	100	-	ns
POWER MOSFET						
	High Side P-MOSFET Resistance	V_{VCC}=5V, I_{SW}=0.5A, T_A=25°C	-	75	90	mΩ
	Low Side N-MOSFET Resistance	V_{VCC}=5V, I_{SW}=0.5A, T_A=25°C	-	55	75	mΩ
	High/Low Side MOSFET Leakage Current		-	-	10	μA
CURRENT-MODE PWM CONVERTER						
Gm	Error Amplifier Transconductance		-	550	-	μA/V
	Error Amplifier DC Gain	COMP=NC	-	80	-	dB
	Current Sense Transresistance		-	400	-	mΩ
T_D	Dead Time		-	20	-	ns
PROTECTIONS						
I_{LIM}	High Side MOSFET Current-Limit	Peak Current	4	5	6	A
T_{OTP}	Over-Temperature Trip Point		-	160	-	°C
	Over-Temperature Hysteresis		-	50	-	°C
	Over-Voltage Protection Threshold		120	-	135	%V_{REF}
	Under-Voltage Protection Threshold		45	50	55	%V_{REF}
SOFT-START, ENABLE, AND INPUT CURRENTS						
	Soft-Start Time		-	1	-	ms
	EN Enable Threshold		-	-	1.4	V
	EN Shutdown Threshold		0.5	-	-	V
	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%V_{OUT}
		POK Low Hysteresis (POK Goes Low)	-	5	-	%V_{OUT}
		POK in from Higher (POK Goes High)	122	125	128	%V_{OUT}
		POK High Hysteresis (POK Goes Low)	-	5	-	%V_{OUT}
	Power Good Pull Low Resistance		-	100	-	Ω

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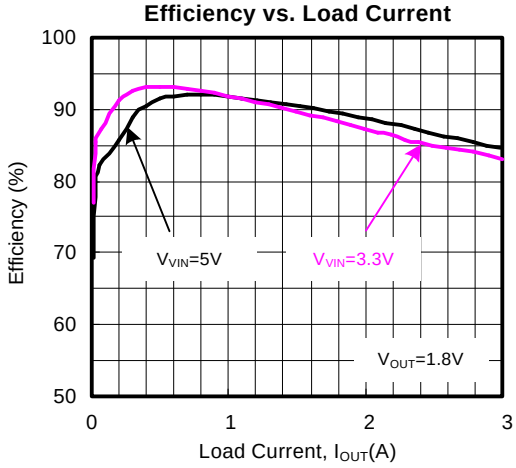
Typical Operating Characteristics

Refer to the "Typical Application Circuit". The test condition is V_{VCC}=V_{VIN}=5V, T_A= 25°C unless otherwise specified.

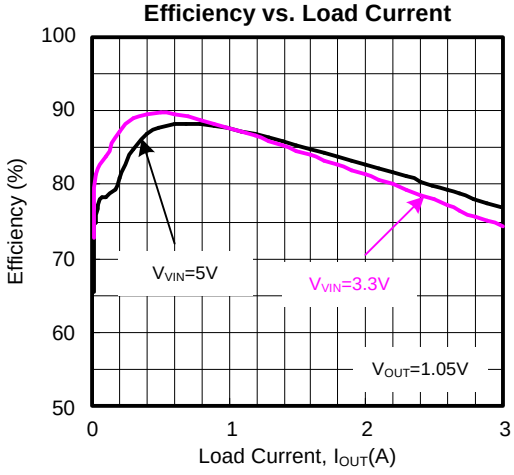
Efficiency vs. Load Current



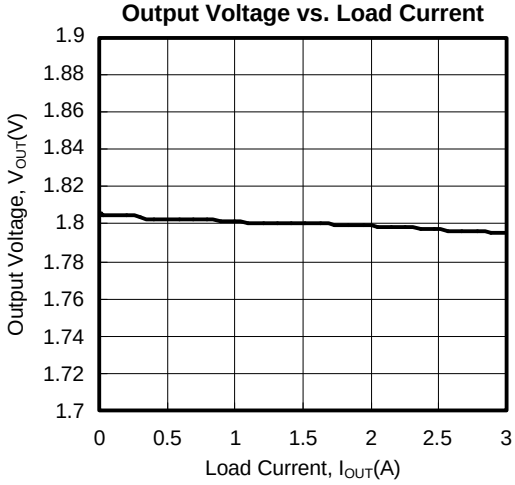
Efficiency vs. Load Current



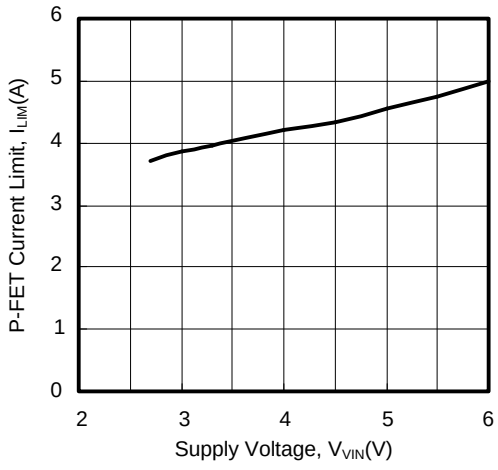
Efficiency vs. Load Current



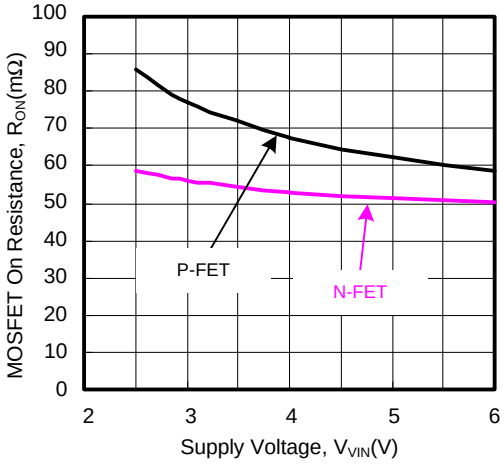
Output Voltage vs. Load Current



Supply Voltage vs. P-FET Current Limit



Supply Voltage vs. MOSFET On Resistance

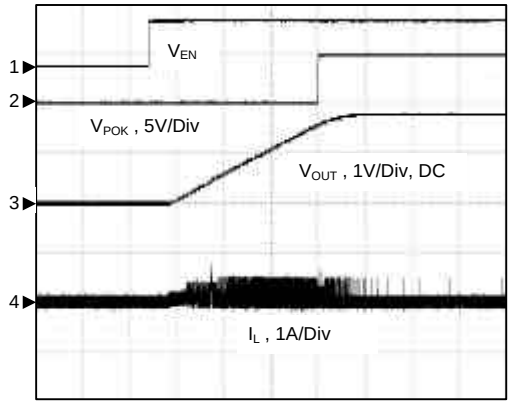


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Operating Waveforms

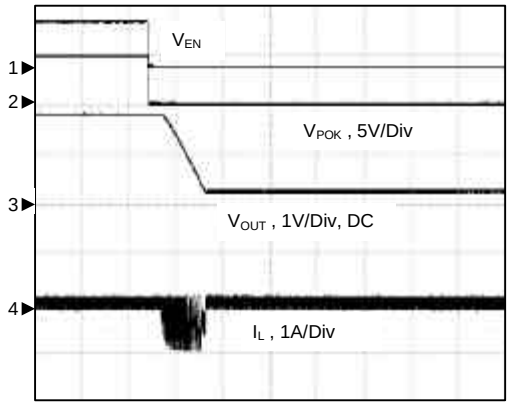
Refer to the typical application circuit. The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Enable without Loading



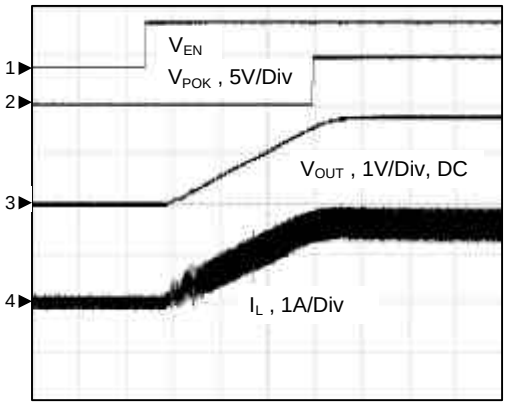
TIME: 200µs/Div

Shutdown



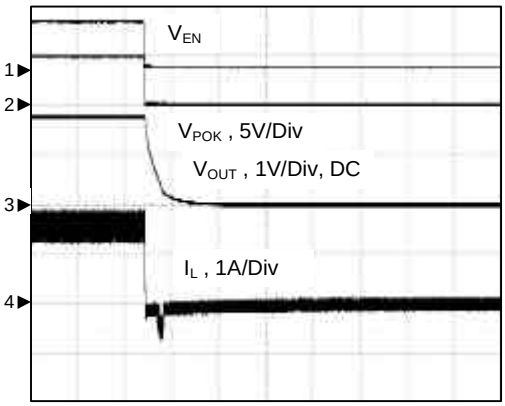
TIME: 200µs/Div

Enable with 1.8A Loading



TIME: 200µs/Div

Shutdown

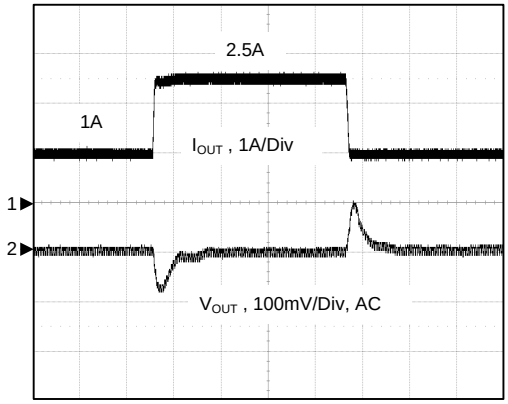


TIME: 200µs/Div

Operating Waveforms

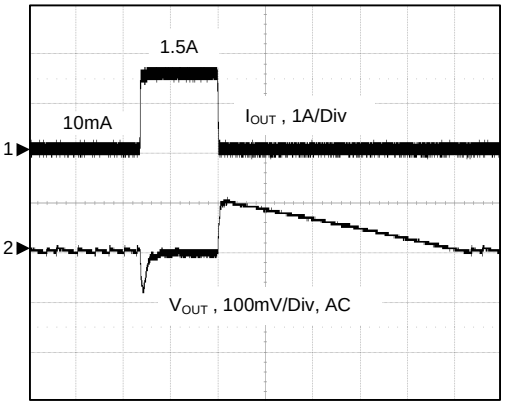
Refer to the typical application circuit. The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Load Transient Response



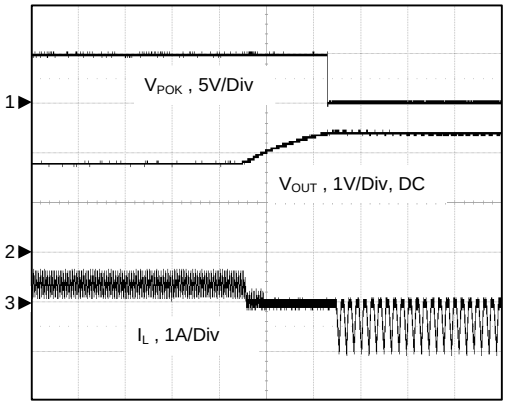
TIME: 20µs/Div

Load Transient Response



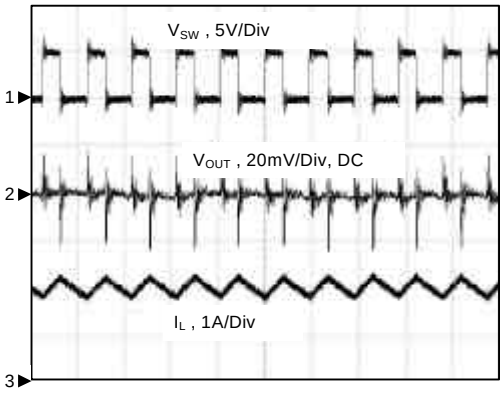
TIME: 50µs/Div

Over Voltage Protection



TIME: 20µs/Div

Normal Operating Waveform



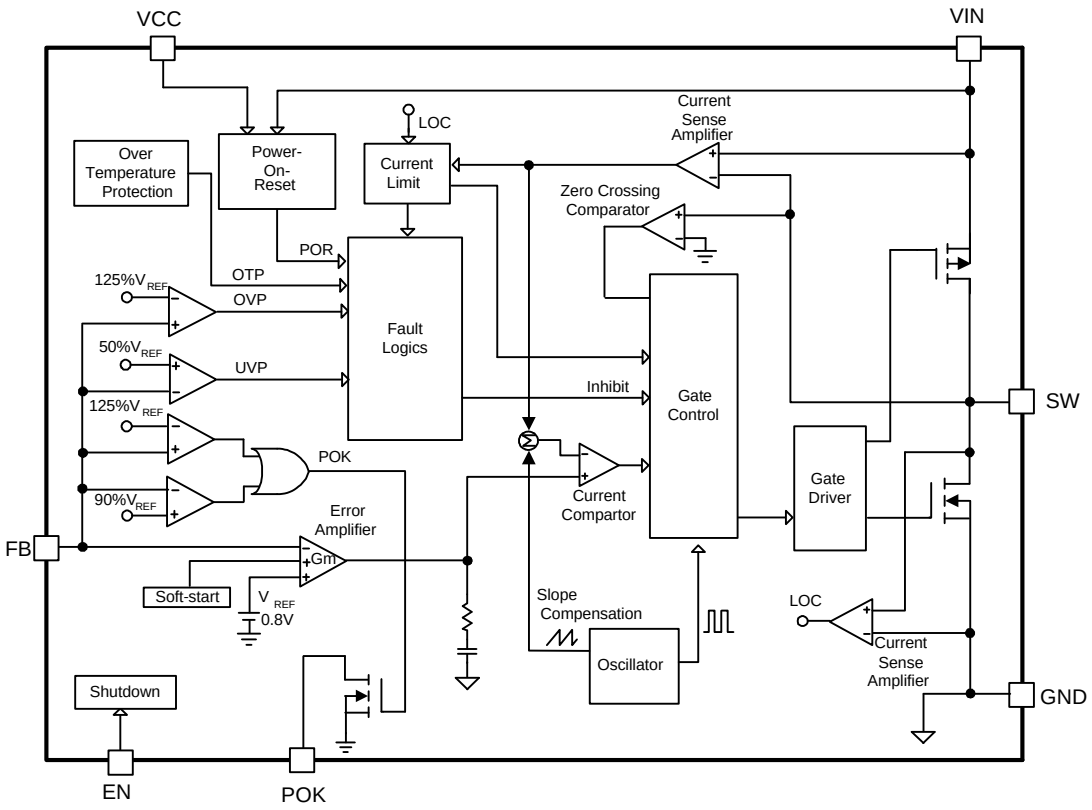
TIME: 1µs/Div

Pin Description

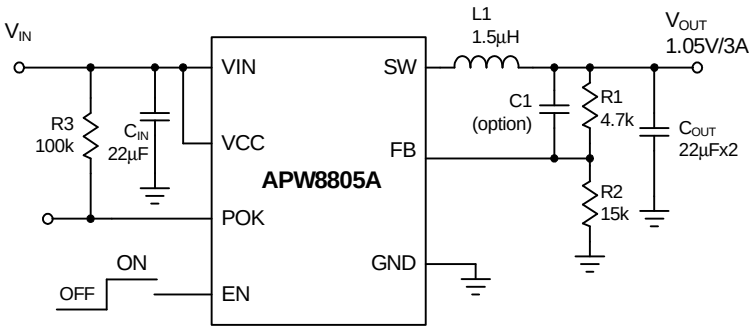
NO.	NAME	FUNCTION
1	FB	Output Feedback Input. The APW8805A senses the feedback voltage via FB and regulates the voltage at 0.8V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
2	VCC	Signal Input. VCC supplies the control circuitry, gate drivers. Connecting a ceramic bypass capacitor from VCC to GND to eliminate switching noise and voltage ripple on the input to the IC.
3	VIN	Power Input. VIN supplies the step-down converter switches. Connecting a ceramic bypass capacitor from VIN to GND to eliminate switching noise and voltage ripple on the input to the IC.
4,5	GND	Ground. Power and signal ground.
6,7	SW	Power Switching Output. SW is the Junction of the high-side and low-side Power MOSFETs to supply power to the output LC filter.
8	NC	No connection.
9	POK	Power Good Output. This pin is open-drain logic output that is pulled to the ground when the output voltage is out of regulation point.
10	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off.
11	GND (Exposed Pad)	Ground and Exposed pad. Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air.

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Block Diagram



Typical Application Circuit



Function Description

VCC and VIN Power-On-Reset (POR)

The APW8805A keeps monitoring the voltage on VCC and VIN pins to prevent wrong logic operations which may occur when VCC or VIN voltage is not high enough for internal control circuitry to operate. The VCC POR rising threshold is 2.4V (typical) with 0.2V hysteresis and VIN POR rising threshold is 1.7V with 0.2V hysteresis.
During start-up, the VCC and VIN voltage must exceed the enable voltage threshold. Then, the IC starts a start-up process and ramps up the output voltage to the voltage target.

Output Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC starts soft-stop function and shuts down converter's output.
The under-voltage threshold is 50% of the nominal output voltage. The under-voltage comparator has a built-in 3µs noise filter to prevent the chips from wrong UVP shutdown being caused by noise. APW8805A will be latched after under-voltage protection.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will trigger soft-stop function and shutdown the converter output.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW8805A. When the junction temperature exceeds T_J=+160°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a start-up process and to regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the APW8805A.

Current-Limit Protection

The APW8805A monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit and over-voltage conditions. Typical high side power MOSFET current limit is 5A.

Soft-Start

The APW8805A has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp connected to one of the positive inputs of the error amplifier, rises up to replace the reference voltage (0.8V) until the voltage ramp reaches the reference voltage. During soft-start without output over-voltage, the APW8805A converter's sinking capability is disabled until the output voltage reaches the voltage target.

Soft-Stop

At the moment of shutdown controlled by EN signal, under-voltage event or over-voltage event, the APW8805A initiates a soft-stop process to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage. During soft-stop, the internal voltage ramp (V_{RAMP}) falls down to replace the reference voltage. Therefore, the output voltage falls down slowly at the light load. After the soft-stop interval elapses, the soft-stop process ends and the IC turns.

Enable and Shutdown

Driving EN to ground places the APW8805A in shutdown. In shutdown mode, the internal N-Channel power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to less than 1µA.

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Function Description (Cont.)

Powr Good Indicator

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, the POK window is from 90% to 125% of the converter reference voltage. When the output voltage has to stay within this window, POK signal will become high. When the output voltage outruns 90% or 125% of the target voltage, POK signal will be pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

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Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

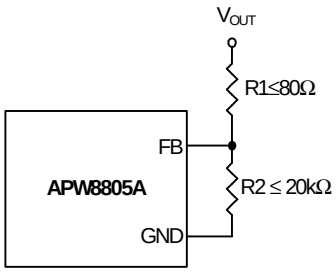
$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in "Typical Application Circuits". A suggestion of maximum value of R2 is 20kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right) = 0.8\cdot\left(1+\frac{R1}{R2}\right)$$

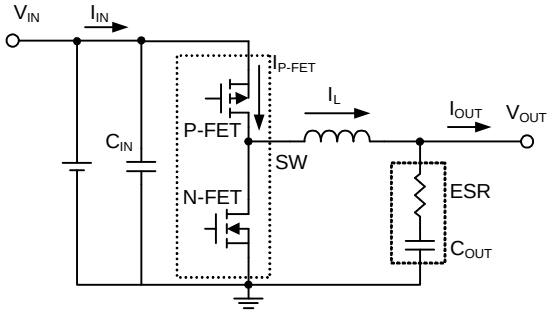


Output Capacitor Selection

The current-mode control scheme of the APW8805A allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

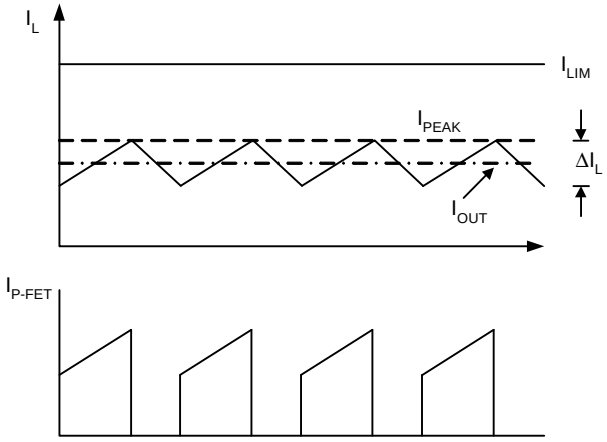
$$\Delta V_{OUT} \cong \frac{V_{OUT}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot L}\cdot\left(ESR+\frac{1}{8\cdot F_{SW}\cdot C_{OUT}}\right)$$

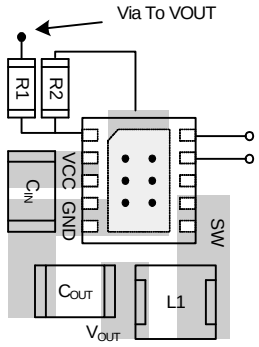
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.



Application Information (Cont.)

Output Capacitor Selection (Cont.)



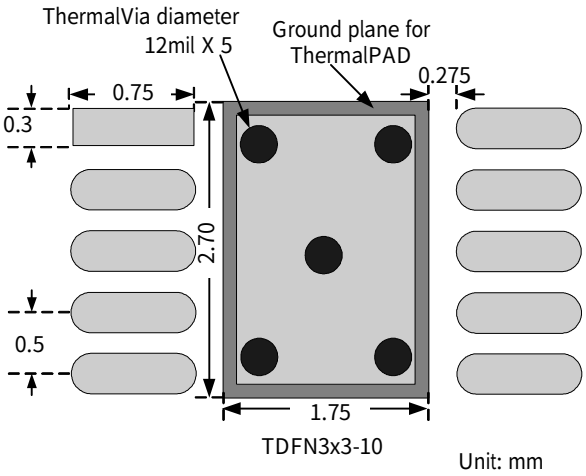


APW8805A Layout Consideration

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

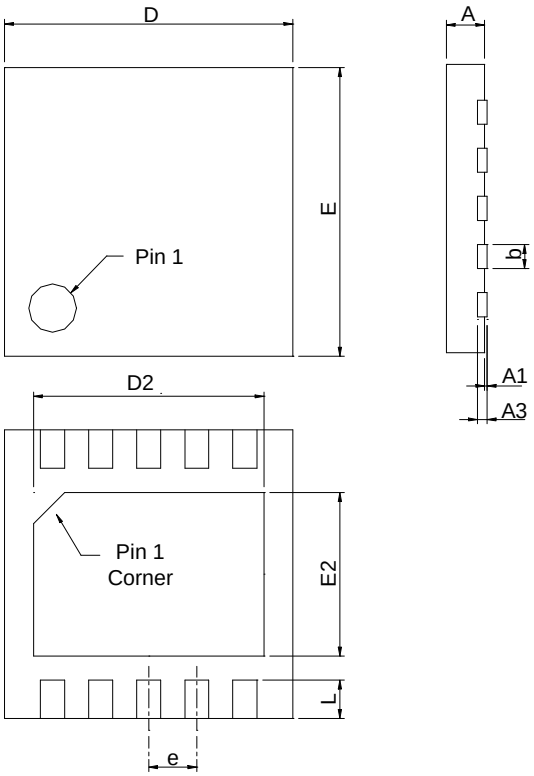
1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to SW and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.



APW8805A Recommended Footprint

Package Information

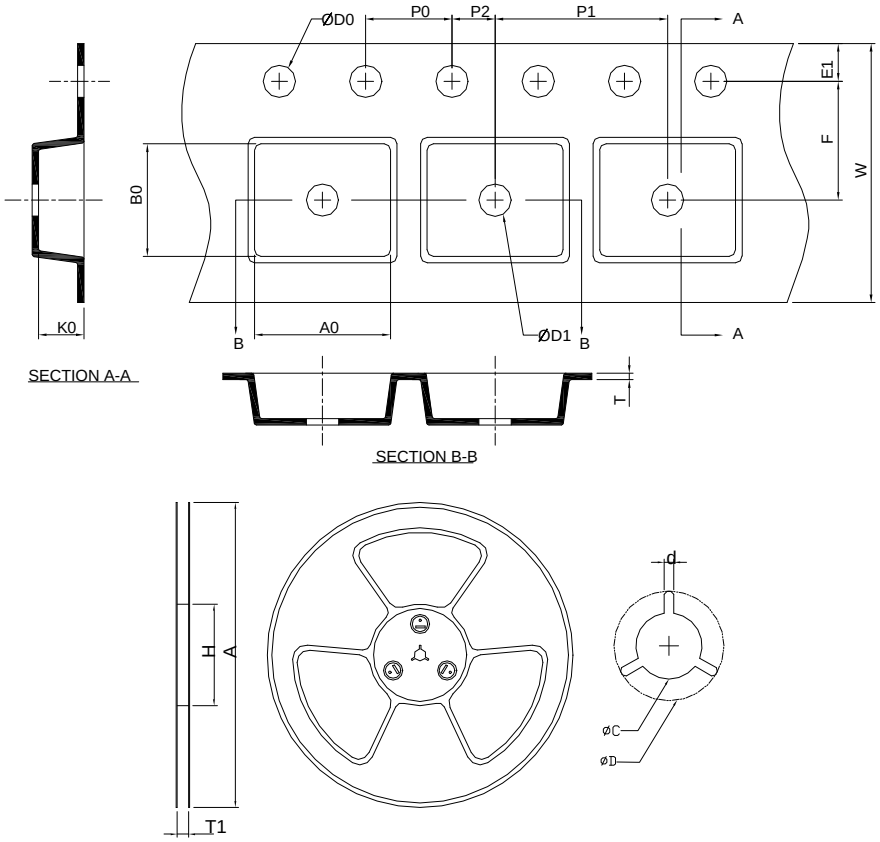
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

(mm)

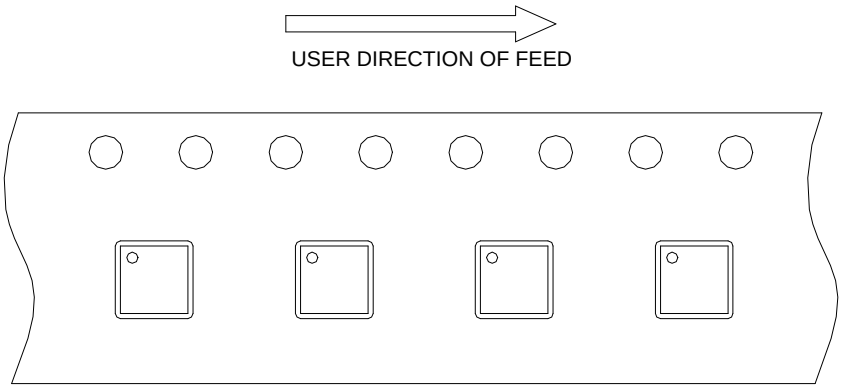
Devices Per Unit

Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

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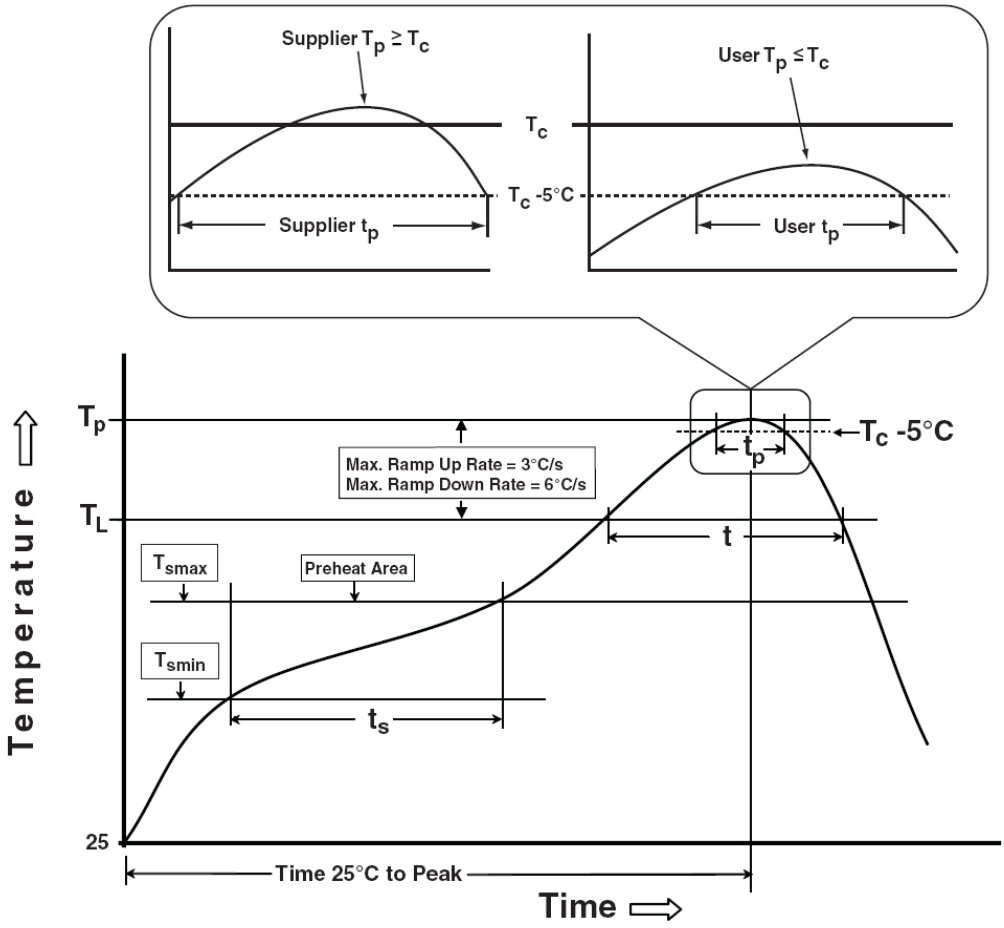
Taping Direction Information

TDFN3x3-10



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Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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