NOT RECOMMENDED FOR NEW DESIGNS

HI-7152

10-Bit High Speed A/D Converter with Track and Hold

January 1998

Features

- **Conversion Time 5μs**
- **Continuous Throughput Rate 200kHz**
- **No Offset or Gain Adjustments Necessary**
- **Internal Track and Hold Amplifier**
- **Analog and Reference Inputs Fully Buffered**
- **μP Compatible Byte Organized Outputs**
- **Low Power Consumption 150mW**
- **Uses a Single 2.5V Reference for ±2.5 V Input Range**

Applications

- **μP Controlled Data Acquisition Systems**
- **DSP**
  - **Avionics**
  - **Sonar**
- **Process Control**
  - **Automotive Transducer Sensing**
  - **Industrial**
- **Robotics**
- **Digital Communications**
- **Image Processing**

Description

The Intersil HI-7152 is a high speed 10-bit A/D converter which uses a Two-Step, Flash algorithm to achieve throughput rates of 200kHz. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

Internal high speed CMOS buffers at both the analog and reference inputs simplify external drive requirements.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor.

Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for interfacing the either 8-bit or 16-bit systems. An out-of-range pin, together with the MSB, can be used to indicate an under-range or over-range condition.

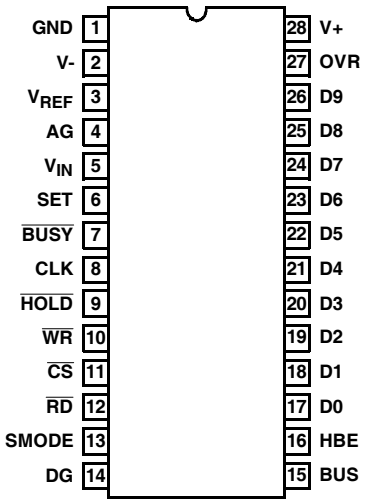
The HI-7152 operates with ±5V supplies. A single +2.5V reference is required to provide a bipolar input range from -2.5V to +2.5V.

Ordering Information

PART NUMBER	LINEARITY (MAX. DLE)	TEMP. RANGE (^{o}C)	PACKAGE
HI3-7152J-5	±1 LSB	0 to 75	28 Ld PDIP
HI3-7152K-5	$\pm^{1}/_{2}$ LSB	0 to 75	28 Ld PDIP
HI3-7152A-9	±1 LSB	0 to 85	28 Ld PDIP
HI3-7152B-9	$\pm^{1}/_{2}$ LSB	0 to 85	28 Ld PDIP
HI1-7152S-2	±1 LSB	-55 to 125	28 Ld CERDIP

Pinout

HI-7152
(PDIP, CERDIP)
TOP VIEW



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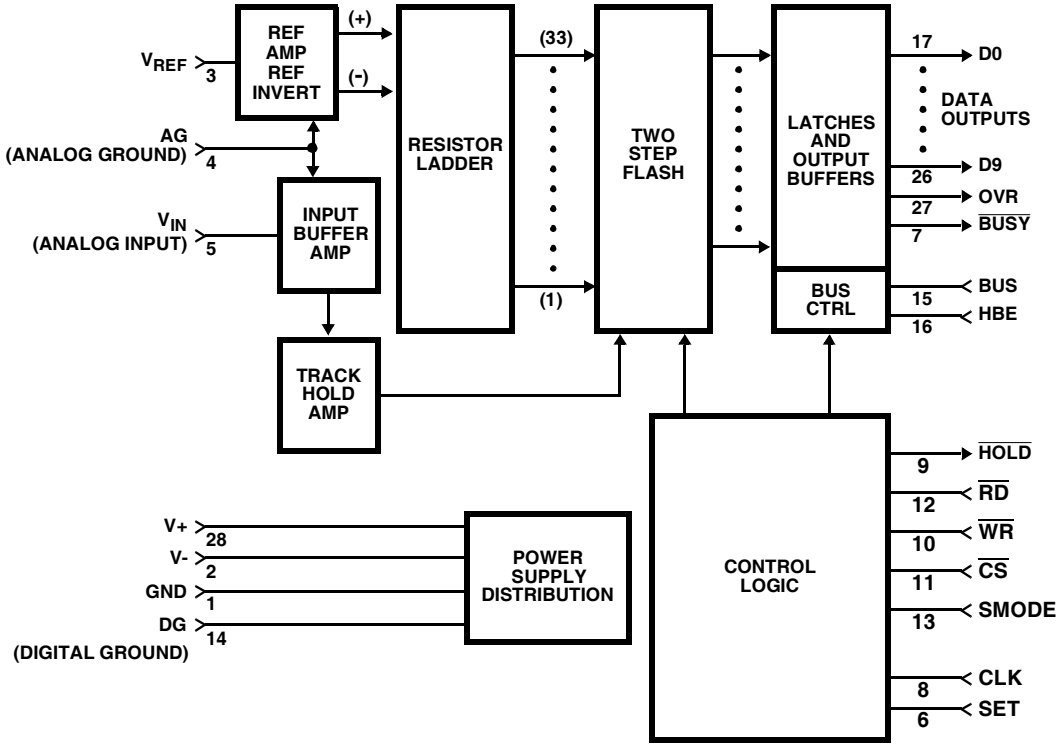
Functional Diagram



Pin Descriptions

PIN	SYMBOL	DESCRIPTION		
1	GND	Ground return for comparators (0V).		
2	V-	Negative supply voltage input (-5V).		
3	V_{REF}	Reference voltage input (+2.50V).		
4	AG	Analog ground reference (0V).		
5	V_{IN}	Analog Input Voltage.		
6	SET	Connect to V+ for proper operation.		
7	$\overline{BUSY}$	Output High-Conversion complete. Output Low - Conversion in progress. Output floats when chip is not selected ($\overline{RD}$ and $\overline{CS}$ both high).		
8	CLK	Clock input.		
9	$\overline{HOLD}$	Indicates start of conversion. Active low.		
10	$\overline{WR}$	Write input. With $\overline{CS}$ low, starts conversion when pulsed low; continuous conversions when kept low.		
11	$\overline{CS}$	Chip select input. Active low.		
12	$\overline{RD}$	Read input. With $\overline{CS}$ low, enables output buffers when pulsed low; outputs updated at end of conversion when kept low.		
13	SMODE	Slow memory mode input. Active high.		
14	DG	Digital ground (0V).		
15	BUS	Bus select input. High = all outputs enabled together D0 - D9, OVR. Low = outputs enabled by HBE.		
16	HBE	Byte select (HBE/LBE) input for 8-bit bus. Input high-High byte select, D8-D9, OVR Input low-low byte select, D0-D7.		
17	D0	Bit 0 (Least significant, LSB).	Output Data Bits (High = True)	Low Byte
18	D1	Bit 1.		
19	D2	Bit 2.		
20	D3	Bit 3.		
21	D4	Bit 4.		
22	D5	Bit 5.		
23	D6	Bit 6.		
24	D7	Bit 7.		
25	D8	Bit 8.		High Byte
26	D9	Bit 9 (Most Significant, MSB).		
27	OVR	Out of Range flag. Valid at end of conversion when output exceeds full scale.		
28	V+	Positive supply voltage input (+5V).		

Absolute Maximum Ratings (Note 1)

Supply Voltage
- V+ to Gnd (DG/AG/GND) . . . . . -0.3V < V+ < +5.7V
- V- to Gnd (DG/AG/GND). . . . . -5.7V < V- < +0.3V

Analog Input Pins . . . . . V- -0.3V < V_{INA} < V+ +0.3V
Digital I/O Pins . . . . . .DG - 0.3V < $V_{I/O}$ < V+ +0.3V
Power Dissipation (Note 2). . . . . <500mW
- Derate above 75°C at -10mW/C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	TBD	N/A
CERDIP Package	TBD	TBD

Maximum Junction Temperature (Hermetic Package or Die) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

Operating Conditions

Temperature Range
- HI3-7152X-5 . . . . . .0°C to 75°C
- HI3-7152X-9 . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input voltages may exceed the supply voltage provided the inputs current is limited to ±1mA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Accuracy Electrical Specifications

V+ = +5V, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz, 50% Duty Cycle, Unless Otherwise Specified (Note 4)

PARAMETER	SYMBOL	(NOTE 3) TEMP. (°C)	J, A GRADE			K, B GRADE			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (Note 5) (With no missing codes)	RES	T_A = 25°C	10	-	-	10	-	-	Bits
		T_{MIN} to T_{MAX}	10	-	-	10	-	-	Bits
Integral Linearity Error	ILE	T_A = 25°C	-	±0.5	±1.0	-	±0.3	±0.5	LSB
		T_{MIN} to T_{MAX}	-	±0.75	±1.0	-	±0.5	±0.75	LSB
Differential Linearity Error	DLE	T_A = 25°C	-	-	±1.0	-	-	±0.5	LSB
		T_{MIN} to T_{MAX}	-	-	±1.0	-	-	±0.75	LSB
Bipolar Offset Error	V_{OS}	T_A = 25°C	-	±1.0	±2.5	-	±0.6	±1.5	LSB
		T_{MIN} to T_{MAX}	-	±1.5	±3.0	-	±1.0	±2.0	LSB
Unadjusted Gain Error	eG+ and eG-	T_A = 25°C	-	±1.0	±2.5	-	±0.6	±1.5	LSB
		T_{MIN} to T_{MAX}	-	±1.5	±3.0	-	±1.0	±2.0	LSB

NOTES:

3. See Ordering Information Table.
4. FSR (Full Scale Range) = 2 X V_{REF} (5V at V_{REF} = 2.5V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.5V).

DC Electrical Specifications

V+ = 5V, V- = -5V, V_{REF} = 2.50V, T_A = 25°C, f_{CLK} = 600kHz, 50% Duty Cycle, Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITION	25°C			0°C to 75°C		-40°C to 85°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
ANALOG INPUT										
Analog Input Range	VIR	V_{IN} = 0V	$-V_{REF}$	-	V_{REF}	$-V_{REF}$	V_{REF}	$-V_{REF}$	V_{REF}	V
Analog INput Bias Current	IBI		-	0.01	100	-	100	-	100	nA
Analog Input Capacitance (Note 6)	CV_{IN}		-	8	20	-	-	-	-	pF
REFERENCE INPUT										
Reference Input Range (Note 7)	VRR	V_{REF} = 2.50V	2.2	2.5	2.6	2.2	2.6	2.2	2.6	V
Reference Input Bias Current	IBR		-	0.01	100	-	100	-	100	nA
Reference Input Capacitance (Note 6)	CV_R		-	7	20	-	-	-	-	pF

DC Electrical Specifications $V+ = 5V$, $V- = -5V$, $V_{REF} = 2.50V$, $T_A = 25^oC$, $f_{CLK} = 600kHz$, 50% Duty Cycle, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITION	25°C MIN	25°C TYP	25°C MAX	0°C to 75°C MIN	0°C to 75°C MAX	-40°C to 85°C MIN	-40°C to 85°C MAX	UNITS
TRACK AND HOLD (See Text)										
Slew Rate	SR	F_{IN} = 100kHz	-	9	-	-	-	-	-	V/µs
Bandwidth	BW		-	1.5	-	-	-	-	-	MHz
Aperture Time			-	30	-	-	-	-	-	ns
Aperture Uncertainty			-	2	-	-	-	-	-	ns
Feedthrough in HOLD			-	-80	-	-	-	-	-	dB
Acquisition Time			-	1.5	-	-	-	-	-	µs
LOGIC INPUTS										
Input High Voltage	V_{IH}	V_{IN} = 0V, V+	2.0	-	-	2.0	-	2.0	-	V
Input Low Voltage	V_{IL}		-	-	0.8	-	0.8	-	0.8	V
Logic Input Current	I_{IL}		-	0.05	1	-	1	-	1	µA
Input Capacitance (Note 6)	C_{IN}		-	5	17	-	-	-	-	pF
LOGIC OUTPUTS										
Output High Voltage	V_{OH}	I_{OH} = -200µA	2.4	-	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA	-	-	0.4	-	0.4	-	0.4	V
Output Leakage Current	I_{OL}	$\overline{RD}$ = V+, V_{OUT} = V+	-	0.04	1	-	10	-	10	µA
		$\overline{RD}$ = V+, V_{OUT} = 0V	-1	-0.01	-	-10	-	-10	-	µA
Output Capacitance (Note 6)	C_{OUT}	High-Z State	-	7	15	-	-	-	-	pF
POWER SUPPLY VOLTAGE RANGE										
(Note 8)	V+	Function Operation Only	4.5	5.0	5.5	4.5	5.5	4.5	5.5	V
(Note 8)	V-		-4.5	-5.0	-5.5	-4.5	-5.5	-4.5	-5.5	V
POWER SUPPLY REJECTION										
V+, V- Gain Coefficient	eGVS	V+ = 5V, V- = -4.75V, -5.25V	-	±0.1	±0.05	-	±0.6	-	±0.6	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	±0.1	±0.5	-	±0.6	-	±0.6	LSB
V+, V- Offset Coefficient	VOSVS	V+ = 5V, V- = -4.75V, -5.25V	-	±0.1	±0.5	-	±0.6	-	±0.6	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	±0.1	±0.5	-	±0.6	-	±0.6	LSB
SUPPLY CURRENTS										
V+ Supply Current	I+	V+ = 5V ±10% V- = -5V ±10% V_{IN} = 0V, Digital Outputs are Unloaded	-	20	30	-	30	-	30	mA
V- Supply Current	I-		-	-10	-15	-	-15	-	-15	mA
GND Current	IGND		-	-8	-	-	-	-	-	mA
DG Current	IDG		-	-2	-	-	-	-	-	mA
AG Current	IAG		-	0.02	-	-	-	-	-	µA

NOTES:

5. FSR (Full Scale Range) = 2 X V_{REF} (5V at V_{REF} = 2.5V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.5V).
6. Parameter not tested. Parameter guaranteed by design, simulation, or characterization.
7. Only V_{OS} and GAIN ERROR functionality tested at 2.2V and 2.6V.
8. Guaranteed by functionality test.

AC Electrical Specifications V+ = 5V ±10%, V- = -5V ±10%, V_{REF} = 2.5V, T_A = 25°C, f_{CLK} = 600kHz, 50% Duty Cycle, C_L = 100pF (including stray for D0 - D9, OVR, $\overline{HOLD}$, $\overline{BUSY}$), Unless Otherwise Specified (Note 12)

PARAMETER	SYMBOL	NOTES	25°C			0°C to 75°C		-40°C to 85°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Continuous Conversion Time	t_{SPS}	10	-	-	3tck	-	3tck	-	3tck	µs
		10	60	-	5	60	5	60	10	µs
Slow Memory Mode Conversion Time	t_{CONV}	6, 9	-	-	4tck +0.9	-	4tck +0.9	-	4tck +0.9	µs
Continuous Throughput	t_{CYC}	10	-	-	$f_{CLK}/3$	-	$f_{CLK}/3$	-	$f_{CLK}/3$	sps
CLOCK Period	t_{CK}	-	-	$1/f_{CLK}$	-	-	-	-	-	
Clock Input Duty Cycle	D	6	45	50	55	45	55	45	55	%
CLOCK to $\overline{HOLD}$ Rise Delay	t_{CKHR}	6	150	290	500	140	525	120	525	ns
$\overline{WR}$ Pulse Width	t_{WRL}	6, 9, 11	200	113	tck/2	225	tck/2	225	tck/2	ns
$\overline{WR}$ to $\overline{HOLD}$ Delay	t_{HOLD}	6, 9	-	80	170	-	200	-	200	ns
$\overline{Busy}$ to Data	t_{BD}	6, 9	-	40	200	-	230	-	230	ns
$\overline{WR}$ to $\overline{RD}$ Active	t_{WRD}	6, 9	100	-	-	100	-	100	-	ns
CLOCK to $\overline{HOLD}$ Fall Delay	t_{CKHF}	6, 10	50	125	250	40	275	25	275	ns
$\overline{HOLD}$ to DATA Change	t_{DATA}	6, 10	100	200	400	90	550	70	550	ns
$\overline{RD}$ LO to Active	t_{RD}	6, 14	-	75	150	-	190	-	190	ns
$\overline{RD}$ HI to Inactive	t_{RX}	6, 15	-	25	60	-	80	-	80	ns
HBE to DATA	t_{AD}	6	-	70	150	-	165	-	165	ns
$\overline{CS}$ to DATA	t_{CD}	6	-	95	180	-	210	-	210	ns
$\overline{RD}$ to $\overline{BUSY}$	t_{BUSY}	6	-	35	200	-	200	-	200	ns
Rise Time	t_r	6, 13	-	50	100	-	125	-	125	ns
Fall Time	t_f	6, 13	-	45	100	-	120	-	120	ns

NOTES:

9. Slow memory mode timing.
10. Fast memory or DMA mode of operation, except the first conversion which is equal to t_{CONV}.
11. Maximum specification to prevent multiple triggering with $\overline{WR}$.
12. All input drive signals are specified with $t_r = t_f \leq 20ns$ and shall swing from V_{IL} -0.4V to V_{IH} +0.4V for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except t_{RD} and t_{RX}).
13. t_r and t_f load is C_L = 100pF (including stray capacitance) to DG and is measured from the 10 - 90% point.
14. t_{RD} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with R_L = 2.5kΩ and C_L = 100pF (including stray) to DG. High-Z to V_{OL} is measured with R_L = 2.5kΩ to V+ and C_L = 100pF (including stray) to DG.
15. t_{RX} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. V_{OH} to High-Z is measured with R_L = 2.5kΩ and C_L = 10pF (including stray) to DG. V_{OL} to High-Z is measured with R_L = 2.5kΩ to V+ and C_L = 10pF (including stray) to DG.

Timing Diagrams

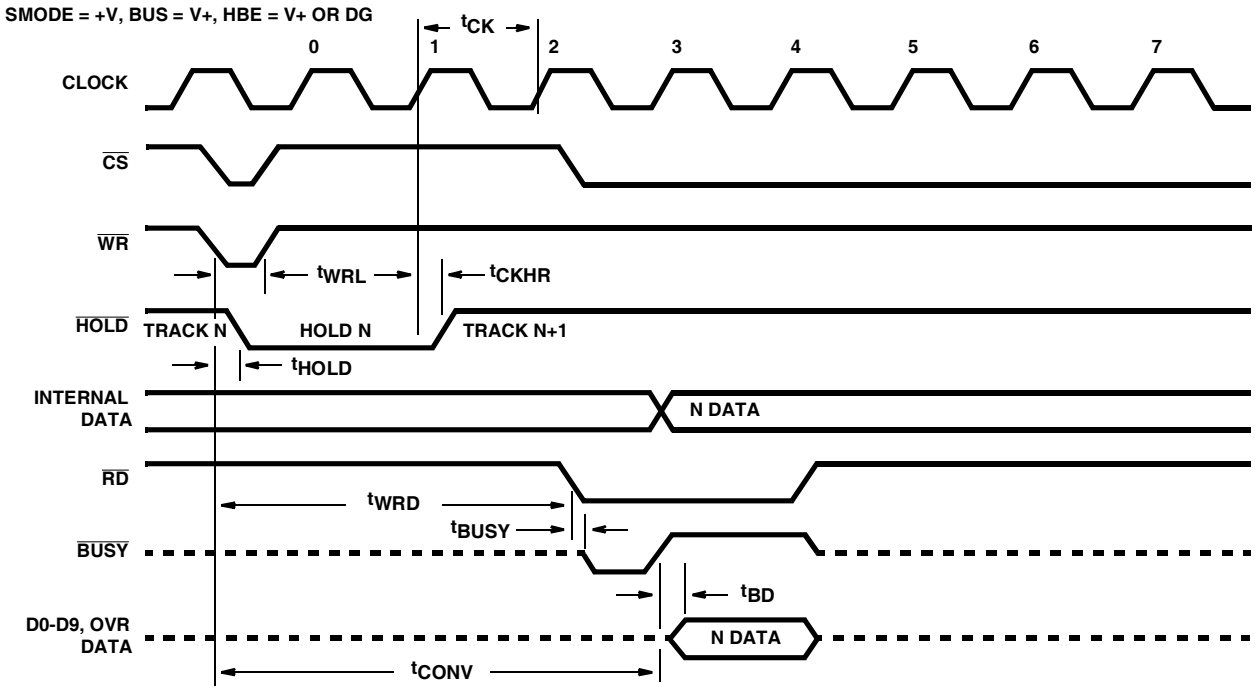


FIGURE 1A. SLOW MEMORY MODE (16-BIT DATA BUS)

Timing Diagrams (Continued)

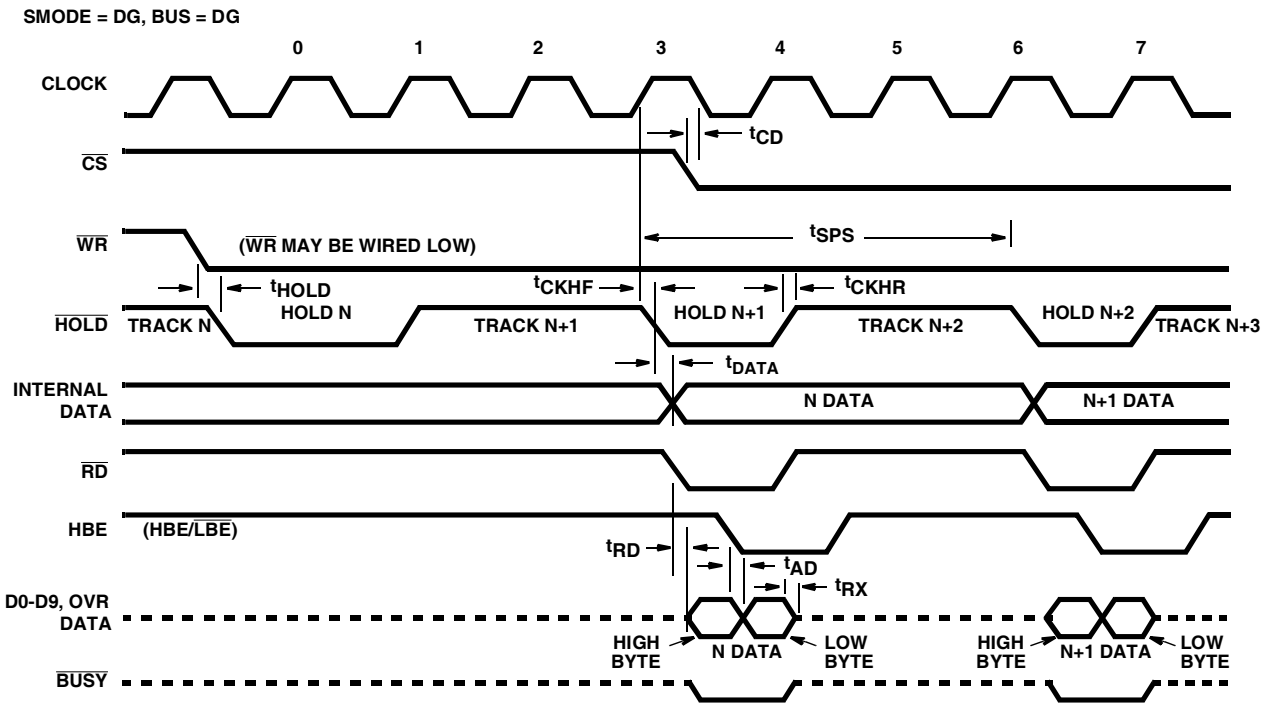


FIGURE 1B. FAST MEMORY MODE (8-BIT DATA BUS)

SMODE = +V: RD, WR, AND CS = DG, BUS = V+, HBE = V+ OR DG

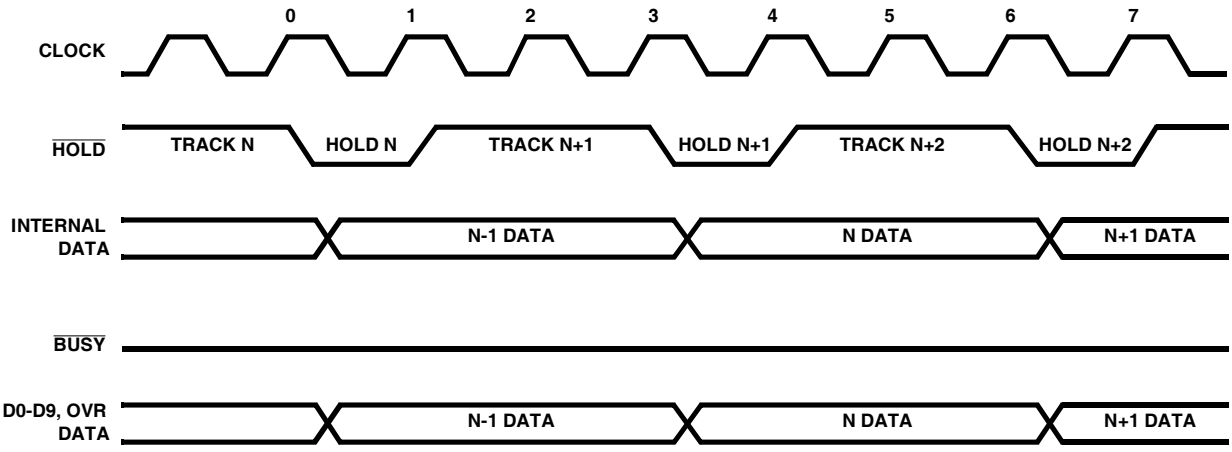
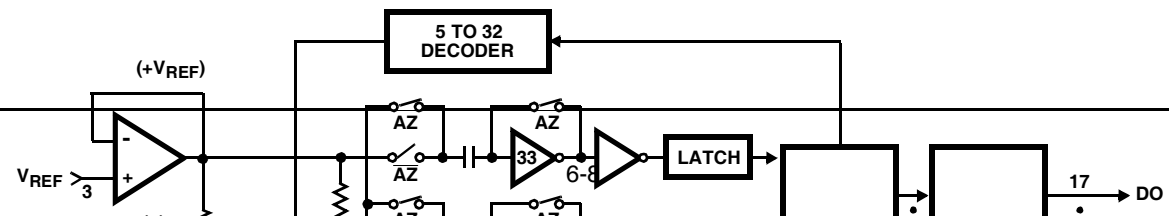


FIGURE 1C. DMA MODE (16-BIT DATA BUS)

Detailed Block Diagram



Detailed Description

The HI-7152 is a high speed 10-bit A/D converter which achieves throughput rates of 200kHz by use of a Two Step Flash algorithm. A pipelined operation has been achieved through the use of switched capacitor techniques which allow the device to sample a new input voltage while a conversion is taking place. The HI-7152 requires a single reference input of +2.5V, which is internally inverted to -2.5V, thereby allowing an input range of -2.5V to +2.5V. 10 bits including sign are two's complement coded. The analog and reference inputs are internally buffered by high speed CMOS buffers, which greatly simplifies the external analog drive requirements for the device.

A/D Section

The HI-7152 uses a conversion algorithm which is generally called a "Two Step Flash" algorithm. This algorithm enables very fast conversion rates without the penalty of high power dissipation or high cost. A detailed functional diagram is presented in Figure 2.

The input voltage is first converted into a 5-bit result (plus Out of Range information) by the flash converter. This flash converter consists of an array of 33 auto-zeroed comparators which perform a comparison between the input voltage and subdivisions of the reference voltage. These subdivisions of the reference voltage are formed by forcing the reference voltage and its negative on the two ends of a string of 32 resistors.

The reference input to the HI-7152 is buffered by a high speed CMOS amplifier which is used to drive one end of the resistor string. Another high speed amplifier configured in the inverting unity gain mode inverts the reference voltage with respect to analog ground and forces in onto the other end of the resistor string. Both reference amplifiers are offset trimmed at the factory in order to increase the accuracy of the HI-7152 and to simplify its usage.

The 5-bit result of the first flash conversion is latched into the upper five bits of double buffered latches. It is also converted back into an analog signal by choosing the ladder voltage which is closest to but less than the input voltage. The selected voltage (V_{TAP}) is then subtracted from the input voltage. This residue is amplified by a factor of 32 and referenced to the negative reference voltage ($V_{SCA} = (V_{IN} - V_{TAP}) \times 32 + V_{REF}$ -). This subtraction and amplification operation is performed by a Switched Capacitor Amplifier (SCA). The output of the SCA falls between the positive and negative reference voltages and can therefore be digitized by the original 5-bit flash converter (second flash conversion).

The 5-bit result of the second flash conversion is latched into the lower five bits of double buffered latches. At the end of a conversion, 10 bits of data plus an Out of Range bit are latched into the second level of latches and can then be put on the digital output pins.

The conversion takes place in three clock cycles and is illustrated in Figure 3. When the conversion begins, the track and hold goes into its hold mode for 1 clock cycle. During the first half clock cycle the comparator array is in its auto-zero mode and it samples the input voltage. During the second half clock cycle, the comparators make a comparison between the input voltage and the ladder voltages. At the beginning of the third half clock cycle, the first most significant 5-bit result becomes available. During the first clock cycle, the SCA was sampling the input voltage. After the first flash result becomes available and a ladder tap voltage has been selected the SCA amplifies the residue between the input and ladder tap voltages. During the next three half clock cycles, while the SCA output is settling to its required accuracy, the comparators go into their auto-zero mode and sample this voltage. During the sixth half clock cycle, the comparators perform another comparison whose 5-bit result becomes available on the next clock edge.

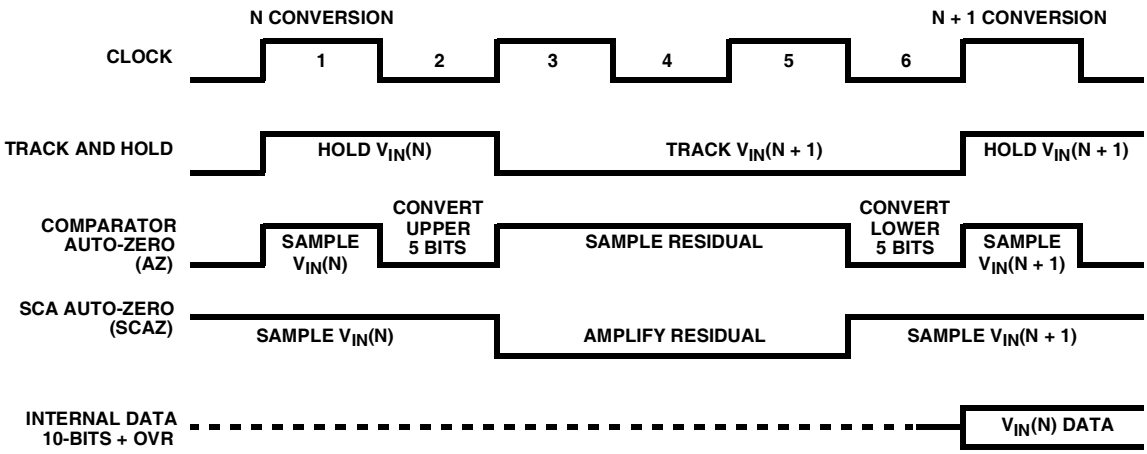


FIGURE 3. INTERNAL ADC TIMING DIAGRAM

TABLE 1. A/D OUTPUT CODE TABLE

ANALOG INPUT (NOTE)		**OUTPUT DATA**										
LSB = 2 (V_{REF}) / 1024	**V_{REF} = 2.500V**	**OVR**	**MSB 9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB 0**
≥ +V_{REF}	2.500V to V+ (+OVR)	1	0	0	0	0	0	0	0	0	0	0
+V_{REF} - 1 LSB	2.49512V (+Full Scale)	0	0	1	1	1	1	1	1	1	1	1
+1 LSB	0.00488V	0	0	0	0	0	0	0	0	0	0	1
0	0.000V	0	0	0	0	0	0	0	0	0	0	0
-1 LSB	-0.00488V	0	1	1	1	1	1	1	1	1	1	1
-V_{REF}	-2.500V (-Full Scale)	0	1	0	0	0	0	0	0	0	0	0
≤ -V_{REF} - 1 LSB	-2.50488V to V- (-OVR)	1	1	0	0	0	0	0	0	0	0	0

NOTE: The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Track and Hold Analog Input

A Track and Hold amplifier has been fully integrated on the front end of the A/D converter. Because of the sampling nature of this A/D converter, the input is required to stay constant only during the first clock cycle. Therefore, the Track and Hold (T/H) amplifier "holds" the input voltage only during the first clock cycle and it acquires the input voltage for the next conversion during the remaining two clock cycles. The high input impedance of the T/H input amplifier simplifies analog interfacing. Input signals up to ±V_{REF} can be directly connected to the A/D without buffering. The A/D output code table is shown in Table 1.

The timing signals for the Track and Hold amplifier are generated internally, and are also provided externally ($\overline{HOLD}$) for synchronization purposes. The T/H amplifier consists of two high speed CMOS amplifiers and an internal hold capacitor. Its typical slew rate and bandwidth are 9V/µs and 1.5MHz respectively. It is configured to give a very small hold pedestal without the use of an external hold capacitor. The hold pedestal is typically less than 100µV.

Acquisition of the analog input signal is the time required by the T/H for its output to reach its final value within a specified error band. This time is a function of the logic delay time, op amp slewing time, and settling time. The T/H is in the track mode for 2 clock cycles (3.3µs at CLK = 600kHz) but the output typically settles to within $^1/_4$ LSB in 1.5µs.

Aperture delay time is the time required for the T/H switch to open following the internal hold command. This is the delay with respect to falling edge of $\overline{WR}$ and the internal hold command. It is equal to T_{HOLD} (type) - 50ns (Typ) which is typically 30ns.

Aperture uncertainty (jitter) is a range of variation in the aperture time. The greater the aperture time the larger the uncertainty in the analog voltage being converted. If the aperture time is nulled out by advancing the hold command ($\overline{WR}$) or the signal is repetitively sampled, aperture uncertainty becomes the major source of time error. The aperture uncertainty for the T/H is typically 2ns which sets the maximum input bandwidth to 77.7kHz for 1 LSB resolution.

$f_{MAX} = 1/(2\pi \times 2^n \times ta)$

where n = resolution in bits

ta = aperture uncertainty

All of the internal amplifiers are offset trimmed during manufacturing to give improved accuracy and to minimize the number of external components. If necessary, offset error can be adjusted either at an external interface buffer or by using digital post correction.

Reference Input

The reference input to the HI-7152 is buffered by a high speed CMOS amplifier. The reference input range is 2.2V to 2.6V.

Power Requirements

Power to the chip should be applied in the following order: V-, V+, and V_{REF}. In applications where V+ is supplied prior to V-, the positive supply current will be approximately 2 times its nominal value until V- is applied (this is not a latchup condition).

Initialization

In fast memory and DMA modes (after proper power, V_{REF}, and clock) up to 6 clock cycles are required for circuit initialization. After circuit initialization, valid data will be available in 3 clock cycles.

Microprocessor Interface

The HI-7152 can be interfaced to microprocessors through the use of standard Write, Read, Chip Select, and HBE control pins. The digital outputs are two's complement coded, three-state gated, and byte organized for bus interface with 8-bit and 16-bit systems. The digital outputs (D0 - D9, OVR, and $\overline{BUSY}$) may be accessed under control of BUS, byte enable input HBE, chip select, and read inputs for a simple parallel bus interface. The microprocessor can read the current data in the output latches in typically 75ns/byte (trd). An over range pin (OVR) together with the MSB (D9) pin set to either a logic 0 or 1 will indicate a positive or negative over-range condition respectively. All digital output buffers are capable of driving one TTL load.

The HI-7152 can be interfaced to a microprocessor using one of three modes: slow memory, fast memory, and DMA mode.

Slow Memory Mode

In slow memory mode, the conversion will be initiated by the microprocessor by selecting the chip ($\overline{CS}$) and pulsing $\overline{WR}$ low. This mode is selected by hardwiring the SMODE pin to V+. This mode is intended for use with microprocessors (such as the 8086) which can be forced into a WAIT state. For example, in configuration where the $\overline{BUSY}$ output is tied to the 8086 READY input, an attempt to read the data before the conversion is complete will force the processor into a WAIT state until $\overline{BUSY}$ goes high, at which time the data at the output is valid. This resembles a 5μs access time RAM. It allows the processor to initiate a conversion, WAIT, and READ data with a single READ instruction. When the 8-bit bus operation is selected, high and low byte data may be accessed in either order. An I/O truth table is presented in Table 2 for the slow memory mode of operation.

TABLE 2. SLOW MEMORY MODE I/O TRUTH TABLE (SMODE = V+)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	FUNCTION
0	0	X	X	X	Initiates a Conversion.
1	X	X	X	X	Disables All Chip Commands.
0	X	0	1	X	D0 - D9 and OVR Enabled.
0	X	0	0	0	Low Byte Enabled: D0 - D7.
0	X	0	0	1	High Byte Enabled: D8 - D9, OVR.
X	X	1	X	X	Disables all Outputs (High Impedance).

NOTE: X = Don't Care

Fast Memory Mode

The fast memory mode of operation is selected by tying the SMODE and $\overline{WR}$ pins to DG. In this mode, the chip performs continuous conversions and only $\overline{CS}$ and $\overline{RD}$ are required to read the data. Whenever the SMODE pin is low, $\overline{WR}$ is independent of $\overline{CS}$ in starting a conversion cycle. During the first conversion cycle, $\overline{HOLD}$ follows $\overline{WR}$ going low.

Data can be read a byte at a time or all 11 bits at once. The internal logic disables the output latches from being updated during a read after the high byte data is accessed. It will continue to be disabled until after the low byte data is accessed. THEREFORE, WHEN 8-BIT BUS OPERATION IS SELECTED, THE DATA MUST BE ACCESSED HIGH BYTE FIRST, LOW BYTE NEXT. If the low byte is accessed first followed by high byte, the results from the next conversion cycle will be lost because the updating of the output latch is disabled. $\overline{BUSY}$ is continuously low when accessed with a read command in this mode. An I/O truth table is presented in Table 3 for the fast memory mode of operation.

The data can be defined in time by monitoring the $\overline{HOLD}$ pin. The conversion data can be read after $\overline{HOLD}$ has gone low.

TABLE 3. FAST MEMORY MODE I/O TRUTH TABLE (SMODE = DG)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	FUNCTION
X	0	X	X	X	Continuous Conversion, $\overline{WR}$ may be Tied to DG.
1	X	X	X	X	Disables Only the $\overline{RD}$ Command.
0	X	0	1	X	D0 - D9 and OVR Enabled.
0	X	0	0	1	High Byte Enabled: D8 - D9, OVR (Enable 1st).
0	X	0	0	0	Low Byte Enabled: D0 - D7 (Must Enable 2nd).
X	X	1	X	X	Disables All Outputs (High Impedance).

NOTE: X = Don't Care

DMA Mode

This mode is a complete hardware mode where the HI-7152 continuously converts. The user implements hardware to store the results in memory, bypassing the microprocessor. This mode is recognized by the chip when SMODE is hardwired to V+ and $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ are hardwired to DG. When 8-bit bus operation is selected, high and low byte data may be accessed in either order. $\overline{BUSY}$ is continuously low when accessed with a read command in this mode. An I/O truth table is presented in Table 4 for the DMA mode of operation.

TABLE 4. DMA MODE I/O TRUTH TABLE (SMODE = V+, $\overline{CS}$ = $\overline{WR}$, $\overline{RD}$ = DG)

BUS	HBE	FUNCTION
1	X	D0 - D9 and OVR Enabled.
0	0	Low Byte Enabled: D0 - D7.
0	1	High Byte Enabled: D8 - D9, OVR.

NOTE: X = Don't Care

Optimizing System Performance

The HI-7152 has three ground pins (AG, DG, GND) for improved system accuracy. Proper grounding and bypassing is illustrated in Figure 4. The AG pin is a ground pin that does not carry any current and is used internally as a reference ground. The reference input and analog input should be referenced to the analog ground (AG) pin. The digital inputs and outputs should be referenced to the digital ground (DG) pin. The GND pin is a return point for the supply current of the comparator array. The comparator array is designed such that this current is approximately constant at all times and does not vary with input voltage. By virtue of the switched capacitor nature of the comparators, it is necessary to hold GND firmly at zero volts at all times. Therefore, the system ground star connection should be located as close to this pin as possible.

As in any analog system, good supply bypassing is necessary in order to achieve optimum system performance (minimize conversion errors). The power supplies should be bypassed with at least a 20μF tantalum and 0.1μF ceramic capacitors to GND. The reference input should be bypassed with a 0.1μF ceramic capacitor to AG. The capacitor leads should be as short as possible.

The pins on the HI-7152 are arranged such that the analog pins are well isolated from the digital pins. In spite of this arrangement, there is always pin to pin coupling. Therefore the analog inputs to the device should not be driven from very high output impedance sources. PC board layout should screen the analog and reference inputs with AG. Using a soldier mask is good practice and helps reduce leakage due to moisture contamination on the PC board.

Applications

Typical applications are illustrated in Figure 5 through 7 for the slow memory, fast memory, and DMA modes of operation. The output data is configured for 16-bit bus operation of these three applications. By tying BUS and DG and connecting the HBE input to the system address decoder, the output data can be configured for 8-bit bus systems.

Figure 8 illustrates an application where the HI-7152 is used with an analog multiplexer to form a multi-channel data acquisition system. Either slow memory or fast memory modes of operation can be selected. Fast memory mode should be selected for maximum throughput. Multiplexer channel acquisition should occur approximately 500ns after $\overline{HOLD}$ goes high. This allows 2 clocks minus 0.5μs for the input to settle. With a 600kHz clock the input has up to 2.8μs to settle.

An intelligent system which performs a scale factor adjustment under software control with the addition of a programmable gain block between the multiplexer and HI-7151 is illustrated in Figure 9. The microprocessor first performs a conversion and then checks the over-range status (OVR) bit. If the OVR bit is high, the microprocessor addresses a precision gain circuit for scale factor adjustment and initiates another conversion. The microprocessor must keep track of the selected scale factor.

The accuracy of the programmable gain amplifier should be better than 0.05%. For optimum system performance, op amp frequency response, settling time, and charge injection of the analog switch must be considered.

Figure 10 illustrates the HI-7152 interfaced to FIFO memories for use in DMA applications.

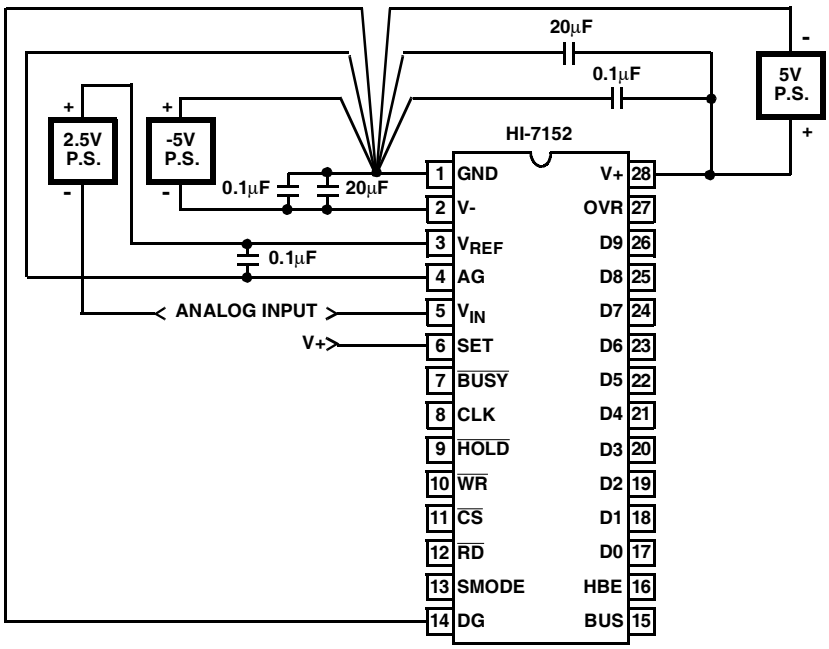
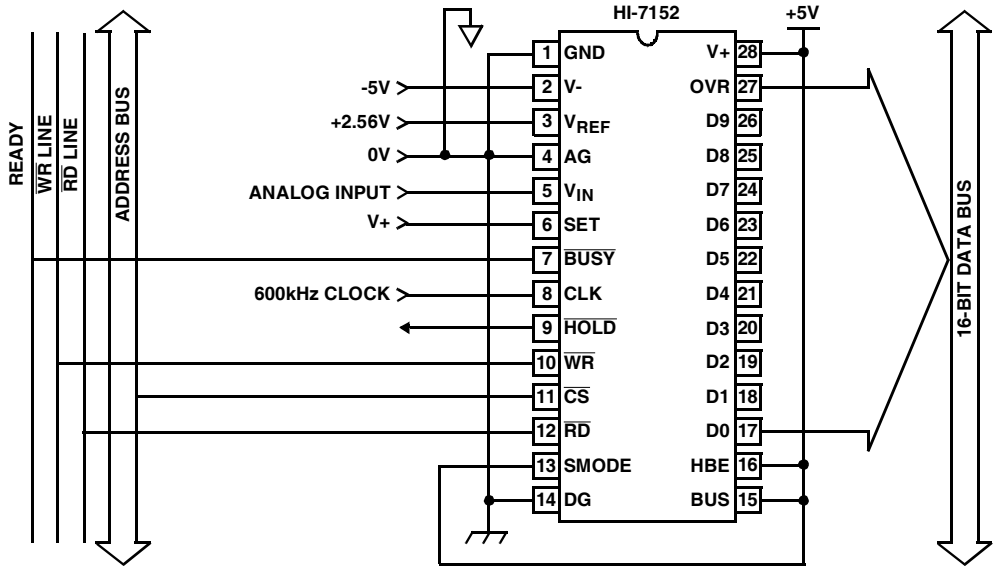


FIGURE 4. GROUND AND POWER SUPPLY DECOUPLING



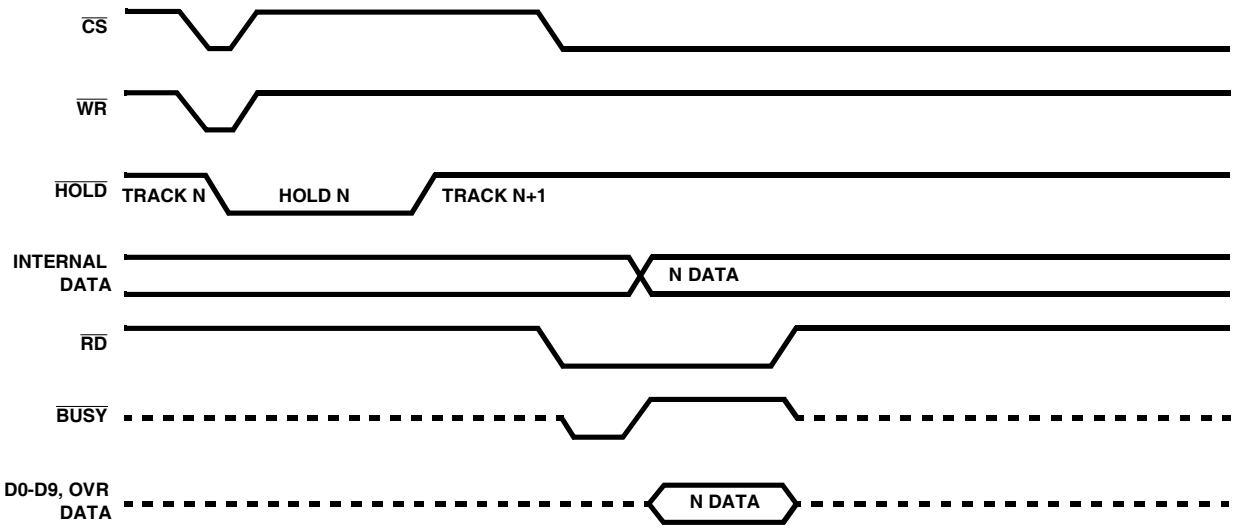


FIGURE 5. SLOW MEMORY MODE APPLICATION

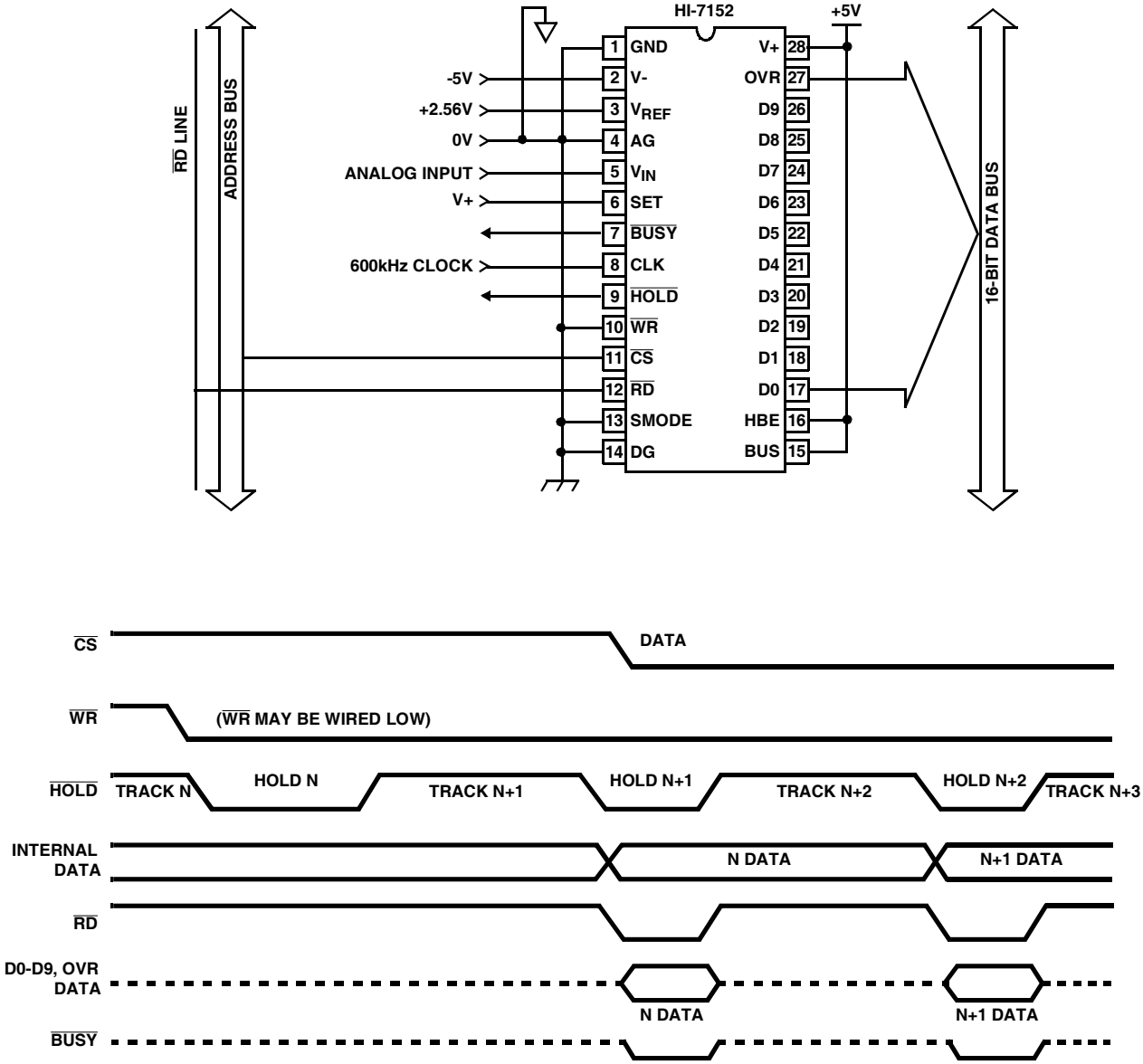


FIGURE 6. FAST MEMORY MODE APPLICATION

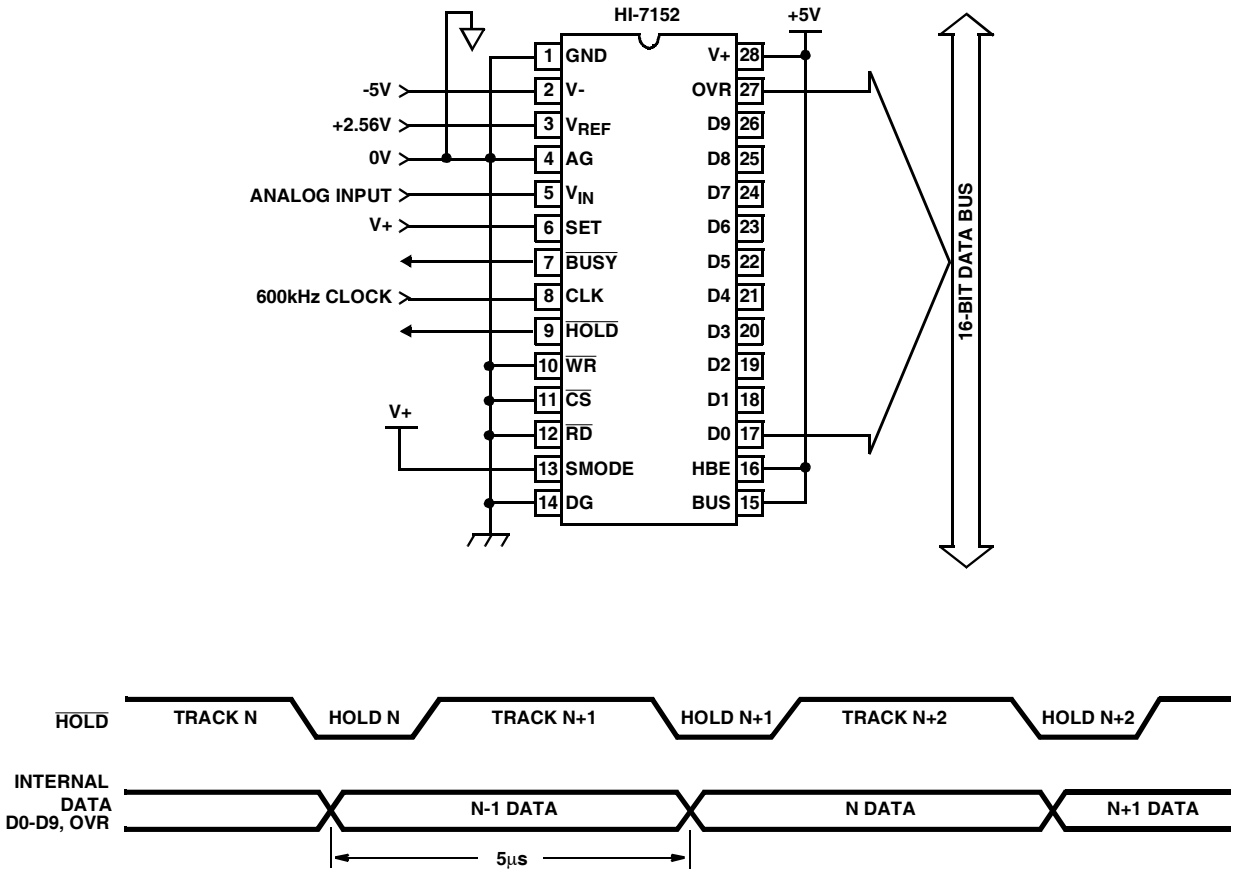


FIGURE 7. DMA MODE APPLICATION

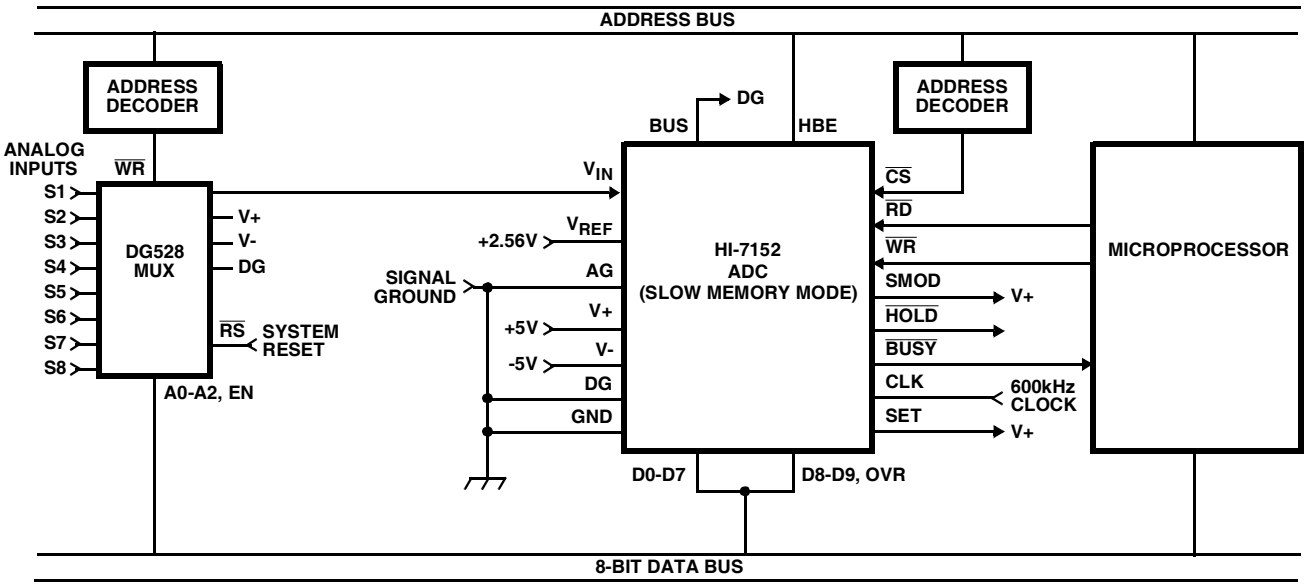


FIGURE 8. MULTI-CHANNEL DATA ACQUISITION SYSTEM

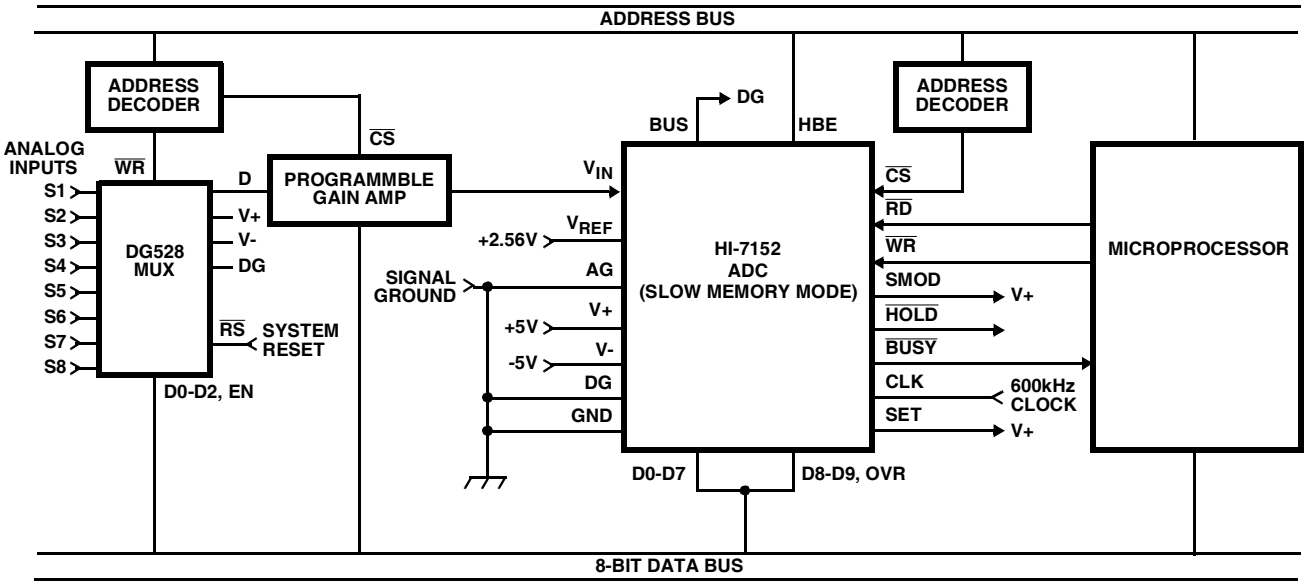


FIGURE 9. MULTI-CHANNEL DATA ACQUISITION SYSTEM WITH PROGRAMMABLE GAIN

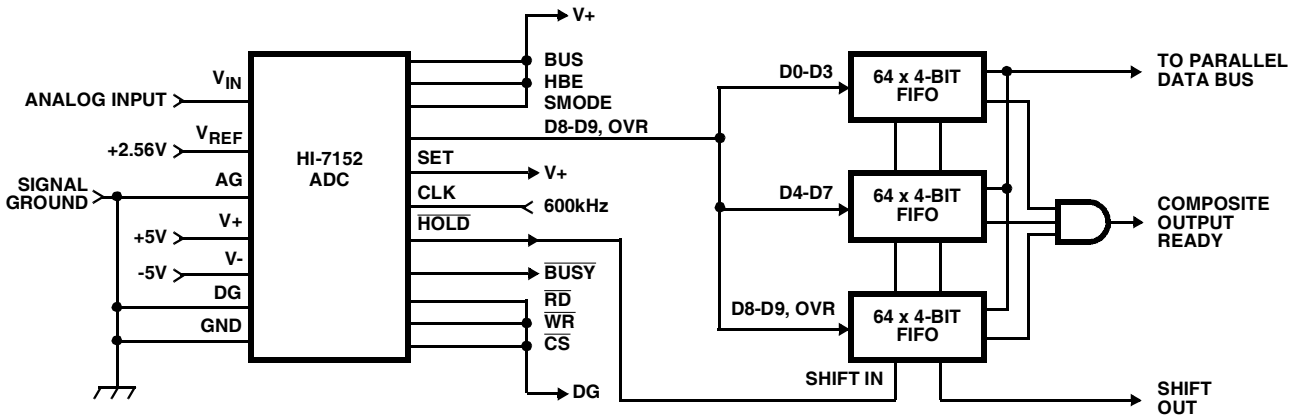


FIGURE 10. DMA/FIFO DATA ACQUISITION SYSTEM