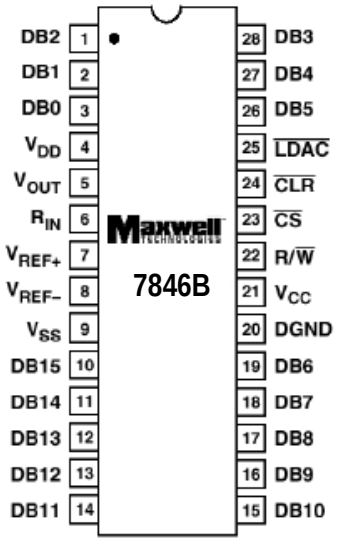
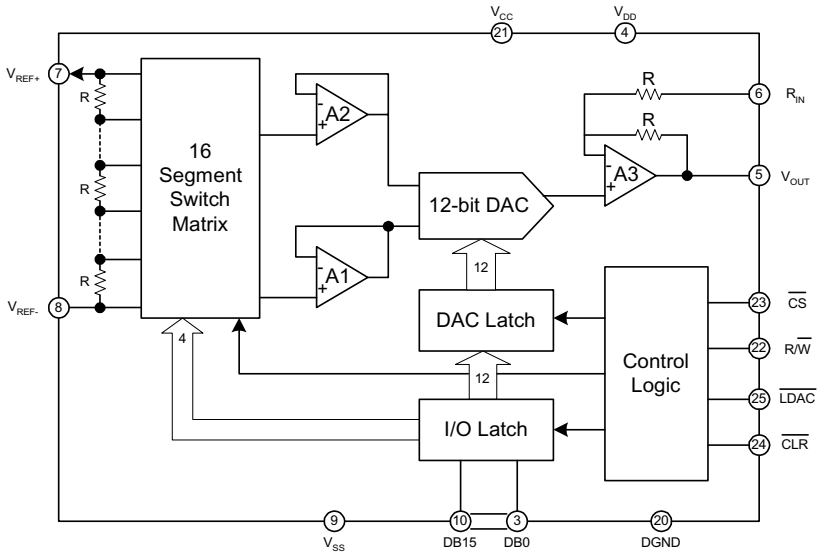
7846B
16-Bit Digital to Analog Converter





Logic Diagram

FEATURES:

- RAD-PAK® technology-hardened against natural space radiation
- Package:
  -28 pin RAD-PAK® Flat Pack
- Microprocessor compatible with readback capability
- 16-Bit monotonicity over temperature
- ±2 LSBs integral linearity error
- Unipolar or bipolar output
- Multiplying capability
- Low power (100 mW typical)

DESCRIPTION:

Maxwell Technologies' 7846B 16-Bit DAC converter microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 7846B has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier which gives the option of unipolar or bipolar output. The 7846B uses a segmented architecture. The 4 MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers. In addition to the excellent accuracy specifications, the 7846B also offers a comprehensive microprocessor interface. There are 16 data I/O pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ have readback function which allows writing to and reading from the I/O latch.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. 7846B PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1-3	DB2-DB0	Data I/O pins. DB0 is LSB.
4	V_{DD}	Positive supply for analog circuitry. This is +15V nominal.
5	V_{OUT}	DAC output voltage pin.
6	R_{IN}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges.
7	V_{REF+}	V_{REF+} Input. The DAC is specified for V_{REF+} = +5V.
8	V_{REF-}	V_{REF-} Input. For unipolar operation connect V_{REF-} to 0V and for bipolar operation connect it to -5V. The device is specified for both conditions.
9	V_{SS}	Negative supply for the analog circuitry. This is -15V nominal.
10-19	DB15-DB6	Data I/O pins. DB15 is MSB.
20	DGND	Ground pin for digital circuitry.
21	V_{CC}	Positive supply for digital circuitry. This is +5V nominal.
22	$R/\overline{W}$	$R/\overline{W}$ Input. This can be used to load data to the DAC or to read back the DAC latch contents.
23	$\overline{CS}$	Chip select input. This selects the device.
24	$\overline{CLR}$	Clear Input. The DAC can be cleared to 000...000 or 100...000.
25	$\overline{LDAC}$	Asynchronous load input to DAC.
26-28	DB5-DB3	Data I/O pins.

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TABLE 2. 7846B ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	MIN	MAX	UNIT
V_{DD} to DGND	-0.3	+17	V
V_{CC} to DGND	-0.3	V_{DD} +0.3 or 7 (Whichever Is Lower)	V
V_{SS} to DGND	-17	+0.3	V
V_{REF+} to DGND	-25	+25	V
V_{REF-} to DGND	-25	+25	V
V_{OUT} to DGND [2]	-25	+25	V
R_{IN} to DGND	-25	+25	V
Digital Input Voltage to DGND	-0.3	V_{CC} +0.3	V
Digital Output Voltage to DGND	-0.3	V_{CC} +0.3	V
Power Dissipation To +75 ˚C Derates above +75 ˚C		 1000 10	 mW mW/˚C
Thermal Inpedance	Θ_{JC}	2.78	°C
Operating Temperature Range	-55	+125	˚C
Storage Temperature Range	-65	+150	˚C

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one absolute maximum rating may be applied at any one time.
2. V_{OUT} may be shorted to DGND, V_{DD}, V_{SS} and V_{CC} provided that the power dissipation of the package is not exceeded.

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{DD}	±10% of value specified in Table 4.
I_{EE}	±10% of value specified in Table 4.
I_{CC}	±10% of value specified in Table 4.

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TABLE 4. 7846B ELECTRICAL SPECIFICATIONS [1]

(VDD=+15V ±5%; VSS=-15V ±5%; V_{CC} = +5 V ±5%, T_A = -55 TO +125°C)

PARAMETER	TEST CONDITIONS/COMMENTS	SUBGROUPS	T_A=-55 °C TO +125 °C	UNIT
Resolution			16	Bits
UNIPOLAR OUTPUT	V_{REF-}=0V, V_{OUT}=0V to +10V			
Relative Accuracy @ 25 °C	1LSB=153µV	1	±16	LSB typ
- T_{MIN} to T_{MAX}		2, 3	±16	LSB max
Differential Nonlinearity Error	Guaranteed Monotonic	1	±1	LSB max
Gain Error @ 25 °C	V_{OUT} Load= 10MΩ	1	±12	LSB typ
- T_{MIN} to T_{MAX}		2,3	±24	LSB max
Offset Error @ 25 °C		1	±12	LSB typ
- T_{MIN} to T_{MAX}		2,3	±24	LSB max
Gain TC [2]		1	±2	ppm FSR/°C typ
Offset TC [2]		1	±2	ppm FSR/°C typ
BIPOLAR OUTPUT	V_{REF-}=-5V, V_{OUT}=-10V to +10V			
Relative Accuracy @ 25 °C	1LSB=305µV	1	±6	LSB typ
- T_{MIN} to T_{MAX}		2, 3	±8	LSB max
Differential Nonlinearity Error	Guaranteed Monotonic	1	±1	LSB max
Gain Error @ 25 °C	V_{OUT} Load=10MΩ	1	±6	LSB typ
- T_{MIN} to T_{MAX}		2, 3	±16	LSB max
Offset Error @ 25 °C	V_{OUT} Load=10MΩ	1	±6	LSB typ
- T_{MIN} to T_{MAX}		2, 3	±16	LSB max
Bipolar Zero Error @ 25 °C		1	±6	LSB typ
- T_{MIN} to T_{MAX}		2, 3	±16	LSB max
Gain TC [2]		1	±2	ppm FSR/°C typ
Offset TC [2]		1	±2	ppm FSR/°C typ
Bipolar Zero TC [2]		1	±2	ppm FSR/°C typ
REFERENCE INPUT				
Input Resistance	Resistance from V_{REF-} to V_{REF+}	1, 2, 3	20	KΩ min
	Typically 30kΩ		40	KΩ max
V_{REF+} Range			V_{SS} + 6 to V_{DD} - 6	V
V_{REF-} Range			V_{SS} + 6 to V_{DD} - 6	V
OUTPUT CHARACTERISTICS				
Output Voltage Swing		1, 2, 3	V_{SS} + 4 to V_{DD} - 3	V max
Resistive Load[1]	To 0V		3	kΩ min
Capacitive Load[3]	To 0V		1000	pF max
Output Resistance			0.3	Ω typ
Short Circuit Current	To 0V or Any Power Supply		±25	mA typ
DIGITAL INPUTS				
V_{IH} (Input High Voltage)		1, 2, 3	2.4	V min
V_{IL} (Input Low Voltage)			0.8	V max
I_{IN} (Input Current)			±10	µA max
C_{IN} (Input Capacitance) [2]			10	pF max
DIGITAL OUTPUTS				
V_{OL} (Output Low Voltage)	I_{SINK} = 1.6mA	1, 2, 3	0.4	V max
V_{OH} (Output High Voltage)	I_{SOURCE} = 400µA		4.0	V min
Floating State Leakage Current	DB0-DB15 = 0 to V_{CC}		±10	µA max
Floating State Output Capacitance [2]			10	pF max

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TABLE 4. 7846B ELECTRICAL SPECIFICATIONS [1]

(VDD=+15V ±5%; VSS=-15V ±5%; V_{CC} = +5 V ±5%, T_A = -55 TO +125°C)

PARAMETER	TEST CONDITIONS/COMMENTS	SUBGROUPS	T_A=-55 °C TO +125 °C	UNIT
POWER REQUIREMENTS [4]				
V_{DD}		1, 2, 3	+11.4/+15.75	V min/V max
V_{SS}			-11.4/-15.75	V min/V max
V_{CC}			+4.75/+5.25	V min/V max
I_{DD}	V_{OUT} Unloaded		5	mA max
I_{SS}	V_{OUT} Unloaded		5	mA max
I_{CC}			1	mA max
Power Supply Sensitivity [5]			2	LSB/V max
Power Dissipation	V_{OUT} Unloaded		100	mW typ

1. Minimum load is 3kΩ.
2. Sample tested to ensure compliance.
3. Maximum load is 1000pF.
4. 7846ARP is functional with power supplies of ±12V. See typical performance curves.
5. Sensitivity to Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.
6. Guaranteed by design

TABLE 5. 7846B AC PERFORMANCE CHARACTERISTICS[1]

(VDD=+15V ±5%; VSS=-15V ±5%; V_{CC} = +5 V ±5%, T_A = -55 TO +125°C)

PARAMETER	TEST CONDITIONS	T_A=25°C	T_A=T_{MIN} TO T_{MAX}	UNIT
Output Settling Time	To 0.006% FSR. V_{OUT} loaded. V_{REF-}=0V.	7	7	µs max
	To 0.003% FSR. V_{OUT} loaded. V_{REF-}=-5V.	9	9	µs max
Digital-to-Analog Glitch Impulse	DAC alternately loaded with 10…0000 and 01…1111. V_{OUT} unloaded.	400	400	nV-secs typ
AC Feed through	V_{REF-}=0V, V_{REF+}=1V rms, 10kHz sine wave. DAC loaded with all 0s.	0.5	0.5	mV pk-pk typ
Digital Feed through	DAC alternately loaded with all 1s and all 0s. CS High.	10	10	nV-secs typ
Output Noise Voltage Density (1kHz-100kHz)	Measured at V_{OUT}. DAC loaded with 0111011…11. V_{REF+}=V_{REF-}=0V.	50	50	nV/(Hz)½ typ

1. Guaranteed by design.

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TABLE 6. 7846B TIMING CHARACTERISTICS[1,2,3,4]

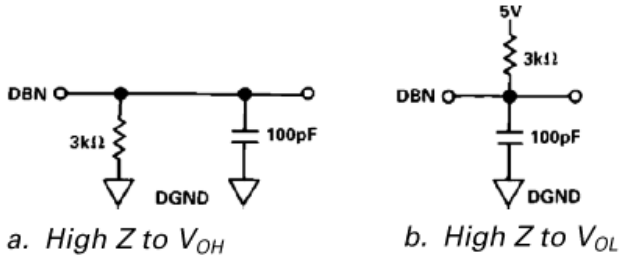
(V_{DD} = +14.25V TO 15.75V; V_{SS} = -14.25V TO -15.75V; V_{CC} = 4.75 TO 5.25V; UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS/COMMENTS	LIMIT AT T_A=-55 ˚C TO +125 ˚C	UNIT
t_1	R/$\overline{W}$ to $\overline{CS}$ Setup Time	50	ns min
t_2	$\overline{CS}$ Pulse Width (Write Cycle)	190	ns min
t_3	R/$\overline{W}$ to $\overline{CS}$ Hold Time	50	ns min
t_4	Data Setup Time	120	ns min
t_5	Data Hold Time	0	ns min
t_6	Data Access Time	320	ns max
t_7	Bus Relinquish Time	10	ns min
		90	ns max
t_8	$\overline{CLR}$ Setup Time	20	ns min
t_9	$\overline{CLR}$ Pulse Width	150	ns min
t_{10}	$\overline{CLR}$ Hold Time	0	ns min
t_{11}	$\overline{LDAC}$ Pulse Width	100	ns min
t_{12}	$\overline{CS}$ Pulse Width (Read Cycle)	330	ns min

1. Guaranteed by design. All input control signals are specified with $t_R = t_F$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
2. t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
3. t_7 is defined as the time required for an output to change 0.5V when loaded with the circuits of Figure 2. Specifications subject to change without notice.
4. See Figure 3 on page 7.

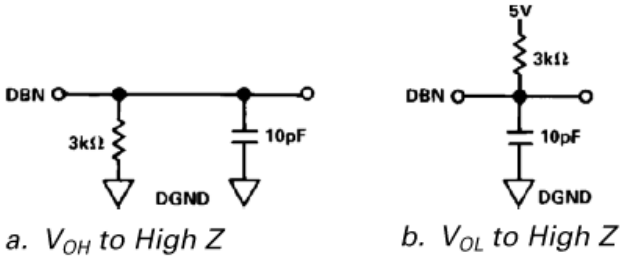
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FIGURE 1. LOAD CIRCUITS FOR ACCESS TIME (t_6)



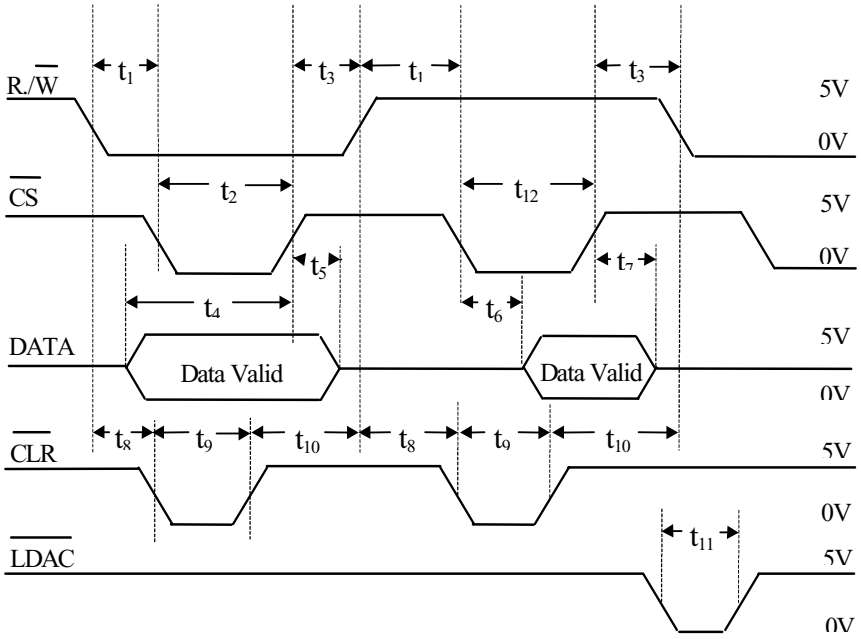
a. High Z to V_{OH} b. High Z to V_{OL}

FIGURE 2. LOAD CIRCUITS FOR BUS RELINQUISH TIME (t_7)



a. V_{OH} to High Z b. V_{OL} to High Z

FIGURE 3. 16-BIT DIGITAL TO ANALOG CONVERTER



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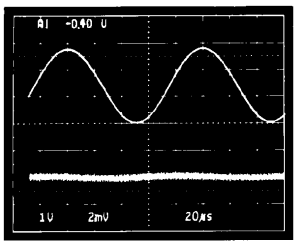


Figure 4. AC Feedthrough. V_{REF+} = 1 V rms, 10 kHz Sine Wave

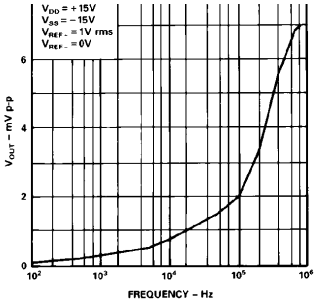


Figure 5. AC Feedthrough vs. Frequency

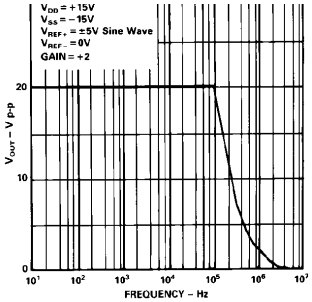


Figure 6. Large Signal Frequency Response

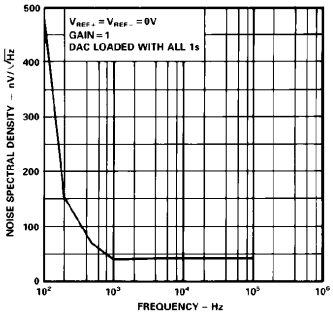


Figure 7. Noise Spectral Density

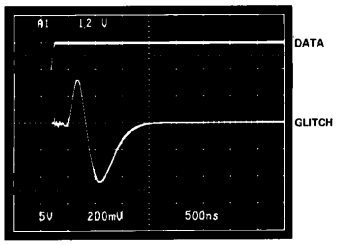


Figure 8. Digital-to-Analog Glitch Impulse without Internal Deglitcher (10 . . . 000 to 011 . . . 111 Transition)

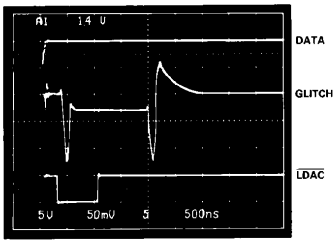


Figure 9. Digital-to-Analog Glitch Impulse with Internal Deglitcher (10 . . . 000 to 011 . . . 111 Transition)

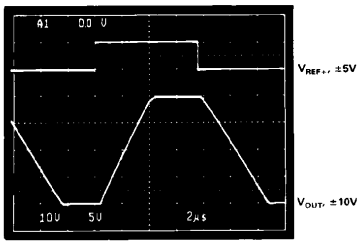


Figure 10. Pulse Response (Large Signal)

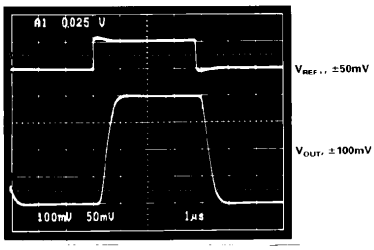


Figure 11. Pulse Response (Small Signal)

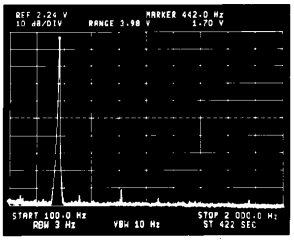


Figure 12. Spectral Response of Digitally Constructed Sine Wave

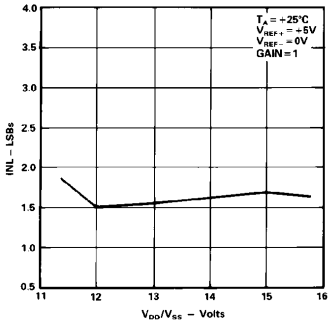


Figure 13. Typical Linearity vs. V_{DD}/V_{SS}

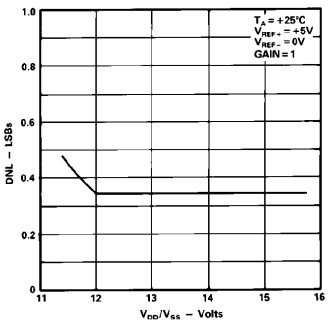
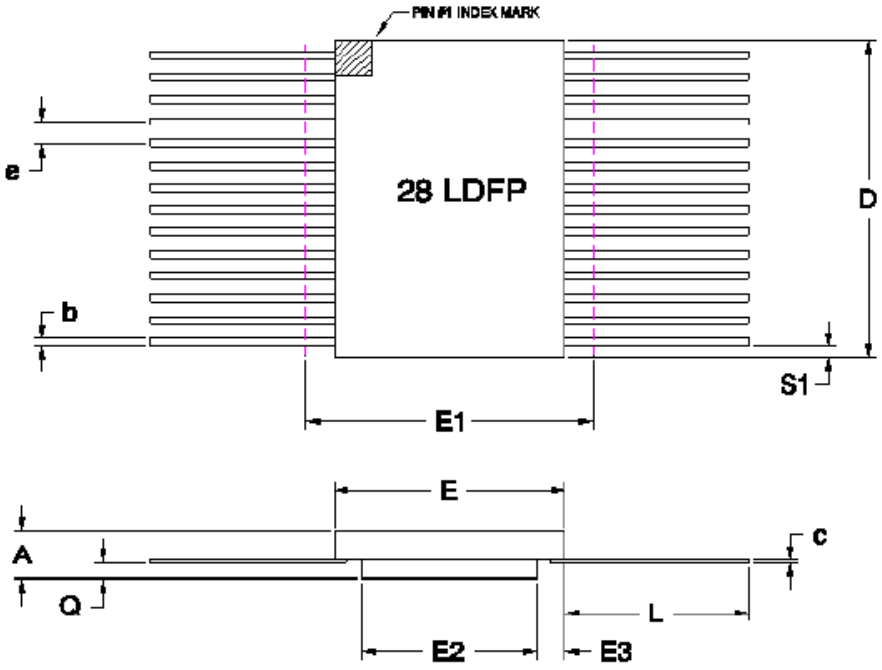


Figure 14. Typical Monotonicity vs. V_{DD}/V_{SS}

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28 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.190	0.207	0.224
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.720	0.740
E	0.380	0.410	0.420
E1	--	--	0.440
E2	0.180	0.250	--
E3	0.030	0.080	--
e	0.050 BSC		
L	0.360	0.370	0.380
Q	0.062	0.073	0.081
S1	0.000	0.027	--
N	28		

Note: All dimensions in inches

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Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

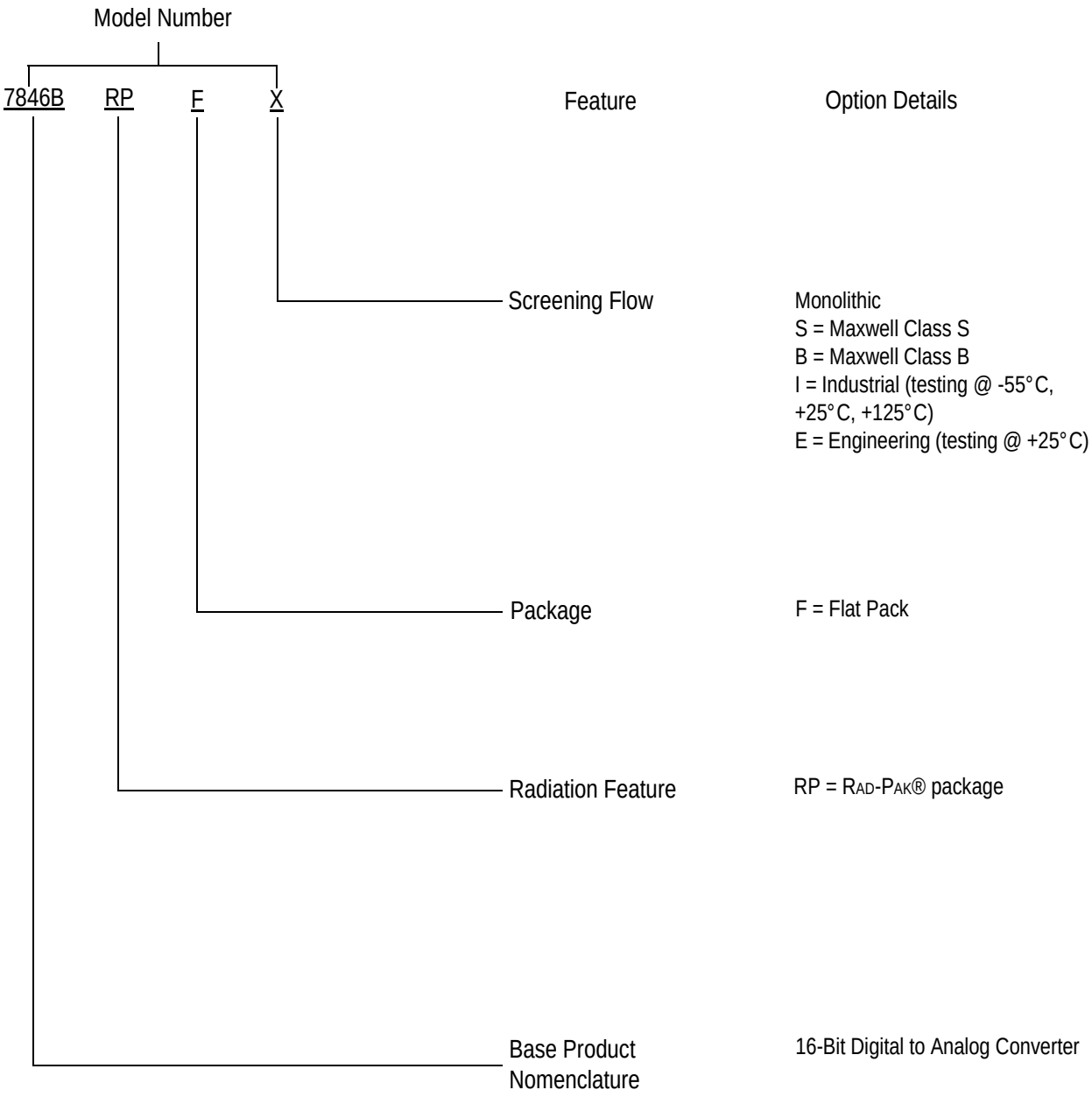
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