

CY62167G Automotive

16-Mbit (1M Words × 16 Bit) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby power
 Typical standby current: 5.5 μA
 Maximum standby current: 75 μA
- High speed: 45 ns / 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Temperature Ranges:
 Automotive-A: -40 °C to +85 °C
 Automotive-E: -40 °C to +125 °C
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

CY62167G is high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC. This device is offered in dual chip-enable.

Devices with dual chip-enable are accessed by asserting both chip-enable inputs – CE₁ as LOW and CE₂ as HIGH.

<u>Data</u> writes are performed by asserting the Write Enable input (WE) LOW, and providing the data and address on device data (I/O_0 through I/O_{15}) and address (A_0 through A_{19}) pins respectively. The Byte High/Low Enable (BHE, BLE) inputs control byte writes, and write data on the corresponding I/O lines

to the <u>memory</u> location specified. BHE controls I/O_8 through I/O_{15} : BLE controls I/O_0 through I/O_7 .

Data reads are performed by asserting the Output Enable (OE) input and providing the required address on the address lines. Read data is accessible on I/O lines (I/O₀ through I/O₁₅). Byte accesses can <u>be performed</u> by asserting the required byte enable signal (BHE, BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through $\underline{I/O}_{15})$ are placed in a HI-Z state when the device is deselected (CE_1 HIGH / CE_2 LOW for dual chip-enable

device), or control signals are de-asserted (\overline{OE} , \overline{BLE} , and \overline{BHE}).

These devices also have a unique "Byte Power down" feature

where if both the Byte Enables (\overline{BHE} and \overline{BLE}) are disabled, the devices seamlessly switches to standby mode irrespective of the state of the chip enable(s), thereby saving power.

The CY62167G device is available in a Pb-free 48-ball VFBGA and 48-pin TSOP I packages. The device in the 48-pin TSOP I package can also be configured to function as a 2 M words × 8 bit device. The logic block diagram is on page 2. Refer to Pin Configurations on page 4 and the associated footnotes for details.

Note
1. This device does not support automatic write-back on error detection.

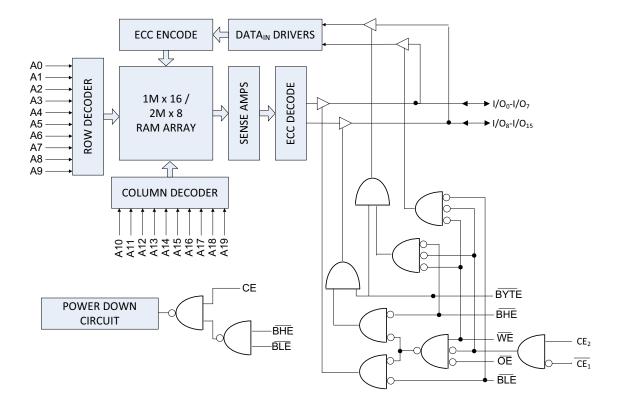
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Logic Block Diagram – CY62167G





CY62167G Automotive

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Pin Configurations

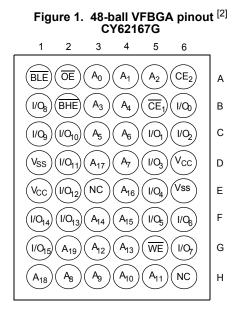


Figure 2. 48-pin TSOP I pinout (Dual Chip Enable without ERR) – CY62167G^[2, 3]

A15 🖬 1	48 416
A14 2	48 = <u>A16</u> 47 = BYTE
A13 _ 3	46 Vss
A12 4	45 – I/O15/A20
A11 🖬 5	44 🖬 1/07
A10 🖬 6	43 🗖 I/O14
A9 🗖 7	42 🗖 1/06
A8 🖴 8	41 🗖 1/013
A19 🛏 9	40 📩 1/O5
NC 🗖 10	39 🗖 I/O12
WE 🗖 11	38 🖿 I/O4
CE ₂ = 12 <u>NC</u> = 13	37 🗖 Vcc
<u>NC</u>	36 🗖 I/O11
BHE = 14	35 🗖 1/03
BLE 🗖 15	34 🛏 I/O10
A18 🗖 16	33 🗖 1/02
A17 = 17	32 = 1/09
A7 = 18	31 - 1/01
A6 = 19	30 = 1/08
A5 🖬 20 A4 🖬 21	29 = 1/ <u>O</u> 0
A4 🖬 21 A3 🖬 22	
A3 H 22 A2 H 23	27 = <u>Vss</u> 26 = <u>CE</u> ₁ 25 = A0
A2 = 23 A1 = 24	20 CE ₁ 25 A0
A1 47	23 A 0

Product Portfolio

				Power Dissipation					
Product	Range	V _{CC} Range (V)	Speed (ns)	Operating I _{CC}	perating I _{CC} , (mA), f = f _{max}		Ι _{SB2} (μΑ)		
			(,	Тур ^[4]	Мах	Typ ^[4]	Max		
CY62167G30	Automotive-E	2.2 V–3.6 V	55	29.0	40.0	5.5	75.0		
C102107G30	Automotive-A	2.2 V-3.0 V	45	29.0	36.0	5.5	16.0		

Notes

NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration. 2.

The BYTE pin in the <u>48-pin TSOP I package</u> must be tied to V_{CC} to use the device as a 1 <u>M × 16 SRAM</u>. The 48-pin TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, pin 45 is A20, while BHE, BLE and I/O₈ to I/O₁₄ pins are not used.
 Indicates the value for the center of Distribution at 3.0 V, 25 °C and not 100% tested.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	–65 °C to + 150 °C
Ambient temperature with power applied	–55 °C to + 125 °C
Supply voltage to ground potential ^[5]	–0.5 V to V _{CC} + 0.5 V
DC voltage applied to outputs in HI-Z state ^[5]	–0.5 V to V _{CC} + 0.5 V
DC input voltage [5]	–0.5 V to V _{CC} + 0.5 V

DC Electrical Characteristics

Over the Operating Range

Output current into outputs (LOW) 20 mA
Static discharge voltage (MIL-STD-883, Method 3015) >2001 V
Latch-up current>140 mA

Operating Range

Grade	Ambient Temperature	V _{cc}
Automotive-E	–40 °C to +125 °C	2.2 V to 3.6 V
Automotive-A	–40 °C to +85 °C	

Parameter	Parameter Description		Test Conditions 5		55 ns	(Autor	notive -E)	55 ns	Unit		
Parameter	Descr	iption	Test Conditio	ns	Min	Typ ^[6]	Max	Min	Тур [6]	Max	Unit
V _{OH}		2.2 V to 2.7 V	V _{CC} = Min, I _{OH} = -0.1	mA	2.0	-	-	2.0	-	-	V
	voltage	2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = -1.0	V _{CC} = Min, I _{OH} = -1.0 mA		-	_	2.2	-	-	
V _{OL}	Output LOW	2.2 V to 2.7 V	V _{CC} = Min, I _{OL} = 0.1 m	V_{CC} = Min, I_{OL} = 0.1 mA		-	0.4	-	-	0.4	V
	voltage	2.7 V to 3.6 V	V _{CC} = Min, I _{OL} = 2.1 m	ıΑ	-	-	0.4	-	-	0.4	
V _{IH}	Input HIGH	2.2 V to 2.7 V	-		2.0	-	V _{CC} + 0.3	2.0	-	V _{CC} + 0.3	V
	voltage ^[5]	2.7 V to 3.6 V	-		2.0	-	V _{CC} + 0.3	2.0	-	V _{CC} + 0.3	
V _{IL}	Input LOW	2.2 V to 2.7 V			-0.3	-	0.6	-0.3	-	0.6	V
	voltage ^[5]	2.7 V to 3.6 V			-0.3	-	0.8	-0.3	-	0.8	
I _{IX}	Input leakage	current	$GND \leq V_{IN} \leq V_{CC}$		-4.0	-	+4.0	-1.0	-	+1.0	μA
I _{OZ}	Output leakag	e current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled		-4.0	-	+4.0	-1.0	-	+1.0	μA
I _{CC}	V _{CC} operating	supply	V _{CC} = Max,	f = f _{MAX}	-	29.0	40.0	_	29.0	36.0	mA
	current		I _{OUT} = 0 mA, CMOS levels	f =1 MHz	-	7.0	18.0	-	7.0	9.0	mA
I _{SB1} ^[7]	Automatic pov current – CMC V_{CC} = 2.2 to 3	DS inputs;	$\overline{CE}_{1} \ge V_{CC} - 0.2 \text{ V or } CE_{2} \le 0.2 \text{ V}$ or (BHE and BLE) $\ge V_{CC} - 0.2 \text{ V}$, $V_{IN} \ge V_{CC} - 0.2 \text{ V}$, $V_{IN} \le 0.2 \text{ V}$, $f = f_{max}$ (address and data only), $f = 0$ (OE, and WE), $V_{CC} = V_{CC(max)}$		_	5.5	75.0	_	5.5	16.0	μA
I _{SB2} ^[7]	Automatic pov current – CMC V _{CC} = 2.2 to 3	DS inputs;	$\label{eq:cellson} \begin{split} \overline{CE}_1 &\geq V_{CC} - 0.2V \text{ or } C\\ \text{or } (\overline{BHE} \text{ and } \overline{BLE}) &\geq V\\ V_{IN} &\geq V_{CC} - 0.2 \text{ V or}\\ V_{IN} &\leq 0.2 \text{ V},\\ f &= 0, \ V_{CC} = V_{CC(max)} \end{split}$		_	5.5	75.0	_	5.5	16.0	μA

Notes

- V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 2 ns.
 Indicates the value for the center of <u>Distribution</u> at 3.0 V, 25 °C and not 100% tested.
 Chip enables (CE₁ and CE₂) and BHE, BLE and BYTE must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.



Capacitance

Parameter ^[8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
JA		Still air, soldered on a 3 × 4.5 inch, 4-layer printed circuit board	31.50	57.99	°C/W
- 30	Thermal resistance (junction to case)		15.75	13.42	°C/W

AC Test Loads and Waveforms

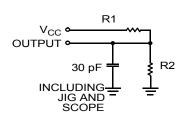
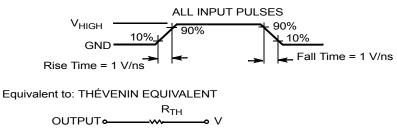


Figure 3. AC Test Loads and Waveforms



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V _{HIGH}	3.0	V

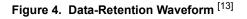


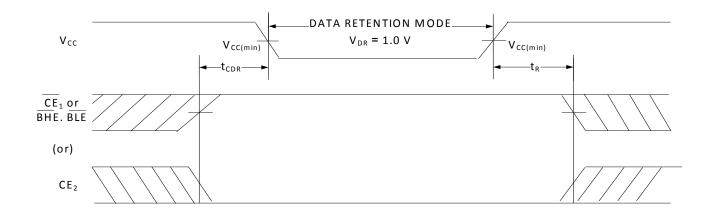
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	55 ns (Automotive -E)			45 ns (Automotive -A)			Unit
Farameter	Description	Conditions	Min	Typ ^[9]	Мах	Min	Typ ^[9]	Мах	Unit
V _{DR}	V _{CC} for data retention		1	-	Ι	1	-	Ι	V
ICCDR ^[10]		$\begin{array}{l} \underline{2.2 \ V < V_{CC} \leq 3.6 \ V} \\ \overline{CE}_1 \geq V_{CC} - \underline{0.2 \ V} \ \text{or} \ CE_2 \leq \underline{0.2 \ V} \\ \text{or} \ (BHE \ \text{and} \ \overline{BLE}) \geq V_{CC} - \underline{0.2 \ V} \\ V_{IN} \geq V_{CC} - \underline{0.2 \ V} \ \text{or} \ V_{IN} \leq \underline{0.2 \ V} \end{array}$	_	5.5	75.0	_	5.5	16.0	μA
t _{CDR} ^[11]	Chip deselect to data-retention time		0	-	_	0	-	-	-
t _R ^[12]	Operation-recovery time		55	-	-	45	-	-	ns

Data Retention Waveform





Notes

- 9. Indicates the value for the center of distribution at 3.0 V, 25°C and not 100% tested. 10. Chip enables (\overline{CE}_1 and CE_2) and \overline{BYTE} must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating. 11. Tested initially and after any design or process changes that may affect these parameters. 12. <u>Full device</u> operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} \geq 100 µs or stable at V_{CC(min}) \geq 100 µs. 13. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both BHE and BLE.



Switching Characteristics

Parameter ^[14]	Departmen	55 ns (Au	tomotive-E)	45 ns (Automotive-A)		Unit
Parameter	Description	Min	Max	Min	Max	Unit
Read Cycle			•			
t _{RC}	Read cycle time	55	-	45	_	ns
t _{AA}	Address to data valid	-	55	-	45	ns
t _{OHA}	Data hold from address change	10	-	10	_	ns
t _{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid / \overline{CE} LOW	-	55	-	45	ns
t _{DOE}	OE LOW to data valid / OE LOW	-	25	-	22	ns
t _{LZOE}	OE LOW to Low Z ^[15]	5	-	5	_	ns
t _{HZOE}	OE HIGH to High Z ^[15, 16]	-	20	-	18	ns
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to Low Z ^[15]	10	-	10	_	ns
t _{HZCE}	CE ₁ HIGH and CE ₂ LOW to High Z ^[15, 16]	-	20	-	18	ns
t _{PU}	CE ₁ LOW and CE ₂ HIGH to power-up	0	-	0	_	ns
t _{PD}	CE ₁ HIGH and CE ₂ LOW to power-down	-	55	-	45	ns
t _{DBE}	BLE / BHE LOW to data valid	-	55	-	45	ns
t _{LZBE}	BLE / BHE LOW to Low Z ^[15]	5	-	5	-	ns
t _{HZBE}	BLE / BHE HIGH to High Z ^[15, 16]	-	20	-	18	ns
Write Cycle [17]	·					
t _{WC}	Write cycle time	55	-	45	-	ns
t _{SCE}	CE ₁ LOW and CE ₂ HIGH to write end	40	-	35	-	ns
t _{AW}	Address setup to write end	40	-	35	-	ns
t _{HA}	Address hold from write end	0	-	0	-	ns
t _{SA}	Address setup to write start	0	-	0	-	ns
t _{PWE}	WE pulse width	40	-	35	-	ns
t _{BW}	BLE / BHE LOW to write end	40	-	35	-	ns
t _{SD}	Data setup to write end	25	-	25	-	ns
t _{HD}	Data hold from write end	0	-	0	-	ns
t _{HZWE}	WE LOW to High Z ^[15, 16]	-	20	-	18	ns
t _{LZWE}	WE HIGH to Low Z ^[15]	10	-	10	_	ns

Notes

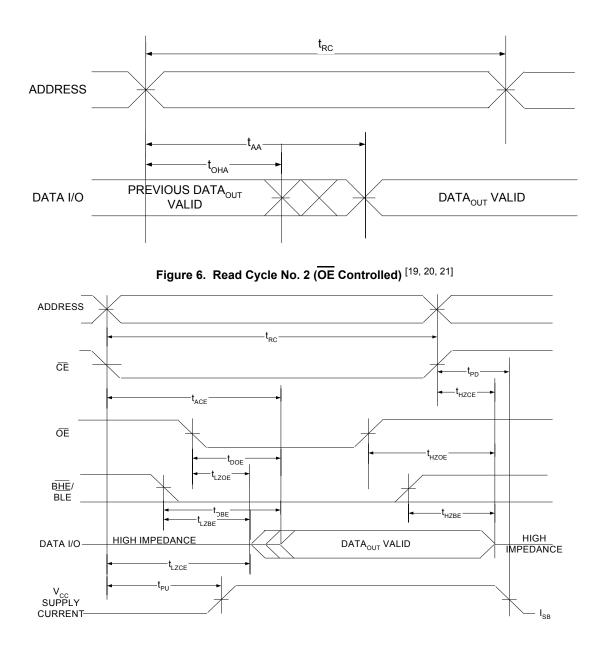
14. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V_{CC} ≥ 3 V) and V_{CC}/2 (for V_{CC} < 3 V), and input pulse levels of 0 to 3 V (for V_{CC} ≥ 3 V) and 0 to V_{CC} (for V_{CC} < 3 V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.

15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZDE}, t_{HZCE} is less than t_{LZDE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZCE}, t_{HZCE}, t_{HZEE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write. Any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.



Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62167G (Address Transition Controlled) ^[18, 19]



Notes

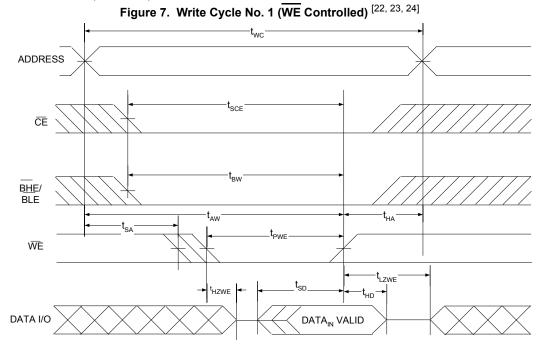
18. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .

19. WE is HIGH for read cycle.
 20. Eor all dual chip enable devices, CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.

21. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.



Switching Waveforms (continued)



Notes

22. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, CE is HIGH.

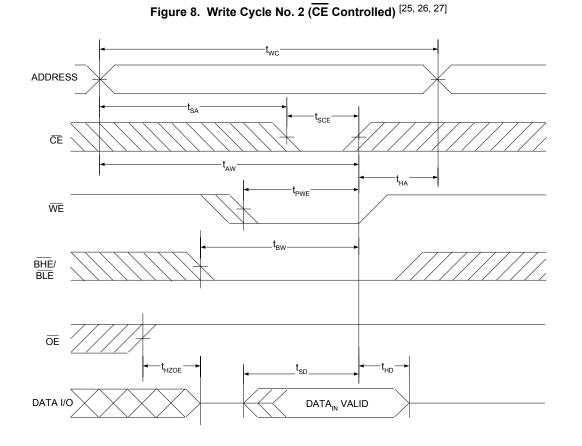
23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

^{24.} Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.





Switching Waveforms (continued)



Notes

- 25. Eor all dual chip enable devices, CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.
- 26. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{|L}$, $\overline{CE}_1 = V_{|L}$, \overline{BHE} or \overline{BLE} or both = $V_{|L}$, and $CE_2 = V_{|H}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

27. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.





Switching Waveforms (continued)

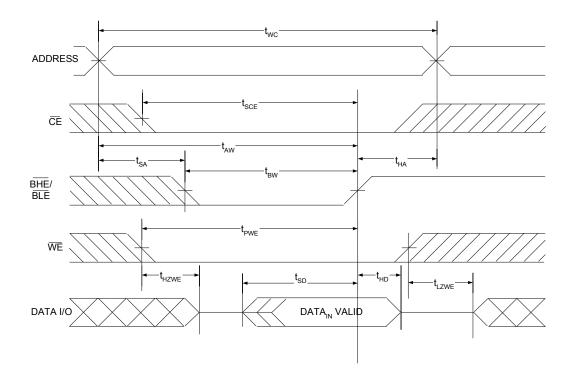


Figure 9. Write Cycle No. 3 (BHE/BLE controlled, OE LOW) ^[28, 29, 30]

Notes

28. Eor all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

29. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{JL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write the edge of the signal that terminates the write terminates the terminate terminate terminates the write terminate terminate terminates the terminate terminate terminates write.

30. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.





Truth Table – CY62167G

CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	X ^[31]	Х	Х	Х	Х	HI-Z	Deselect/Power-down	Standby (I _{SB})
X ^[31]	L	Х	Х	Х	Х	HI-Z	Deselect/Power-down	Standby (I _{SB})
X ^[31]	X ^[31]	Х	Х	Н	Н	HI-Z	Deselect/Power-down	Standby (I _{SB})
L	Н	Н	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Η	L	Н	L	Data Out (I/O ₀ –I/O ₇); HI-Z (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Η	L	L	Н	HI-Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	Н	Х	Х	HI-Z	Output disabled	Active (I _{CC})
L	Н	L	Х	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	Н	L	Data In (I/O ₀ –I/O ₇); HI-Z (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	L	Н	HI-Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})

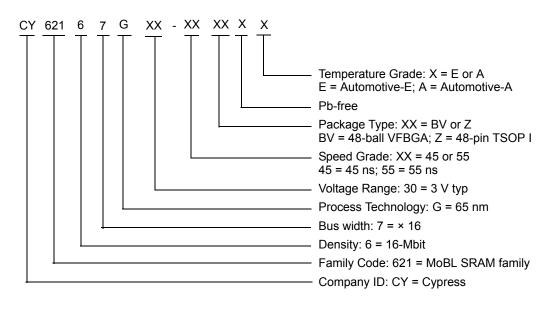
Note 31. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167G30-55BVXE	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	Automotive-E
	CY62167G30-55ZXE		48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A	
45	CY62167G30-45ZXA	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A	Automotive-A
	CY62167G30-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	

Ordering Code Definitions

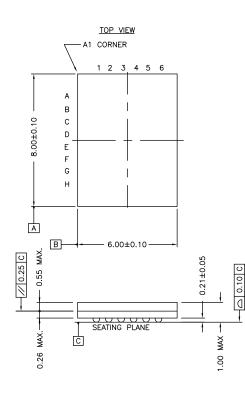


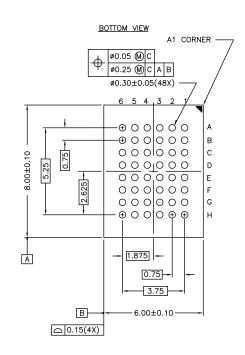




Package Diagram

Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150





NOTE:

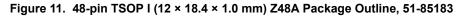
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H



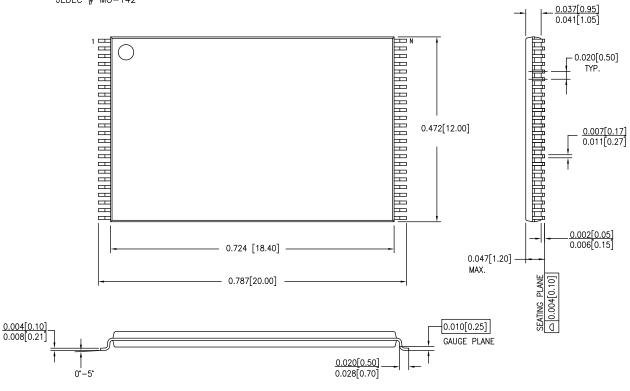


Package Diagram (continued)



DIMENSIONS IN INCHES[MM] MIN.

JEDEC # MO-142



51-85183 *D





Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
VFBGA	very fine-pitch ball grid array
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μS	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts



Document History Page

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*C	5083752	NILE	01/13/2016	Changed status from Preliminary to Final.
*D	5130998	NILE	02/12/2016	Updated Logic Block Diagram – CY62167G. Updated Pin Configurations: Added Note 3 and referred the same note in Figure 2. Updated DC Electrical Characteristics: Updated Note 7. Updated Data Retention Characteristics: Updated Note 10.



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