

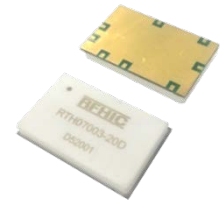


Product Features

- GaN on SiC Chip on Board
- Surface Mount Hybrid Type
- 2-Stage Doherty Amplifier
- High Efficiency
- No Matching circuit needed

Applications

- RF Sub-Systems
- Base Station
- RRH
- 4G/ LTE system
- Small cell



Package Type : SP-1E

Description

Accommodating the future of 4G/LTE small cells, RFHIC introduces RTH07003-20D amplifier fabricated using an advanced high power density Gallium Nitride (GaN) semiconductor process.

Electrical Specifications @ $V_{ds1}=5V$, $V_{ds2}=30V$, $T_a=25^\circ C$

PARAMETER	UNIT	MIN	TYP	MAX	CONDITION
Frequency Range	MHz	773	778	783	ZS = ZL = 50 ohm
Power Gain		27	30	-	
Gain Flatness	dB	-1.5	-	+1.5	-
Input Return Loss		-	-14	-9	
Pout @ Average	dBm	-	34.7	-	2.951W
Pout @ Saturation	dBm	42.2	42.7	-	Pulse Width=20us, Duty cycle 10%
ACLR @ BW 10MHz LTE (PAPR 7.5dB)	dBc	-	-29	-25	Non DPD
		-	-53	-	With DPD
Doherty Efficiency	%	-	43	-	$T_c=25^\circ C$
Total Efficiency		35	38	-	
Drive Amp. Idq	mA	-	180	-	Inverted Doherty
Carrier Amp. Idq		-	120	-	
Peaking Amp. Idq		-	0	-	
Supply Voltage	V	-4.9	-4.5	-3.0	Vgc
		-4.9	-2.8	-2.0	Vgp
		-	5.0	-	Vds1
		-	30	-	Vds2

Caution

The drain voltage must be supplied to the device after the gate voltage is supplied

Turn on → Turn on the Gate voltage supply and last turn on the Drain voltage supplies

Turn off → Turn off the Drain voltage and last turn off the Gate voltage

Note

1. ACLR Measured Pout=34.7dBm @ $f_c \pm 10MHz / 9.015MHz$
LTE 10MHz 1FA PAPR=7.5dB @ 0.01% probability on CCDF

Mechanical Specifications

PARAMETER	UNIT	TYPICAL	RATING
Mass	g	6.0	± 1.0
Dimension	mm	32 x 20 x 4.2	± 0.15

Absolute Maximum Ratings

PARAMETER	UNIT	RATING	SYMBOL	CONDITION
Gate-Source Voltage	V	-10 ~ 0	V _{gc} V _{gp}	T _c =25°C
Drain-Source Voltage 1	V	7	V _{ds1}	T _c =25°C
Drain-Source Voltage 2	V	50	V _{ds2}	T _c =25°C
Gate Current	mA	4 4	Carrier Peaking	T _c =25°C
Power Dissipation	W	6.1	P _d	T _c =85°C
Operating Junction Temperature	°C	225	T _J	-
Operating Case Temperature	°C	-30 ~ 85	T _C	-
Storage Temperature	°C	-40 ~ 100	T _{STG}	-
Soldering Temperature ^{*1}	°C	260	T _s	30s Max.
RF Input Level (Pulse)	dBm	30	Pin	T _c =25°C

*1 Reflow cycle limit : 1time

Operating Voltages & Input level

PARAMETER	UNIT	MIN	TYP	MAX	SYMBOL
Drain Voltage 1	V	4.75	5	5.25	V _{ds1}
Drain Voltage 2	V	29.5	30	30.5	V _{ds2}
Gate Voltage (on-stage)	V	-4.9	V _{gc} ^{*2}	-3.0	V _{gc}
Gate Voltage (on-stage)	V	-4.9	V _{gp} ^{*3}	-2.0	V _{gp}
Gate Voltage (off-stage)	V	-	-8	-	V _{gc}
Gate Voltage (off-stage)	V	-	-8	-	V _{gp}
RF Input Level (Pulse)	dBm	-	-	25	Pin

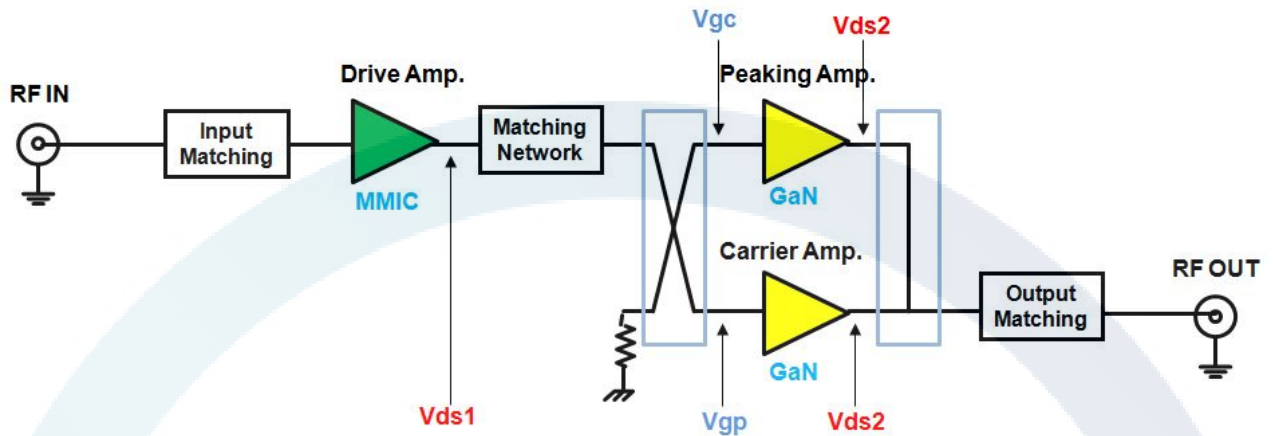
*2 V_{gc}(Pin#13) set: Lower V_{gc} of Δ-1.75V at Peaking I_{dq} 100mA±5%

*3 V_{gp}(Pin#5) set: Carrier I_{dq} 120mA±5%

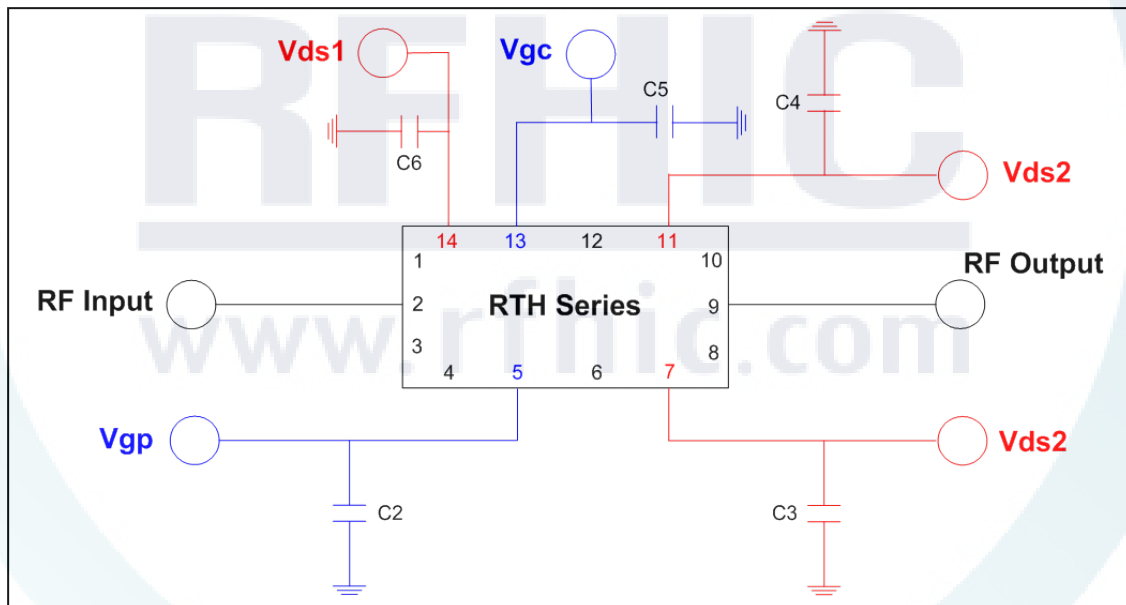
ESD Level

PARAMETER	STANDARD	RESULT
HBM	JESD22-A114E	Class 1B/ passed Voltage 700V
MM	JESD22-A115C	Class A/ passed Voltage 150V

Block Diagram



Application Circuit



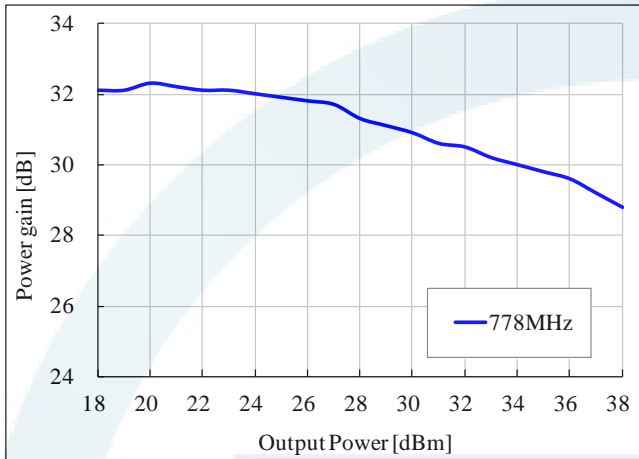
Bill of Material (Evaluation board)

LOCATION	Part Number	Value	Manufacturer
C3, C4, C6	1812B225K101CT	2.2uF / 100V	WALSIN
C2, C5	GRM188R71C105KA12D	1uF / 16V	MURATA
PCB	RO4350B	2Layer, 20mil, 1oz	ROGERS

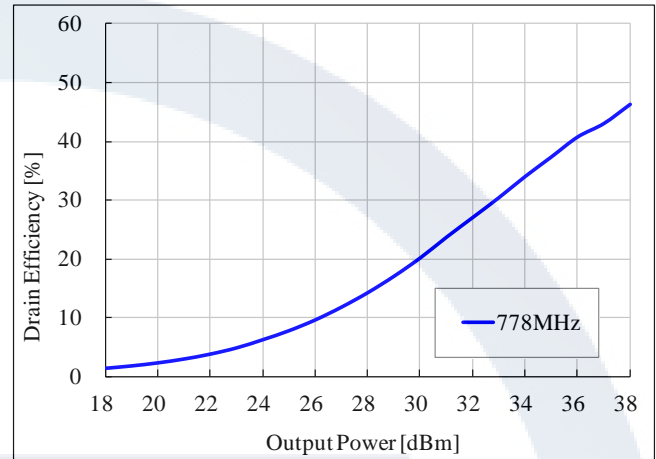
Performance Charts

* **Bias condition** @ Drive $I_{dq}=180\text{mA}$, Carrier $I_{dq}=120\text{mA}$, Peaking $I_{dq}=0\text{mA}$, $T_a=25^\circ\text{C}$

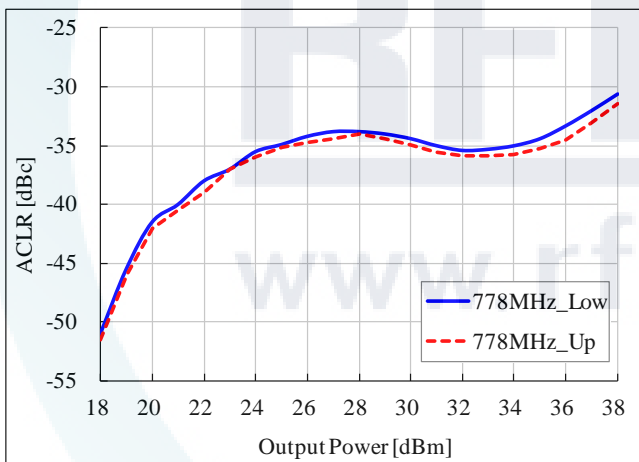
Power Gain vs. Output Power



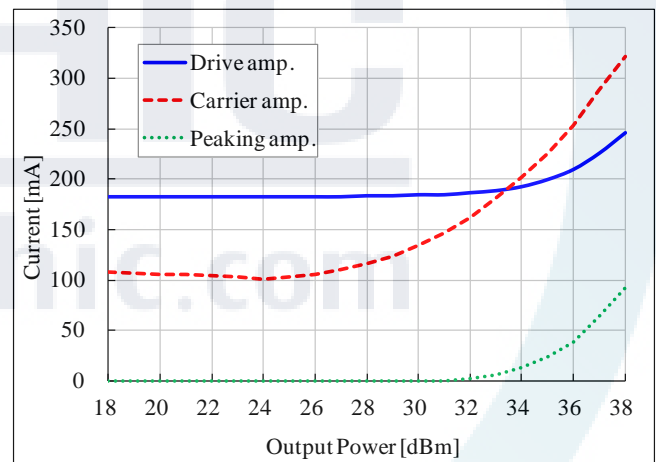
Drain Efficiency vs. Output Power



ACLR vs. Output Power

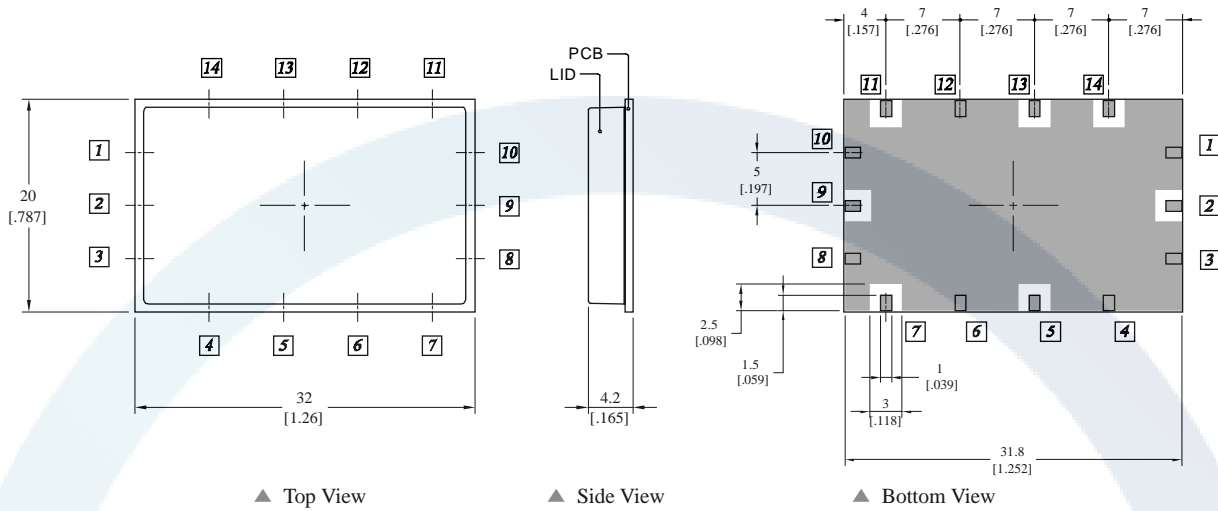


Current vs. Output Power



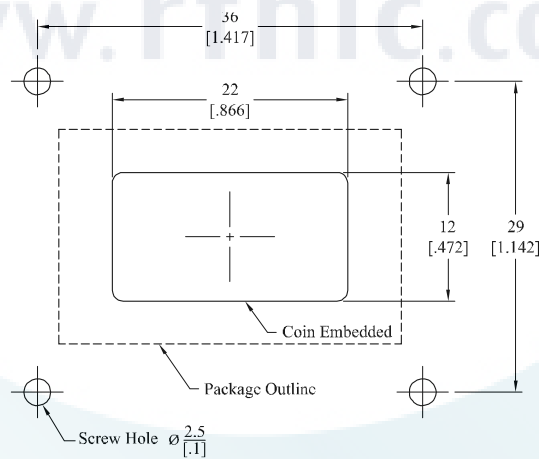
Package Dimensions (Type: SP-1E)

* Unit: mm[inch] | Tolerance: ± 0.15 [.006]



Pin Description (RTH07003-20D)							
Pin No	Function	Pin No	Function	Pin No	Function	Pin No	Function
1	GND	4	GND	8	GND	11	Vds2
2	RF In	5	Vgp	9	RF Out	12	GND
3	GND	6	GND	10	GND	13	Vgc
		7	Vds2			14	Vds1

Recommended Mounting Configuration



* Mounting Configuration Notes

- For the proper performance of the device, Ground / Thermal via holes must be designed to remove heat.
- To properly use heatsink, ensure the ground/thermal via hole region to contact the heatsink. We recommend the mounting screws be added near the heatsink to mount the board
- In designing the necessary RF trace, width will depend upon the PCB material and construction.
- Use 1 oz. Copper minimum thickness for the heatsink.
- Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink
- We recommend adding as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
- We recommend that the PCB with the RF device in a hybrid package(RTH Series) is not washed to remove the flux.

Ordering Information

Part Number	Package Design
RTH07003-20D	-R (Reel)
	-B (Bulk)
	-EVB (Evaluation Board)

Revision History

Part Number	Release Date	Version	Modification	Data Sheet Status
RTH07003-20D	2016.04.20	3.0	Electrical Specification (1p) Performance Charts (3p)	-
RTH07003-20D	2015.06.22	1.3	Electrical Specification	-
RTH07003-20D	2015.06.04	1.2	Electrical Specification Absolute Maximum Ratings	-



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