

# Quasi-Resonant Buck Controller for Precise Current Regulation and Wide Analog Dimming

## NCL30076

The NCL30076 is a DC–DC buck controller for wide dimming range down to 1% by analog dimming control to relieve audible noise and flicker in PWM dimming. ON Semiconductor’s proprietary LED current calculation technique driven by zero input offset amplifiers performs precise constant current in the whole analog dimming range. Multi–mode operation provides high efficiency with minimized switching loss by QR at heavy load and deep analog dimming by DCM at light load.

PWM dimming control is also provided in case that constant LED color temperature is required. The NCL30076 has several protections such as LED short protection, over current protection, thermal shutdown and VDD over voltage protection for robust system reliability.

### Features

- Wide Analog Dimming Range: 1~100%
- Low CC Tolerance:  $\pm 2\%$  at 100% Load &  $\pm 20\%$  at 1% Load
- Low System BOM
- LED Off Mode at Standby
- Low Standby Current
- PWM Dimming Available
- Gate Sourcing and Sinking Current of 0.5 A/0.8 A
- Robust Protection Features
  - ◆ LED Short Protection
  - ◆ Over Current Protection
  - ◆ Thermal Shutdown
  - ◆ V<sub>DD</sub> Over Voltage Protection

### Typical Applications

- LED Lighting System



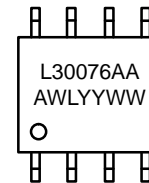
ON Semiconductor®

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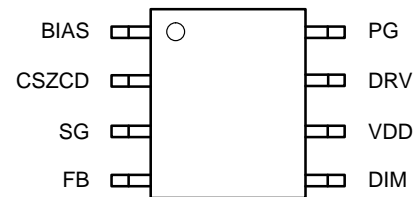
SOIC–8 NB  
CASE 751

### MARKING DIAGRAM



L30076 = Specific Device Code  
 AA = Default Trimming Option  
 A = Assembly Location  
 WL = Wafer Lot Traceability Code  
 YYWW = 4 Digit Data Code

### PIN ASSIGNMENT



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping
NCL30076AADR2G	SOIC–8 NB	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



# NCL30076

## PIN CONFIGURATION

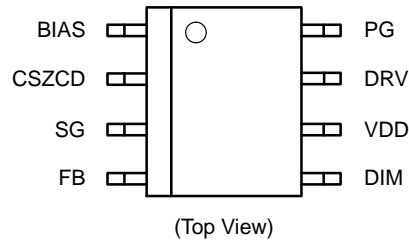


Figure 3. Pin Configuration

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	BIAS	3.3 V BIAS	This pin is 3.3 V LDO output to bias the internal digital circuit
2	CSZCD	CS and ZCD Sensing	This pin detects the switch current and the inductor current zero cross time
3	SG	Signal Ground	Signal Ground is close to control pin circuit such as CSZCD, DIM and FB
4	FB	Feedback	Output of feedback OTA
5	DIM	Dimming Input	Dimming signal is provided to this pin
6	VDD	Power Supply	IC operating current is supplied to this pin
7	DRV	Output Drive	This pin is connected to drive external switch
8	PG	Power Ground	Power Ground is close to the capacitors at BIAS and VDD pin

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## SPECIFICATIONS

### MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
VDD, DRV Pin Voltage Range	$V_{MV(MAX)}$	-0.3 to 30	V
DIM, FB, CSZCD, BIAS Pin Voltage Range	$V_{LV(MAX)}$	-0.3 to 5.5	V
Maximum Power Dissipation ( $T_A < 50^\circ\text{C}$ )	$P_{D(MAX)}$	550	mW
Maximum Junction Temperature	$T_{J(max)}$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 to 150	$^\circ\text{C}$
Junction-to-Ambient Thermal Impedance	$R_{\theta JA}$	145	$^\circ\text{C/W}$
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2	kV
ESD Capability, Charged Device Model (Note 2)	$ESD_{CDM}$	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
- This device series incorporates ESD protection and is tested by the following methods:
  - ESD Human Body Model per JEDEC Standard JESD22-A114
  - ESD Charged Device Model per JEDEC Standard JESD22-C101
  - Latch-up Current Maximum Rating  $\pm 100$  mA per JEDEC Standard JESD78

### RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Junction Temperature	$T_J$	-40	125	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### ELECTRICAL CHARACTERISTICS ( $V_{DD} = 15$ V and $T_J = -40$ ~ $125^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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#### VDD SECTION

IC Turn-On Threshold Voltage		$V_{DD(ON)}$	9.3	10.0	10.7	V
IC Turn-Off Threshold Voltage		$V_{DD(OFF)}$	7.4	8.0	8.6	V
Startup Current	$V_{DD} = V_{DD(ON)} - 1.6$ V	$I_{DD(ST)}$	-	250	400	$\mu\text{A}$
Operating Current		$I_{DD(OP)}$	-	6.5	8.0	mA
Standby Current		$I_{DD(SB)}$	-	200	300	$\mu\text{A}$

#### BIAS SECTION

BIAS Voltage		$V_{BIAS}$	3.23	3.30	3.37	V
	$T_J = 25$ ~ $100^\circ\text{C}$ (Note 4)		3.25	3.30	3.35	

#### DIM SECTION

DIM Voltage for 100% $V_{REF}$	$V_{DIM} = 1.9$ V	$V_{DIM(REF-MAX)}$	1.755	1.80	1.845	V
DIM Voltage for 99% $V_{REF}$		$V_{DIM(MAX-EFF)}$	1.730	1.78	1.827	V
Standby Enabling DIM Voltage		$V_{DIM(SB-ENA)}$	50	75	100	mV
Standby Disabling DIM Voltage		$V_{DIM(SB-DIS)}$	60	100	140	mV
Standby Delay Time		$t_{SB(DELAY)}$	9	10	11	ms

# NCL30076

## ELECTRICAL CHARACTERISTICS ( $V_{DD} = 15\text{ V}$ and $T_J = -40\text{--}125^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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### FB SECTION

FB OTA Source Current	$I_{FB} = (V_{LED} - V_{REF}) \times g_{M(FB)} \times 10$ $V_{REF} = 150\text{ mV}, V_{LED} = 100\text{ mV}$	$I_{FB(SOURCE)}$	-14.0	-11.5	-9.0	$\mu\text{A}$
FB OTA Sink Current	$I_{FB} = (V_{LED} - V_{REF}) \times g_{M(FB)} \times 10$ $V_{REF} = 50\text{ mV}, V_{LED} = 100\text{ mV}$	$I_{FB(SINK)}$	9.0	11.5	14.0	$\mu\text{A}$
FB OTA Transconductance	$g_{M(FB)} = I_{FB} / \{(V_{REF} - V_{LED}) \times 10\}$	$g_{M(FB)}$	18	23	28	$\mu\text{mho}$
FB OTA High Voltage	$V_{REF} = 150\text{ mV}, V_{LED} = 100\text{ mV}$	$V_{FB(HIGH)}$	4.7	-	-	V
FB Minimum Clamping Voltage	$V_{REF} = 0\text{ mV}, V_{LED} = 100\text{ mV}$	$V_{FB(CLP)}$	0.4	0.5	0.6	V

### CS SECTION

CS Regulation		$V_{CS(REG-MAX)}$	155	160	165	mV
CS Current Limit Maximum		$V_{CS(LIM-MAX)}$	390	410	430	mV
CS Current Limit Minimum		$V_{CS(LIM-MIN)}$	145	155	165	mV

### DUTY SECTION

Leading Edge Blanking Time at Turn-on		$t_{LEB(TON)}$	360	400	440	ns
Maximum Ton Time		$t_{ON(MAX)}$	45	50	55	$\mu\text{s}$
Minimum Toff Time	$V_{FB} = 3.8\text{ V}$	$t_{OFF(MIN)}$	900	1250	1500	ns
Maximum Toff Time	$V_{FB} = 0.5\text{ V}$	$t_{OFF(MAX)}$	1.17	1.30	1.43	ms
Maximum FB Voltage for Min. Toff		$V_{FB(MAX-TOFF)}$	3.30	3.43	3.55	V
Minimum FB Voltage for Max. Toff		$V_{FB(MIN-TOFF)}$	0.9	1.1	1.3	V
Quasi-Resonant Delay Time		$t_{QR}$	0.45	0.50	0.55	$\mu\text{s}$

### DRV SECTION

DRV Low Voltage		$V_{DRV(LOW)}$	-	-	0.2	V
DRV High Voltage	$V_{DD} = 15\text{ V}$	$V_{DRV(HIGH)}$	11	12	13	V
DRV Rising Time	$C_{DRV} = 3.3\text{ nF}$	$t_{DRV(R)}$	60	100	145	ns
DRV Falling Time	$C_{DRV} = 3.3\text{ nF}$	$t_{DRV(F)}$	25	55	105	ns

### AUTO RESTART SECTION

Auto Restart Time at Protection		$t_{AR(PROT)}$	0.9	1.0	1.1	s
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### VDD OVER VOLTAGE PROTECTION SECTION

VDD Over Voltage Threshold Voltage		$V_{DD(OVP)}$	22	23	24	V
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### OVER CURRENT PROTECTION SECTION

CS Over Current Protection Threshold		$V_{CS(OC)}$	0.9	1.0	1.1	V
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### THERMAL SHUTDOWN SECTION

Thermal Shut Down Temperature (Note 3)		$T_{SD}$	130	150	170	$^\circ\text{C}$
Thermal Shut Down Hysteresis (Note 3)		$T_{SD(HYS)}$	25	30	35	$^\circ\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.

4. Guaranteed by characterization.

TYPICAL CHARACTERISTICS

(These characteristic graphs are normalized at  $T_A = 25^\circ\text{C}$ )

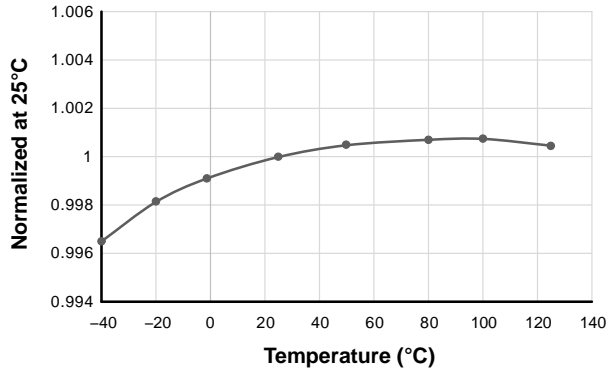


Figure 4.  $V_{BIAS}$  vs. Temperature

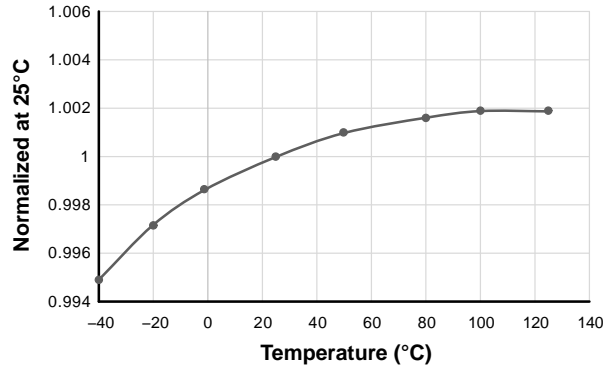


Figure 5.  $V_{DIM(MAX)}$  vs. Temperature

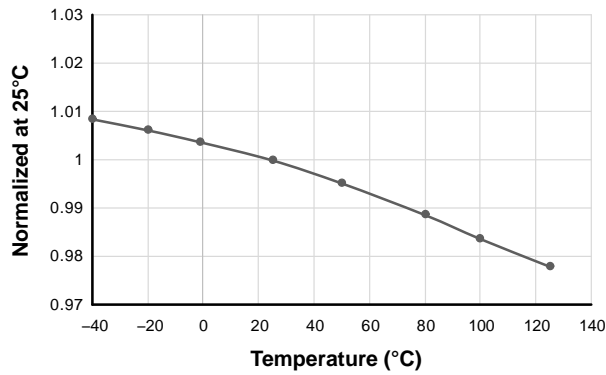


Figure 6.  $g_{M(FB)}$  vs. Temperature

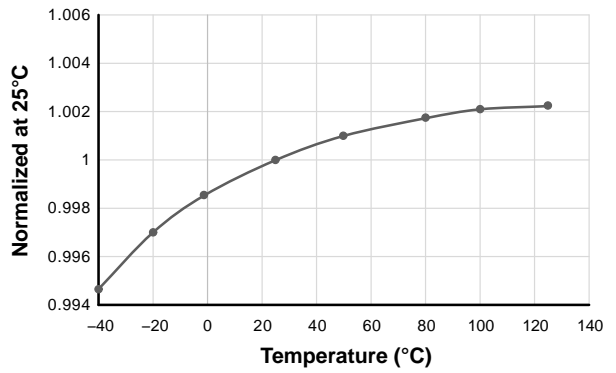


Figure 7.  $V_{CS(REG-MAX)}$  vs. Temperature

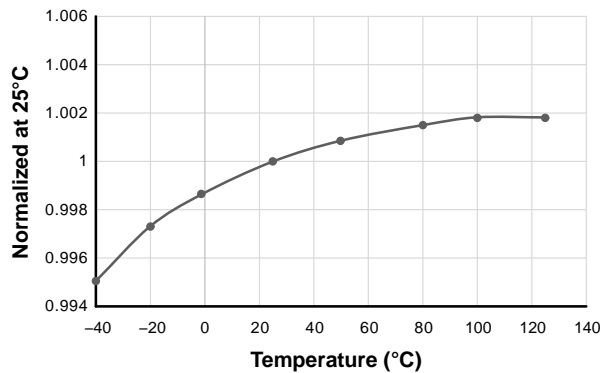


Figure 8.  $V_{CS(LIM-MIN)}$  vs. Temperature

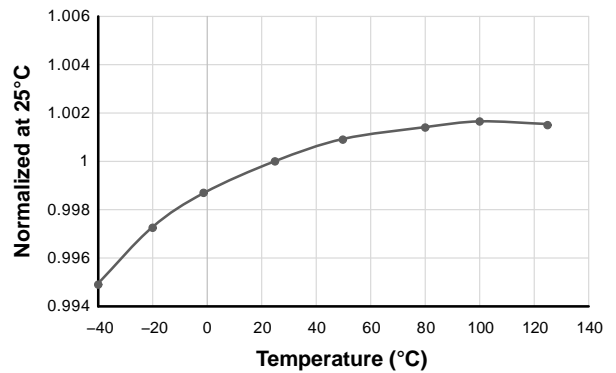


Figure 9.  $V_{DD(OVP)}$  vs. Temperature

## APPLICATION INFORMATION

### General

NCL30076 provides wide analog dimming down to 1% with accurate CC regulation. According to buck inductor, input voltage and output voltage, deep dimming down to 0.1~0.2% load can be achieved. Thanks to ON Semiconductor's proprietary LED current calculation technique, NCL30076 is able to sense the current of LED load connected at input voltage node with no upper limit of the input voltage with high design flexibility and system reliability. LED current sensed by internal zero input offset amplifiers performs accurate CC regulation in the whole analog dimming range. Therefore, CC tolerance is tightly controlled within  $\pm 2\%$  at 100% load and  $\pm 20\%$  at 1% load.

### Wide Analog Dimming

Wide analog dimming range is obtained by transitioning multi-mode operation between QR and DCM according to the dimming condition. At full load condition, QR with valley switching minimizes switching loss for high system efficiency and DCM is activated at light load condition to perform deep analog dimming. Internal LED current calculator and a digital compensator provide dimming linearity over the entire dimming range.

### PWM Dimming

Analog dimming has benefits for less audible noise and flicker compared to PWM dimming. However, PWM dimming method is generally required to keep the constant LED color temperature in specific applications. NCL30076 supports PWM dimming by simply providing PWM dimming signal to DIM pin.

### Precise CC Regulation

CC regulation is very important especially in programmable LED driver system to keep constant LED current under system variation of LED load, inductor, temperature, etc. NCL30076 applies zero input offset amplifiers at LED current calculator and OTA. Those blocks can implement precise LED current sensing and FB voltage generation.

Therefore, NCL30076 supports low CC tolerance less than  $\pm 2\%$  at full load and  $\pm 20\%$  at 1% load in the system variation.

### Soft start

At startup, an internal soft start block gradually reduces  $T_{OFF}$  time from maximum  $T_{OFF}$  limit so that LED current is settled smoothly without overshoot current and unexpected flash.

### Standby Mode

When  $V_{DIM}$  is lower than a standby threshold voltage for 10 ms, standby mode is triggered with LED turn-off and IC current consumption is minimized.

### Auto Restart (AR) at Protection

Once protection is triggered, IC operation stops for 1 second and begins soft start operation after the auto restart time delay.

### VDD Over Voltage Protection (OVP)

When VDD is higher than  $V_{DD(OVP)}$  threshold, over voltage protection is triggered.

### Short LED Protection (SLP)

When LED is short circuited, the buck stage operates at minimum switching frequency, so the maximum turn-off time control protects the freewheeling diode from thermal stress.

### Over Current Protection (OCP)

When CSZCD voltage exceeds the over current threshold voltage, switching is immediately shut down after leading edge blanking time in the short circuit condition of the inductor or the freewheeling diode.

### Thermal Shot Down (TSD)

When IC junction temperature is higher than  $150^{\circ}\text{C}$ , TSD is triggered and released when the temperature is lower than  $120^{\circ}\text{C}$ .

BASIC OPERATION

NCL30076 is the current mode buck controller in which DRV is off when  $V_{CSZCD}$  reaches to  $V_{CS.LIM}$  and DRV is on by inductor current zero cross signal ( $V_{TOFF.ZCD}$ ) in QR and  $T_{OFF.FB}$  generator output ( $V_{TOFF.FB}$ ) in DCM as shown in Figure 10.  $V_{LED}$  is calculated based on  $V_{CSZCD}$  in precise LED current calculator block composed of zero input offset amplifiers and  $V_{REF}$  is controlled by DIM signal by below equation.

$$V_{REF} [V] = \frac{V_{DIM} - 0.2 V}{10} \quad (eq. 1)$$

$V_{LED}$  is compared with  $V_{REF}$  by OTA to generate  $V_{FB}$ .  $V_{FB}$  sets  $V_{CS.LIM}$  as below equation.

$$V_{CS.LIM} [V] = \frac{V_{FB}}{10} + 37.5 mV \quad (eq. 2)$$

$V_{FB}$  also controls  $V_{TOFF.FB}$  signal by  $T_{OFF.FB}$  generator in which  $V_{TOFF.FB}$  is triggered at  $T_{OFF.FB}$  after DRV is turned off.

$$T_{OFF.FB} [\mu s] = \frac{2.7}{V_{FB} - 1.1} + 0.1 \quad (eq. 3)$$

When  $V_{CSZCD}$  drops after the inductor current zero cross, IC counts  $t_{QR}$  (0.5  $\mu s$ ) and trigger  $V_{TOFF.ZCD}$ . In QR mode,  $V_{TOFF.ZCD}$  signal is generated later than  $V_{TOFF.FB}$  signal and DRV on is determined by  $V_{TOFF.ZCD}$  for valley switching. In DCM mode, DRV on is set by  $V_{TOFF.FB}$  as  $T_{OFF.FB}$  is longer than  $V_{TOFF.ZCD}$  triggering time.

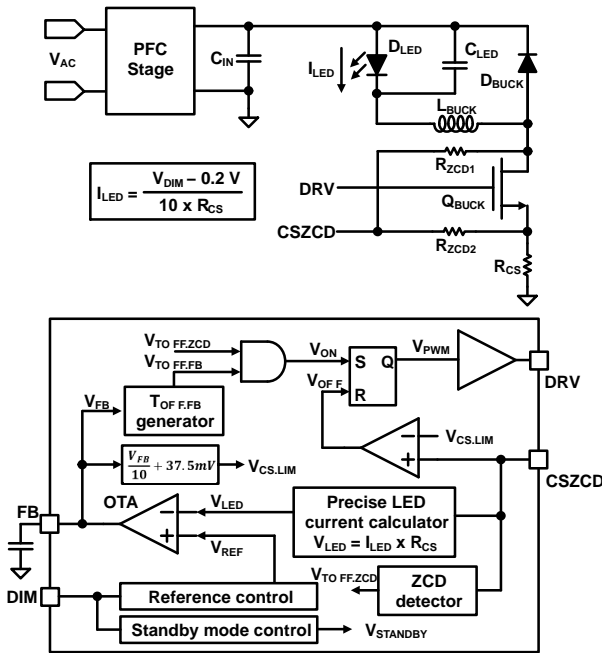


Figure 10. NCL30076 Block Diagram

Wide Analog Dimming

NCL30076 operates in QR at full load and in DCM at light load for a wide dimming range. Figure 11 shows how NCL30076 operates with  $V_{DIM}$ .

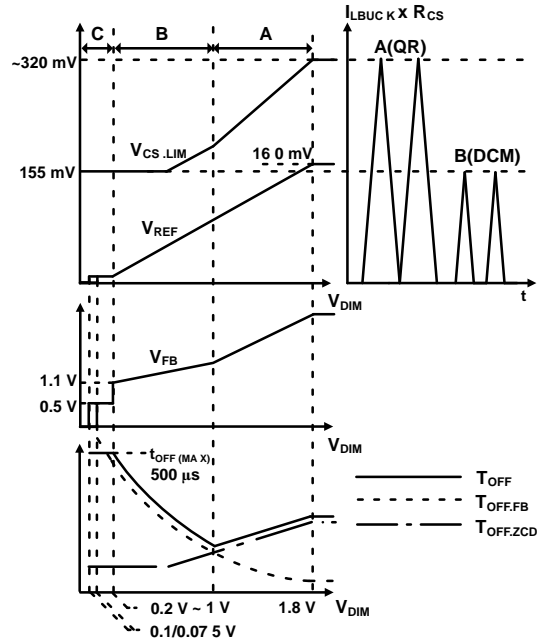


Figure 11. Operation Mode vs.  $V_{DIM}$

- **A:**  $V_{FB}$  controls  $V_{CS.LIM}$  and  $T_{OFF}$  is determined by  $T_{OFF.ZCD}$  with QR switching as  $T_{OFF.ZCD}$  is longer than  $T_{OFF.FB}$ .
- **B:** Operating mode is transitioned from QR to DCM at the boundary between A and B region which is approximately half load.  $T_{OFF}$  is determined by  $T_{OFF.FB}$  as  $T_{OFF.FB}$  is longer than  $T_{OFF.ZCD}$ . When  $V_{DIM}$  is further reduced,  $V_{CS.LIM}$  is no longer controlled by  $V_{FB}$  and clamped to minimum  $V_{CS.LIM}$  (155 mV).
- **C:** When  $V_{DIM}$  is lower than 0.2 V,  $V_{REF}$  is set to 0 V and  $V_{FB}$  is pulled down to 0.5 V clamping voltage with min. LED current under open loop control. When  $V_{DIM}$  is lower than 0.075/0.1 V, standby mode is triggered with LED turn-off.

Precise CC Regulation

Current sensing amplifier and OTA applies zero input offset compensation technique for precise CC regulation and dimming curve linearity in multi-mode operation

Table 1 shows CC tolerance measured by changing inductor ( $\pm 15\%$ ), temperature ( $-10, 25, 90^\circ C$ ), output voltage (100, 200, 300 V) and controller 150 pcs (3 lot variation) in 400 V input 100 W driver. As a result, CC tolerance with system variables at 1% deep dimming condition is less than  $\pm 26\%$  and less than  $\pm 3.0\%$  at full load condition.

Table 1. CC TOLERANCE (150 pcs)

Inductor : ±15% Temp. : -10 / 25 / 90 °C	100% Load	50% Load	10% Load	5% Load	2% Load	1% Load
V <sub>OUT</sub> : 100 V	1.99	3.77	4.41	5.32	9.22	16.23
V <sub>OUT</sub> : 200 V	1.83	3.70	4.76	5.23	8.64	14.44
V <sub>OUT</sub> : 300 V	1.86	3.06	4.33	5.80	10.57	20.54*
V <sub>OUT</sub> : 100 / 200 / 300 V	2.29	4.10	5.45	6.94	13.48	25.38*

\*The main deviation factor is high temperature condition. The Total CC tolerance at 1% deep dimming condition without high temperature condition is less than 20%.

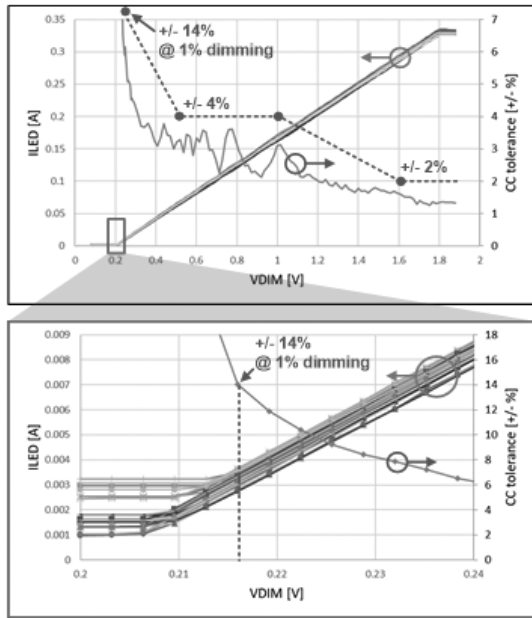


Figure 12. NCL30076 Dimming Curve and CC Tolerance

**Standby Mode**

Standby mode is triggered by V<sub>DIM</sub> as shown in Figure 13.

- **A:** When V<sub>DIM</sub> is lower than V<sub>DIM(SB-ENA)</sub>, DRV is shut down. So, LED lamps turn off.
- **B:** After t<sub>SB(DELAY)</sub> (10 ms), standby mode is entered and NCL30076 current consumption drops to I<sub>DD(SB)</sub>.
- **C:** When V<sub>DIM</sub> is higher than V<sub>DIM(SB-DIS)</sub>, standby mode is immediately terminated and IC starts up.

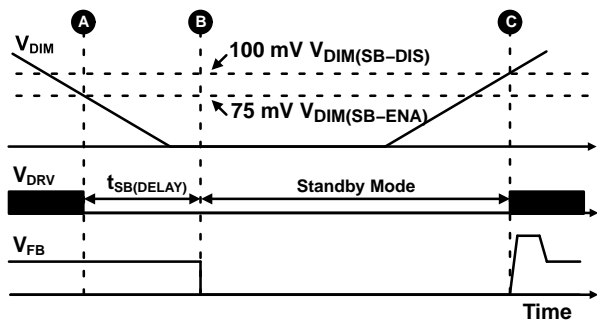


Figure 13. NCL30076 Standby Mode

**Soft Start**

During soft start operation, Internal soft start counter T<sub>OFF.SS</sub> contributes to T<sub>OFF</sub> by reduced from t<sub>OFF(max)</sub>. When T<sub>OFF.SS</sub> reaches to the steady state level, V<sub>FB</sub> is settled to regulation level and T<sub>OFF</sub> is finally decided to T<sub>OFF.FB</sub> or T<sub>OFF.ZCD</sub> by load condition. In the end of the soft start time, T<sub>OFF.SS</sub> reaches to 0 and doesn't affect T<sub>OFF</sub> control anymore. Figure 14 shows how the soft start operates at full load condition where T<sub>OFF.FB</sub> is not engaged as T<sub>OFF</sub> is set by T<sub>OFF.ZCD</sub> in QR mode.

- **A:** T<sub>OFF</sub> is determined by T<sub>OFF.SS</sub> which is reduced from t<sub>OFF(MAX)</sub>. V<sub>FB</sub> is pulled up and the system operates in DCM mode.
- **B:** T<sub>OFF</sub> is controlled by T<sub>OFF.ZCD</sub> as T<sub>OFF.SS</sub> is shorter than T<sub>OFF.ZCD</sub>. V<sub>LED</sub> is closer to V<sub>REF</sub>, and V<sub>FB</sub> starts falling.
- **C:** V<sub>FB</sub> is settled in regulation level and steady state starts.

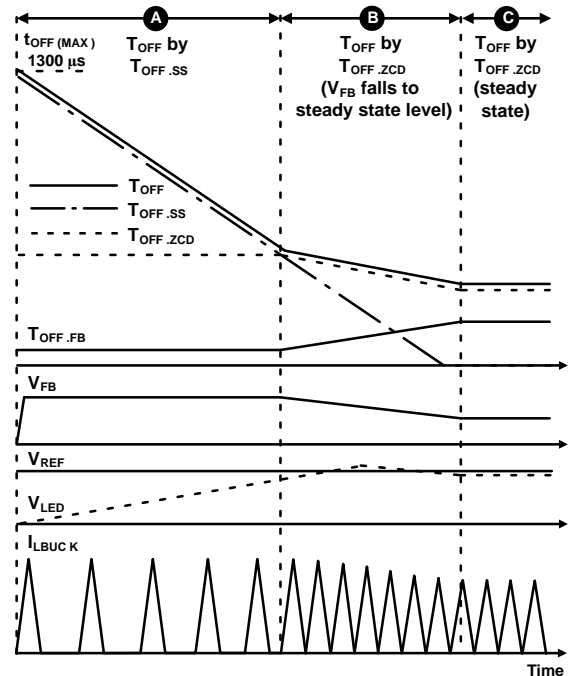


Figure 14. Soft Start Sequence (Full Load Startup in QR)

### Protections

- **VDD Over Voltage Protection (OVP)**  
When VDD is higher than  $V_{DD(OVP)}$  (23 V), VDD OVP is triggered with 1 sec AR timer. Open LED protection can be implemented by VDD OVP when VDD is supplied by auxiliary winding in the buck inductor.
- **Over Current Protection (OCP)**  
When CSZCD voltage is higher than  $V_{CS(OCP)}$  (1 V) after leading edge blanking time,  $t_{LEB(TON)}$  (400 ns), IC immediately shuts down with 1 sec AR timer.
- **Short LED Protection (SLP)**  
When LED load is short-circuited,  $T_{OFF}$  is lengthened to 1300  $\mu$ s,  $t_{OFF(MAX)}$  due to the absence of zero cross detection. Therefore, max.  $T_{OFF}$  control protects the freewheeling diode from thermal stress and the diode current is regulated close to the LED current set by  $V_{DIM}$ .
- **Thermal Shut Down (TSD)**  
When the junction temperature is higher than  $T_{SD}$ , the system shuts down and the junction temperature is monitored at every 1 second AR delay time. When the temperature is lower than  $T_{SD} - T_{SD(HYS)}$ , the system restarts.

APPENDIX: DIMMING CURVE AND CC TOLERANCE WITH SYSTEM VARIABLES

- System: NCL30076 100 W ( $V_{IN}$ : 400 V /  $V_{OUT}$ : 100 ~ 300 V /  $I_{OUT(MAX)}$ : 333 mA)
- Temperature variation: -10 / 25 / 90 °C
- Inductance variation:  $\pm 15\%$  (1.36 mH ~ 1.84 mH)
- Output Voltage: 100 / 200 / 300 V
- NCL35076 Controller: 150 pcs (3 lot variation)

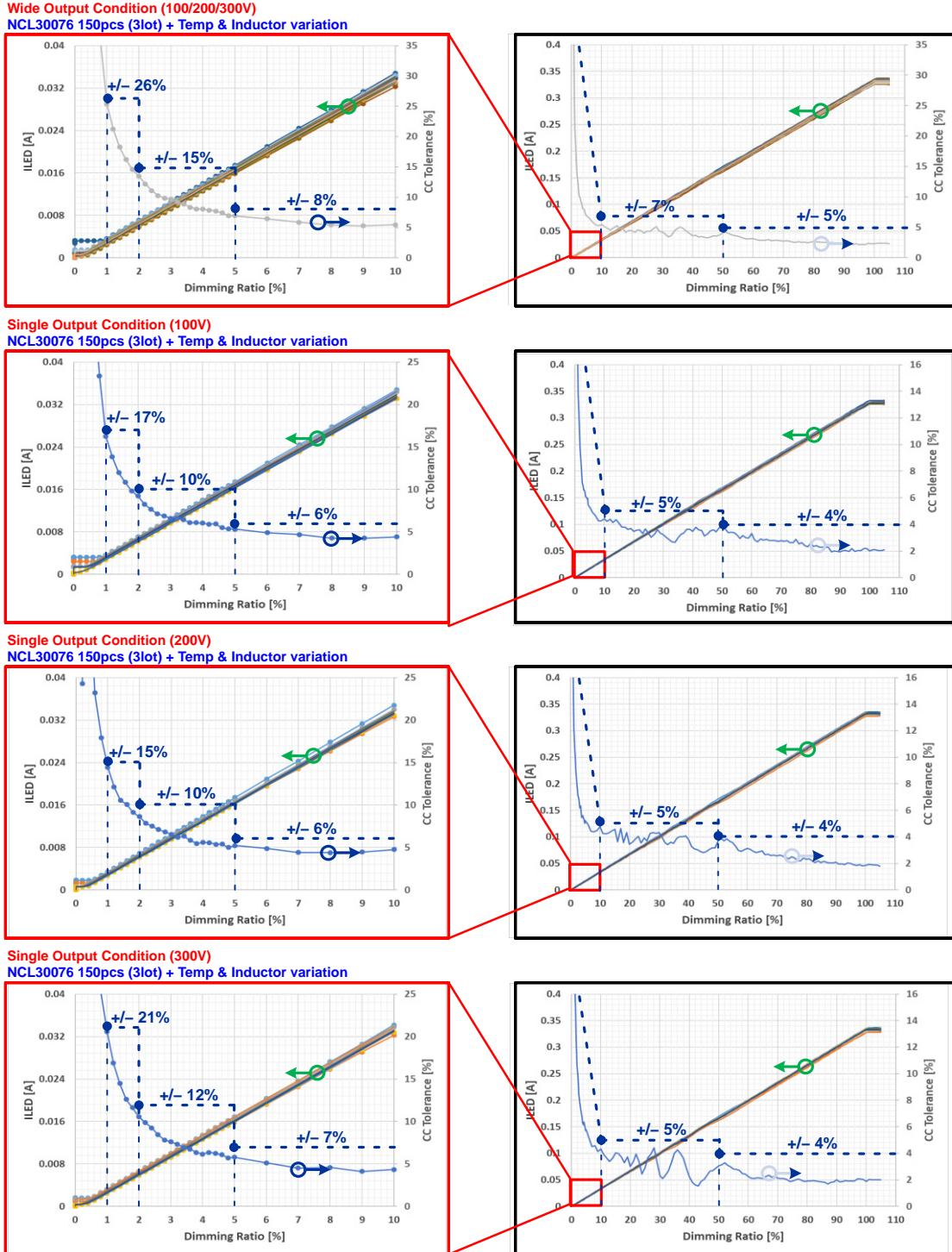
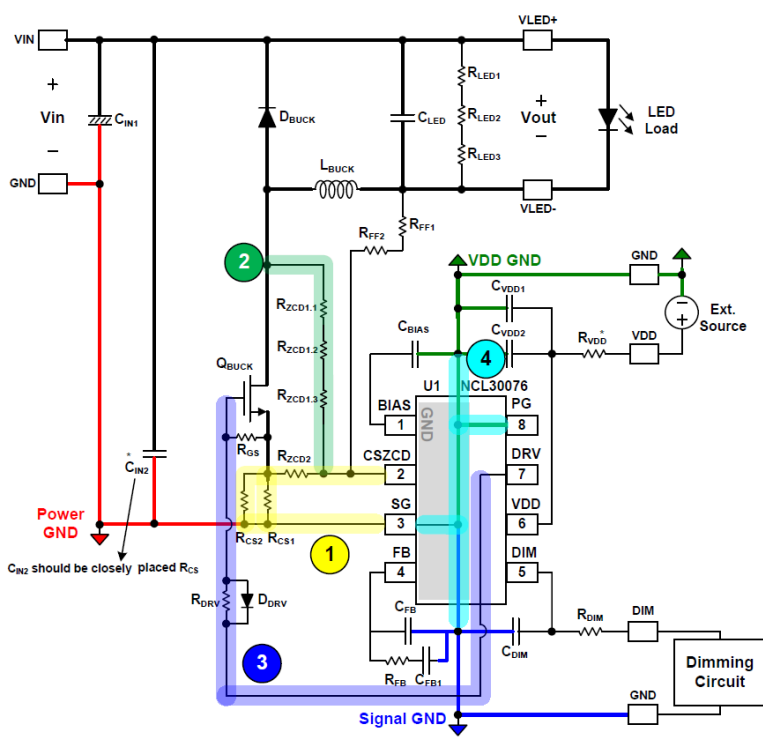


Figure 15. CC Tolerance (150 pcs)

PCB LAYOUT GUIDANCE



**Layout guidance 1**

Current sensing path (CSZCD - RZCD2 - RCs - SG) should be **short**. This path and IC should be **away** from L<sub>BUCK</sub>.

**Layout guidance 2**

1. CSZCD node should be **away** from Drain node.  
2. R<sub>ZCD1</sub> resistors should be **close** each other.

Series	Zigzag	90° angle

3. R<sub>ZCD1</sub> type guidance  
- Three 1206 (3216) SMD resistors  
- Two axial resistor

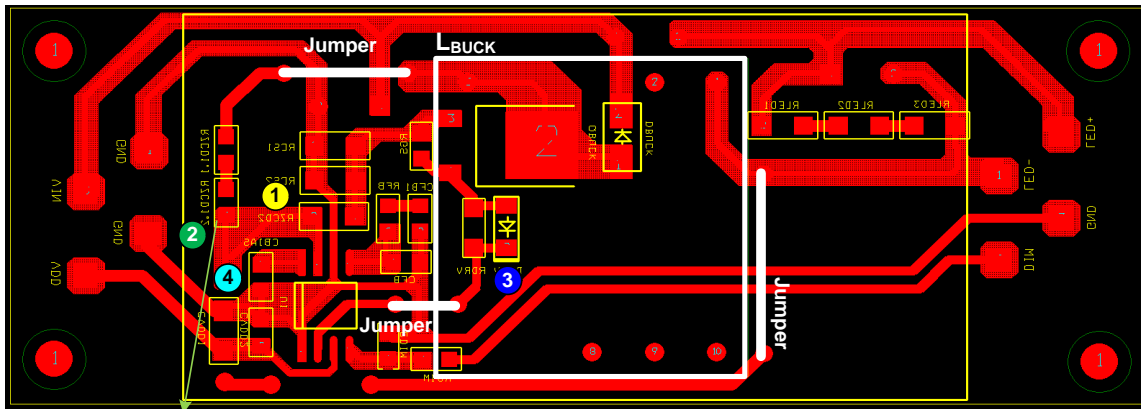
**Layout guidance 3**

FB and DIM node should be **away** from DRV node

**Layout guidance 4**

BIAS and VDD circuits are connected to VDD GND (= PG pin).  
FB and DIM circuits are connected to Signal GND.  
VDD GND and Signal GND join at the bottom of IC with SG connection.

**\* Important!!**  
RVDD and CIN2 must be added for improving switching noise immunity

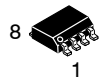


\* RZCD1 should be properly selected according to rated voltage.

Figure 16. Layout Guidance

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

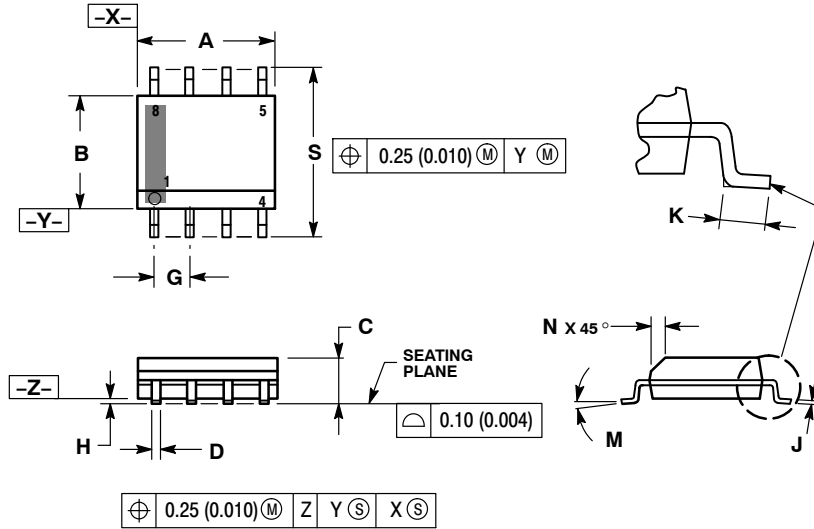
ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

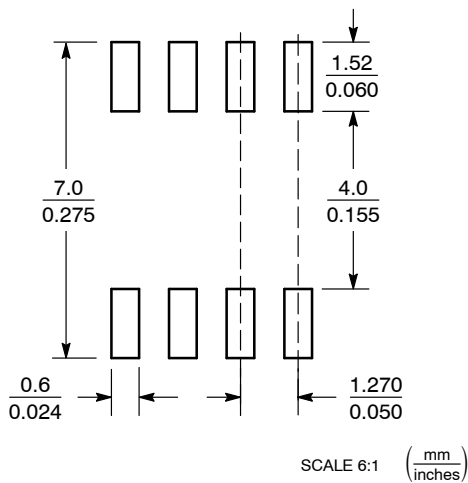
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

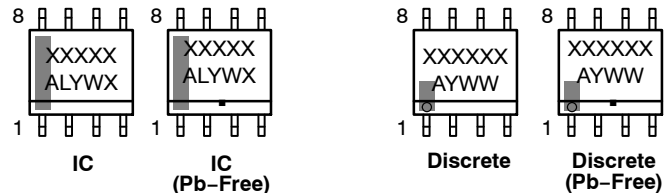
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p><b>STYLE 2:</b><br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p><b>STYLE 6:</b><br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p><b>STYLE 7:</b><br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p><b>STYLE 11:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p><b>STYLE 14:</b><br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p><b>STYLE 18:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p><b>STYLE 19:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p><b>STYLE 26:</b><br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p><b>STYLE 27:</b><br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p><b>STYLE 28:</b><br/>         PIN 1. SW_TO_GND<br/>         2. DASIC OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p><b>STYLE 29:</b><br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |   |   |

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