SRPE-30E1A0

Non-Isolated DC-DC Converter

The Bel SRPE-30E1A0 is part of the non-isolated DC-DC converter power module series. The module uses a vertical SMT package. This converter is available in a range of output voltages from 0.6 VDC to 2.0 VDC over a wide range of input voltage (Vin = 4.5 – 13.2 VDC).

Key Features & Benefits

- 4.5 – 13.2 VDC Input
- 0.6 – 2.0 VDC / 30 A Output
- Non-Isolated
- Wide Output Trim Range
- Fixed Frequency
- Output Over-Voltage Shutdown
- High Efficiency
- OCP/SCP
- High Power Density
- Power Good Signal
- Overtemperature Shutdown
- Remote Sense
- Wide Input Voltage Range
- Remote On/Off
- Low Cost
- Under-Voltage Lockout
- Wide Operating Temperature Range (0 °C - 50 °C)
- Class II, Category 2, Non-Isolated DC/DC Converter (refer to IPC-9592B)

RoHS Compliant

Applications

- Networking
- Computers and Peripherals
- Telecommunications

1. MODEL SELECTION

MODEL NUMBER	OUTPUT VOLTAGE	INPUT VOLTAGE	MAX. OUTPUT CURRENT	MAX. OUTPUT POWER	TYPICAL EFFICIENCY
SRPE-30E1A0G SRPE-30E1A0R	0.6 – 2.0 VDC	4.5 - 13.2 VDC	30 A	60 W	91.5%

PART NUMBER EXPLANATION

S	R	PE	-	30	E	1A	0	x
Mounting Type	RoHS Status	Series Name		Output Current	Input Range	Output Voltage	Active Logic	Package
Surface Mount	RoHS	SMD SIP		30 A	4.5 - 13.2 V	0.6 - 2.0 V	Active High	G – Tray Package R – Tape and Reel Package

2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
Continuous non-operating Input Voltage		-0.3	-	15	V
Output Enable Terminal Voltage		-0.3	-	15	V
Ambient Temperature		0	-	50	°C
Storage Temperature		-40	-	125	°C
Altitude		-	-	2000	m

NOTE: Ratings used beyond the maximum ratings may cause a reliability degradation of the converter or may permanently damage the device.

3. INPUT SPECIFICATIONS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Input Voltage		4.5	12	13.2	V
Input Current (full load)		-	-	15.0	A
Input Current (no load)	All Vin, Vout = 0.6 V, at Ta = 25°C.	-	20	35	mA
	All Vin, Vout = 1.2 V, at Ta = 25°C.	-	35	50	
	All Vin, Vout = 2.0 V, at Ta = 25°C.	-	45	70	
Remote Off Input Current		-	100	150	mA
Input Reflected Ripple Current (rms)	Vout = 2.0 V, Iout = 30 A. With simulated source impedance of 1 µH, 5 Hz to 20 MHz. Use	-	-	30	mA
Input Reflected Ripple Current (pk-pk)	100 µF/100 V electrolytic capacitors with ESR < 0.2 ohm max @ 25°C.	-	-	100	mA
Turn-on Voltage Threshold	Ta = 20 - 50°C	3.8	4.3	5	V
	The turn on voltage should not be less than 7 V when Ta = 0 - 20°C.	7	8	9	V
Turn-off Voltage Threshold		3.8	4.1	4.5	V

NOTE: All specifications are typical at 25 °C unless otherwise stated

4. OUTPUT SPECIFICATIONS

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
Output Voltage Set Point	Vo,set ≥ 0.9 VDC	Setpoint test condition: Vin = 12 V, Iout = half load, Ta = 25°C	-2	-	2	%Vo,set
	Vo,set < 0.9 VDC		-3	-	3	
Load Regulation		Vin = 38 – 55 V, Io = 100% load	-	25	40	mV
Line Regulation		Vin = 42/50 V, Io = 0~100% load (The output droop voltage from no load to full load is about 0.6 V).	-	0.6	0.65	V
Regulation Over Temperature			-2	-	2	%Vo,set
Output Ripple and Noise (pk-pk)		Condition: Vin = 12 V, Iout = full load, Ta = 25°C; measured with a 10 µF+7*100 µF ceramic cap and 3*470 µF POSCAP ESR ≤ 12 m ohm at output.	-2	-	2	%Vo,set
Output Ripple and Noise (rms)			-	±3	-	%Vo,set
Output Current Range			-	-	30	mV
Output DC Current Limit			-	-	5	mV
Turn On Time			-	-	5	ms
Overshoot at Turn On			-	0	5	%
Output Capacitance			470	-	9000	µF
TRANSIENT RESPONSE						
△V 50% ~ 75% of Max Load	Overshoot	Vin = 12 V, Vout = 2.0 V, di/dt = 2.5 A/µs. Measured with a 10 uF+7*100 µF ceramic cap and 3*470 µF POSCAP ESR ≤ 12m ohm at output.	-	40	60	mV
	Settling Time		-	20	50	µs
△V 75% ~ 50% of Max Load	Overshoot		-	40	60	mV
	Settling Time		-	20	50	µs

NOTE: All specifications are typical, at 25°C unless otherwise stated.

5. GENERAL SPECIFICATIONS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Efficiency	Vo = 0.6 V, TA = 25°C	79	80	-	%
	Vo = 1.2 V, TA = 25°C	86	87.7	-	
	Vo = 2.0 V, TA = 25°C	90	91.5	-	
Switching Frequency		-	500	-	kHz
Over Temperature Protection		-	125	-	°C
Output Voltage Trim Range (Wide Trim)	This voltage is achieved by trimming up output slowly.	0.6	-	2	V
Weight		-	10.4	-	g
MTBF	Calculated Per Telcordia SR-332, Issue 3 (Vin = 12 V, Vo = 0.9 V, Io = 30 A, T a= 40°C， with 300 LFM, FIT = 10^9/MTBF)	-	71.7	-	Mhrs
FIT		-	13.9	-	-
Dimensions (L × W × H)			1.20 x 0.59 x 0.65		inch
			30.48 x 15.00 x 16.51		mm

NOTE: All specifications are typical, at 25°C unless otherwise stated.

6. REMOTE ON/OFF

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Signal Low (Unit Off)	Remote On/Off pin open, unit off.	0	-	1.5	V
Signal High (Unit On)		1.8	-	15	V

7. EFFICIENCY DATA

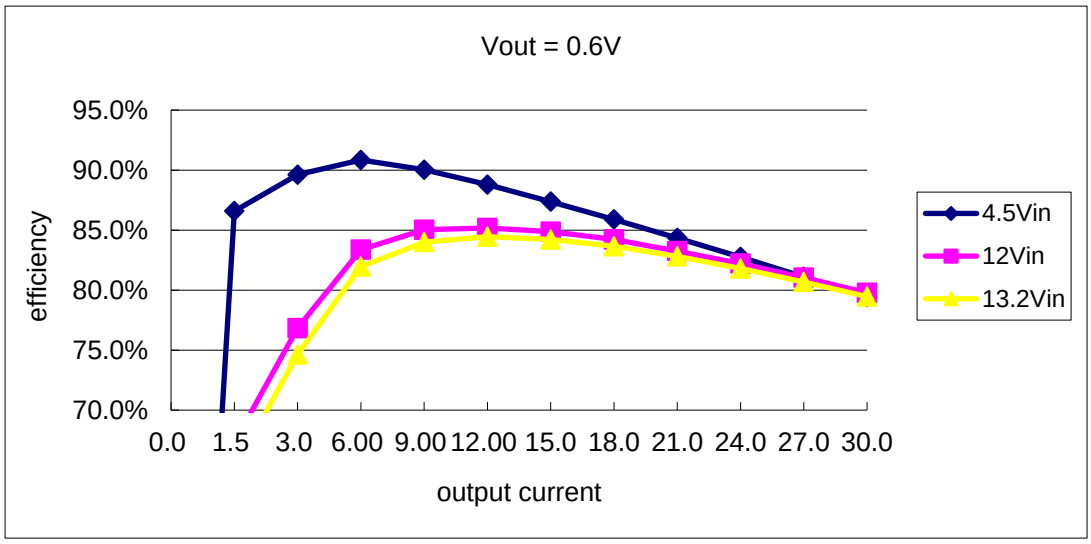

Figure 1. Efficiency @ Vo = 0.6 V

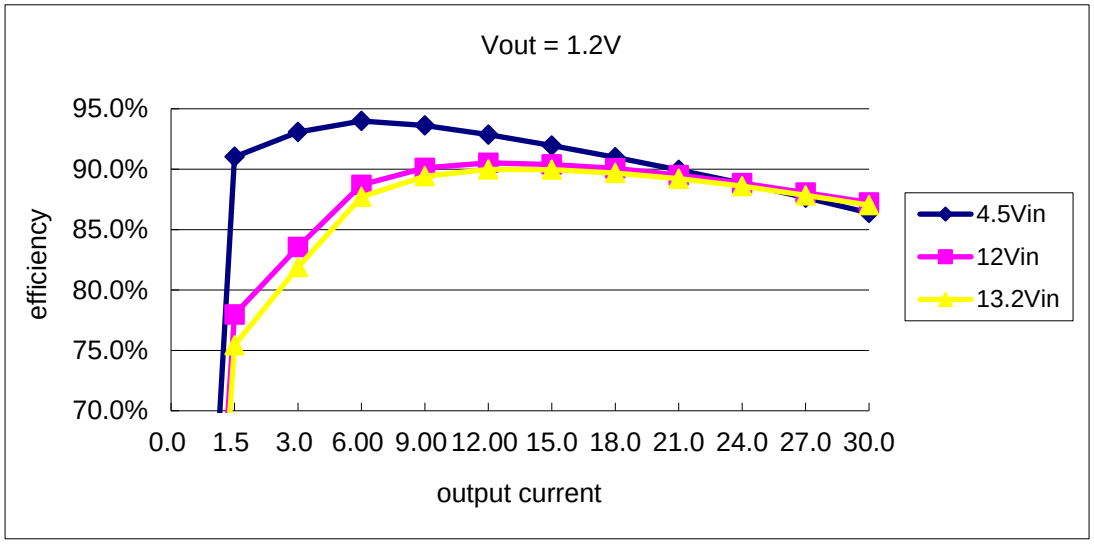

Figure 2. Efficiency @ Vo = 1.2 V

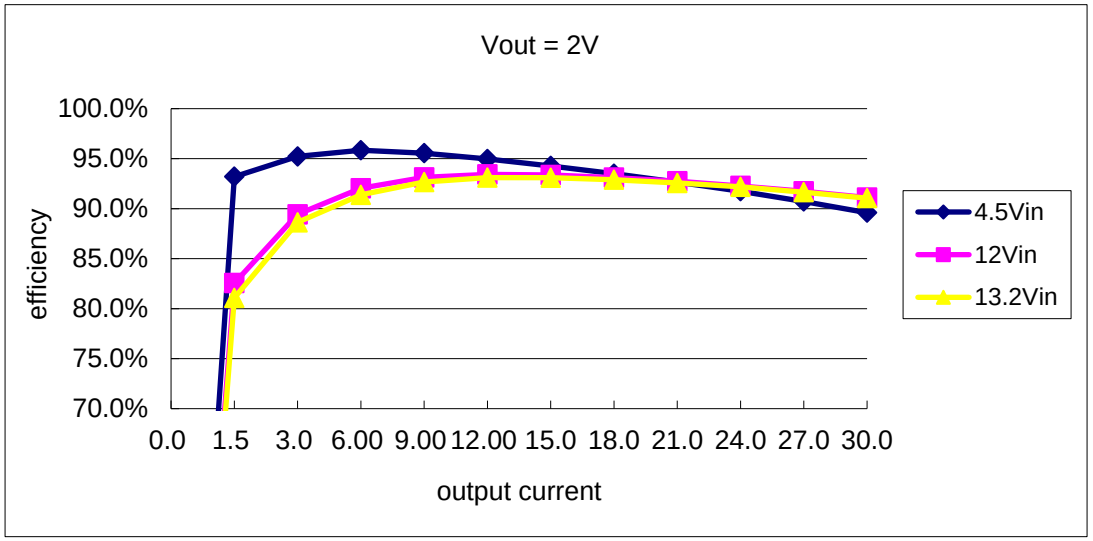

Figure 3. Efficiency @ Vo = 2.0 V

8. INPUT NOISE

Input Reflected Ripple Current

Testing setup

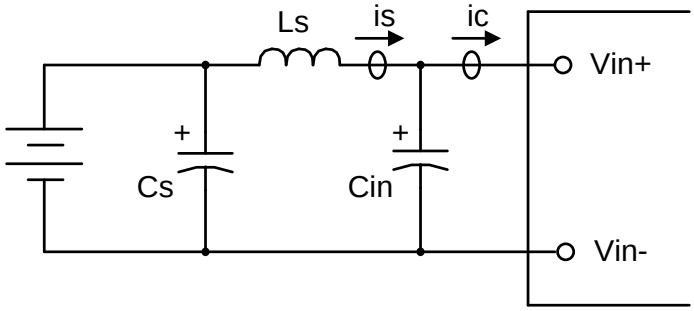

Figure 4. Test setup

Notes and values in testing:

is: Input Reflected Ripple Current
ic: Input Terminal Ripple Current
Ls: Simulated Source Impedance (1 µH)
Cs: Offset possible source Impedance (100 µF, ESR < 0.2 Ω @ 100 kHz, 20˚C)
Cin: Electrolytic capacitor, should be as close as possible to the power module to damp ic ripple current and enhance stability. Recommendation: 100 µF, ESR < 0.2 Ω @ 100 kHz, 20˚C.

Below measured waveforms are based on above simulated and recommended inductance and capacitance.

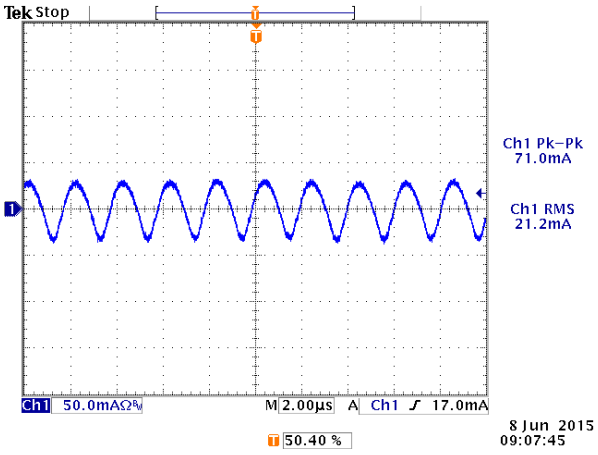

Figure 5. is (input terminal ripple current), AC component

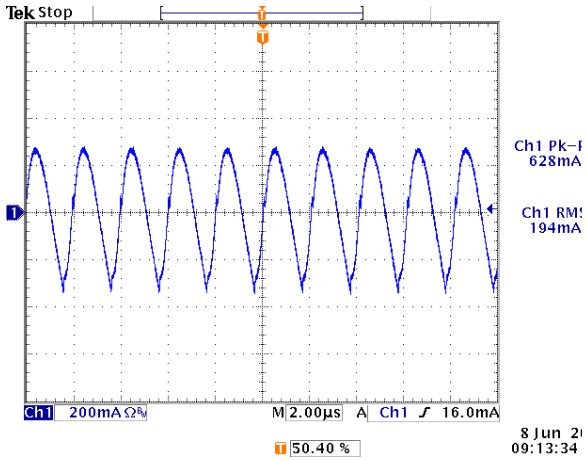

Figure 6. ic (input terminal ripple current), AC component

NOTE: Vin = 12 V, Vo = 2 V, Io = 30 A, with 1*10 µF ceramic and 1*470 µF polymer capacitor at the output, Ta = 25˚C.

9. THERMAL DERATING CURVES

Airflow direction, hot spot location and allowed maximum temperature:

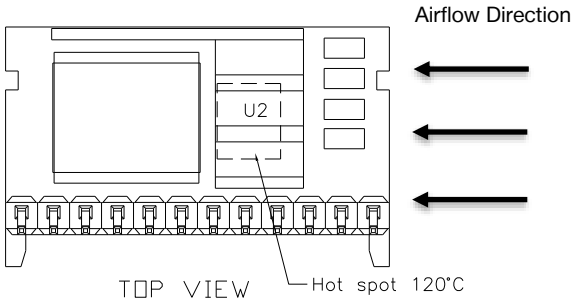

Figure 7. Airflow direction, Hot spot location and allowed maximum temperature

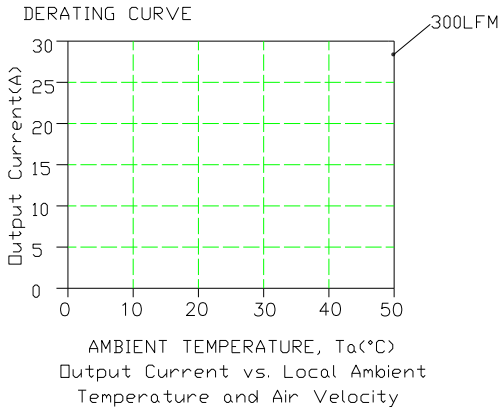

Figure 8. Vin = 12 V, .06 V≤ Vo < 1.2 V

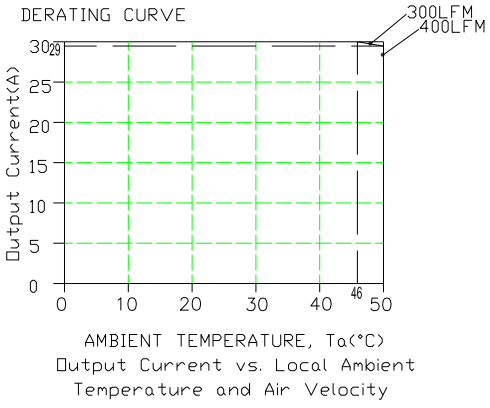

Figure 9. Vin = 12 V, 1.2 V≤ Vo < 2 V

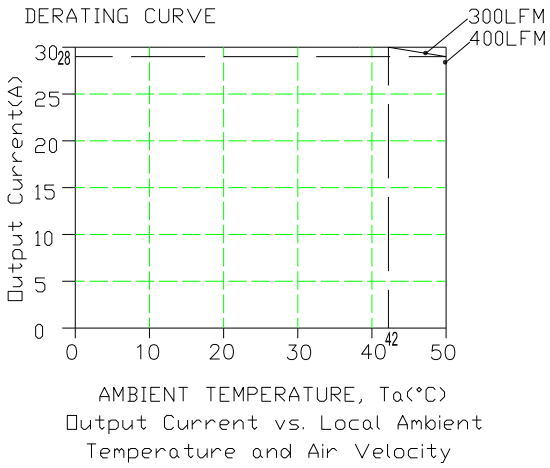

Figure 10. Vin = 12V, Vo = 2 V

10. RIPPLE AND NOISE WAVEFORM

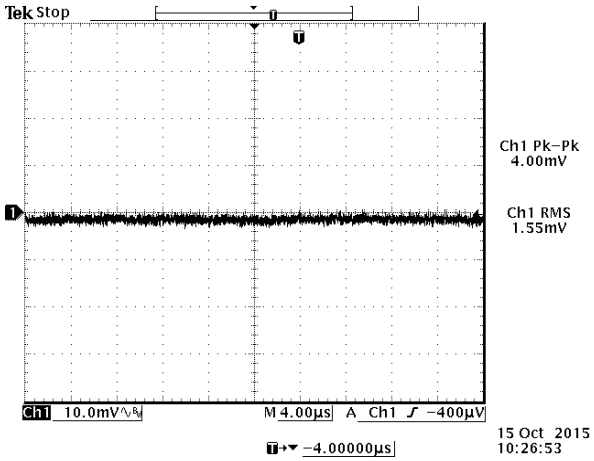

Figure 11. Ripple and noise at full load, 12 VDC input 0.6 VDC / 30 A output and Ta = 25℃

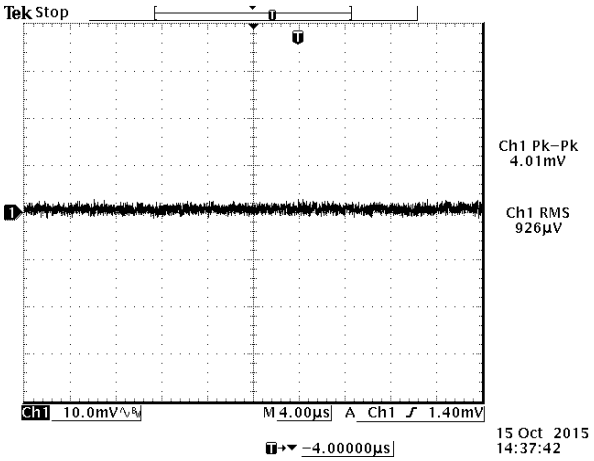

Figure 12. Ripple and noise at full load, 12 VDC input 0.9 VDC / 30 A output and Ta = 25℃

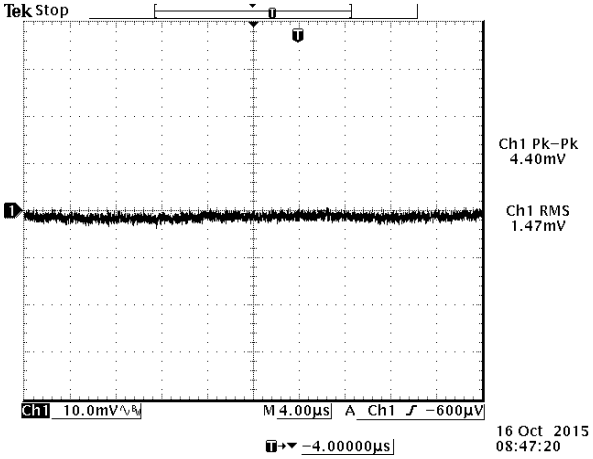

Figure 13. Ripple and noise at full load, 12 VDC input 2.0 VDC / 30 A output and Ta = 25℃

NOTE: Test condition of the output ripple and noise:
0-20 MHz BW, with a 10 µF+7*100 µF ceramic cap and 3*470 µF POSCAP ESR ≤ 12 m ohm at output.

11. TRANSIENT RESPONSE WAVEFORMS

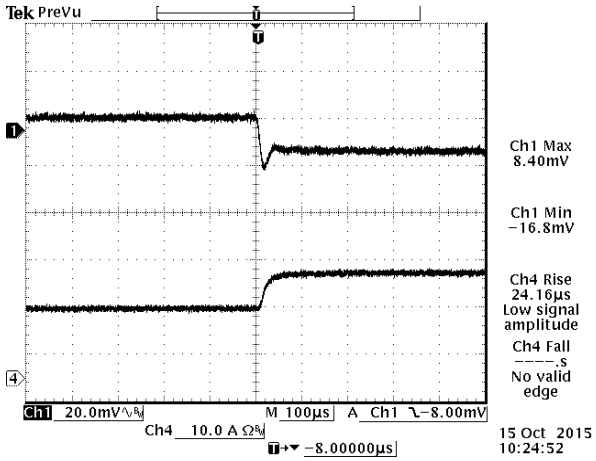

Figure 14. Vin = 50%-75% Load Transient at Vin = 12 VDC Vout = 0.6 VDC @ Ta = 25℃

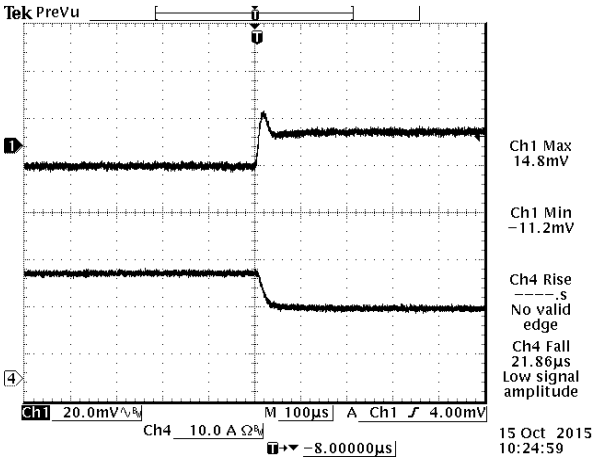

Figure 15. Vin = 75% - 50% Load Transient at Vin = 12 VDC Vout = 0.6 VDC @ Ta = 25℃

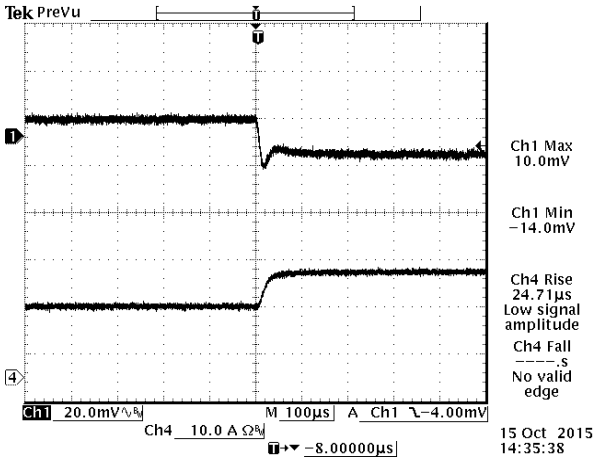

Figure 16. Vin = 50%-75% Load Transient at Vin = 12 VDC Vout = 0.9 VDC @ Ta = 25℃

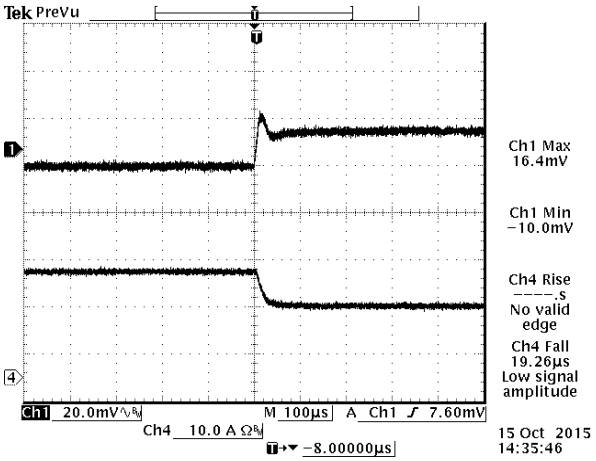

Figure 17. Vin = 75% - 50% Load Transient at Vin = 12 VDC Vout = 0.9 VDC @ Ta = 25℃

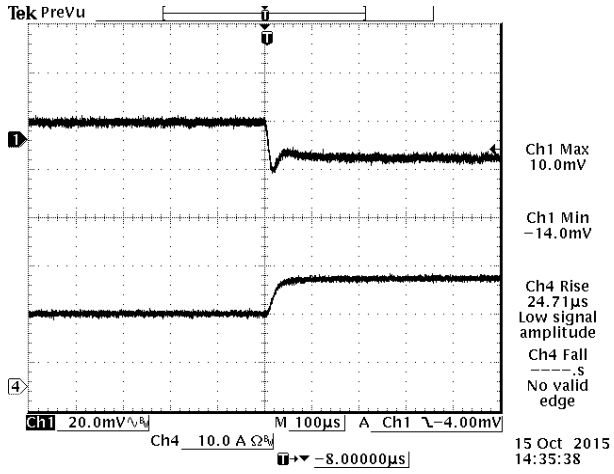

Figure 18. Vin = 50% - 75% Load Transient at Vin = 12 VDC Vout = 2.0 VDC @ Ta = 25℃

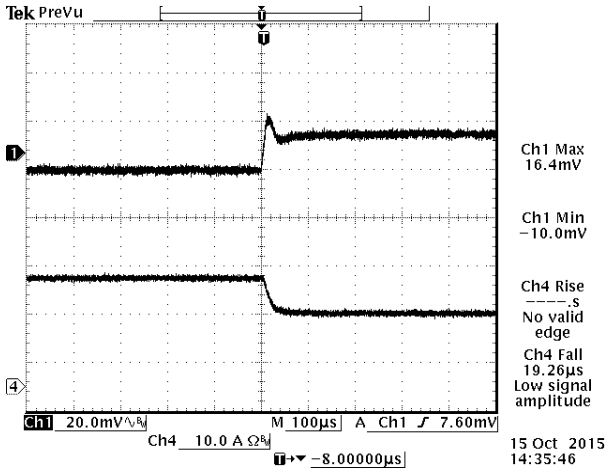

Figure 19. Vin = 75% - 50% Load Transient at Vin = 12 VDC Vout = 2.0 VDC @ Ta = 25℃

NOTE: Test condition of the Transient response:
di/dt = 2.5 A/µs, with a 10 µF+7*100 µF ceramic cap and 3*470 µF POSCAP ESR ≤ 12 m ohm at output.

12. INPUT UNDER-VOLTAGE LOCKOUT

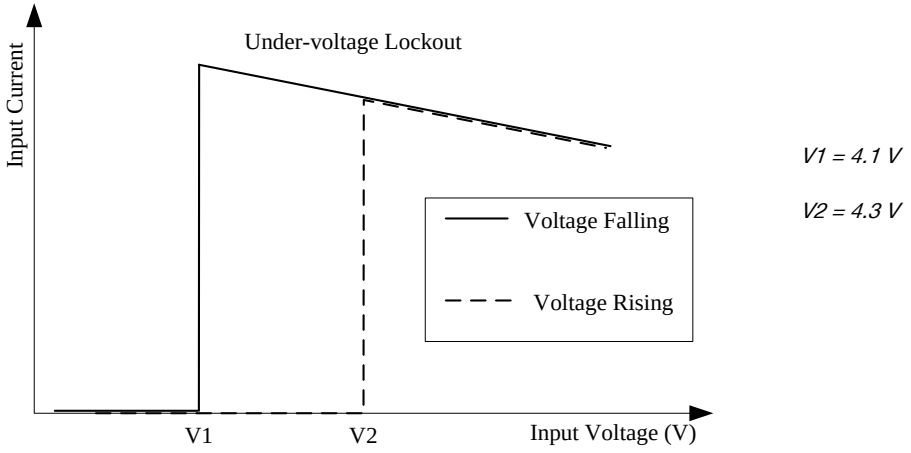

Figure 20. Input under-voltage lockout

13. STARTUP & SHUTDOWN

RISE TIME

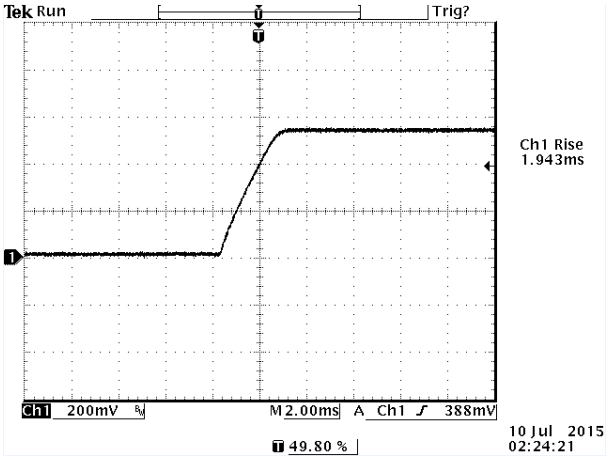

Figure 21. Rise time at full load, 12 VDC input
0.6 VDC / 30 A output and Ta = 25℃

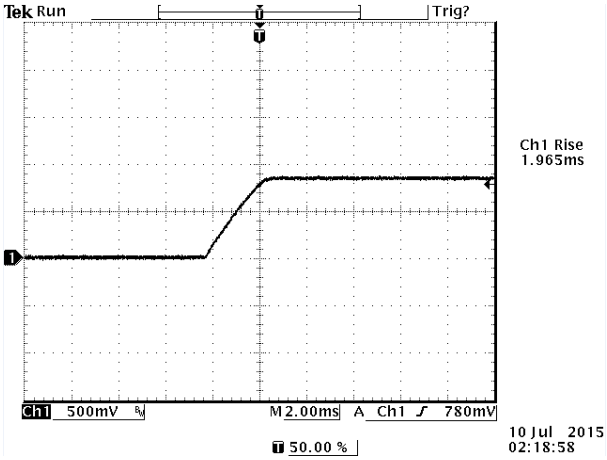

Figure 22. Rise time at full load, 12 VDC input
0.9 VDC / 30 A output and Ta = 25℃

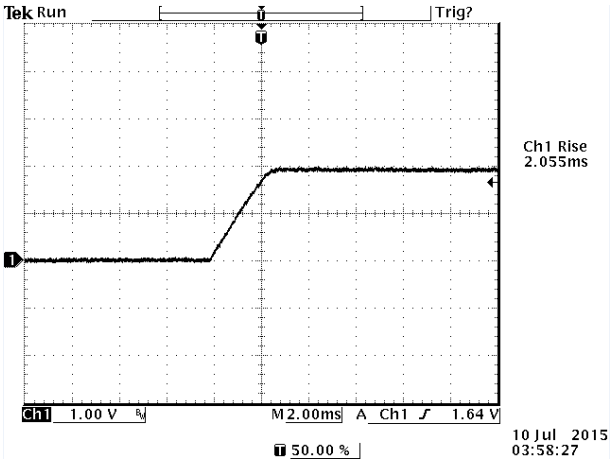

Figure 23. Rise time at full load, 12 VDC input
2.0 VDC / 30 A output and Ta = 25℃

NOTE: Test condition of the Rise time:
di/dt = 2.5 A/μs, with a 10 μF+7*100 μF ceramic cap and 3*470 μF POSCAP ESR ≤ 12 m ohm at output.

STARTUP TIME
Startup from remote on/off
Ch1: Vo
Ch3: remote on/off
Test Condition:
With a 10 µF+7*100 µF ceramic cap and 3*470 µF POSCAP ESR ≤ 12 m ohm at output.

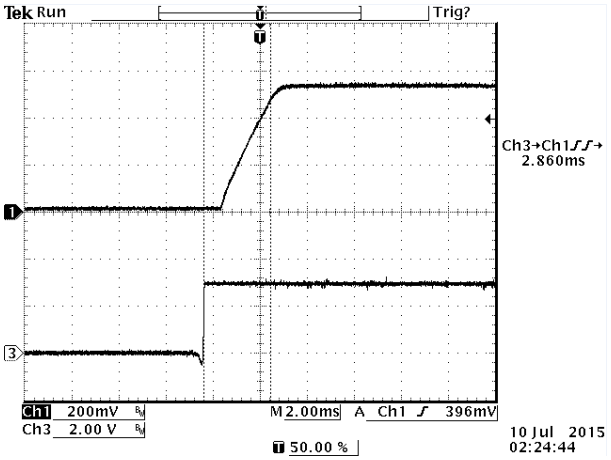

Figure 24. Startup time at full load, 12 VDC input
0.6 VDC / 30 A output and Ta = 25°C

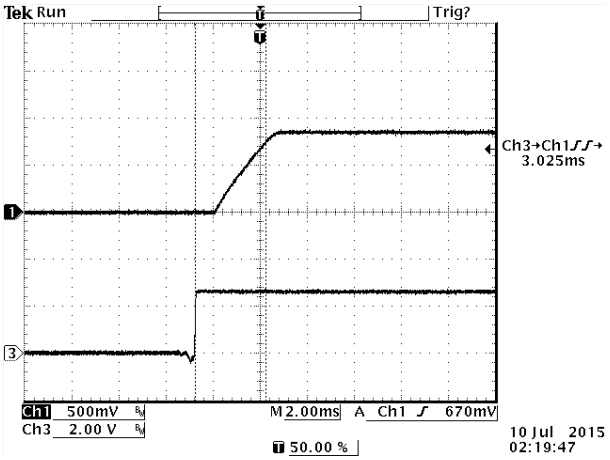

Figure 25. Startup time at full load, 12 VDC input
0.9 VDC / 30 A output and Ta = 25°C

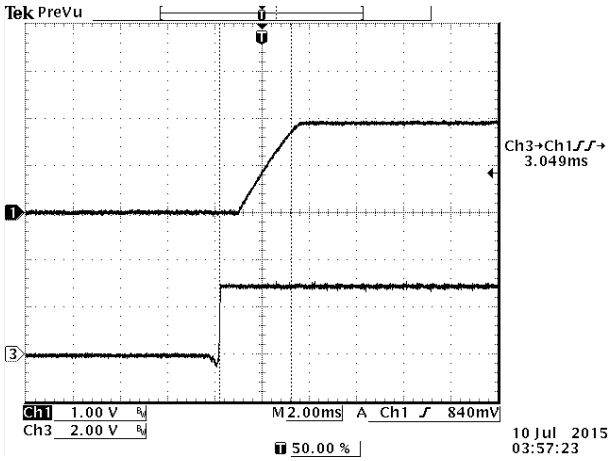

Figure 26. Startup time at full load, 12 VDC input
2.0 VDC / 30 A output and Ta = 25°C

14. TRIM

Output Voltage Set-Point Adjustment
Maximum trim up voltage is 2 V.
Minimum trim up voltage is 0.6 V.

Trim up circuit (using an external resistor)

Equations for calculating the trim resistor are shown below.
The Trim Up resistor should be connected between the Trim pin and the GND.
SRP1-30E1A0 Trim up Resistor Calculate Unit: kΩ
Vo is the desired output voltage.
Rtrimup is the required resistance between TRIM and GND.

$$Rtrimup = \frac{1.2}{Vo - 0.6}$$

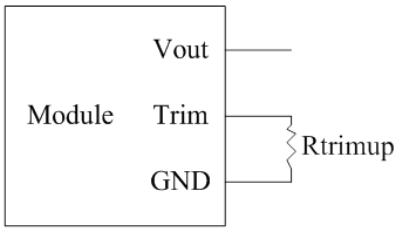

Figure 27. Trim up circuit (using an external resistor)

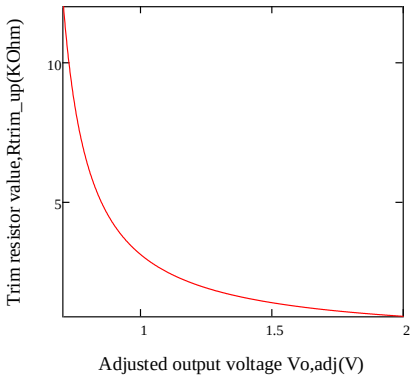

Figure 28. Trim up curve

Trim up circuit (using external PWM signal)

Equations for calculating the duty cycle are shown below.

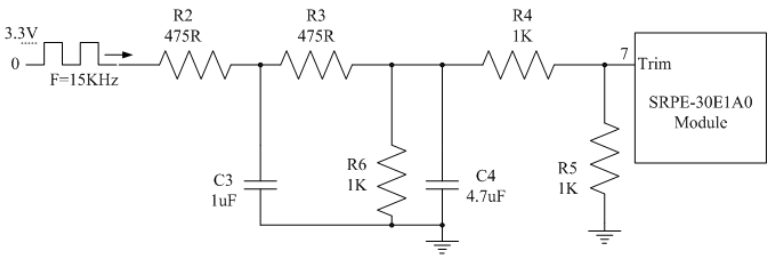

Figure 29. Trim up circuit (using external PWM signal)

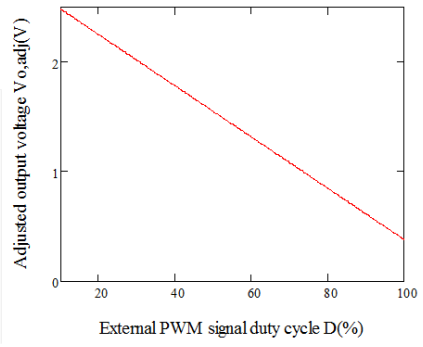

Figure 30. External PWM signal duty cycle

SRP1-30E1A0 Trim up duty cycle Calculate Unit: %

$$Vo(\mathrm{D}) = 2.72 - 0.0234D$$

Vo is the desired output voltage.
D is the external PWM signal duty cycle.

15. OVER CURRENT PROTECTION

To provide protection in a fault output overload condition, the module is equipped with internal current-limiting circuitry and can endure current limiting for a few milliseconds. If the overcurrent condition persists beyond a few milliseconds, the module will shut down into hiccup mode and restart once every 40 ms. The module operates normally when the output current goes into specified range. The typical average output current is 4 A during hiccup.

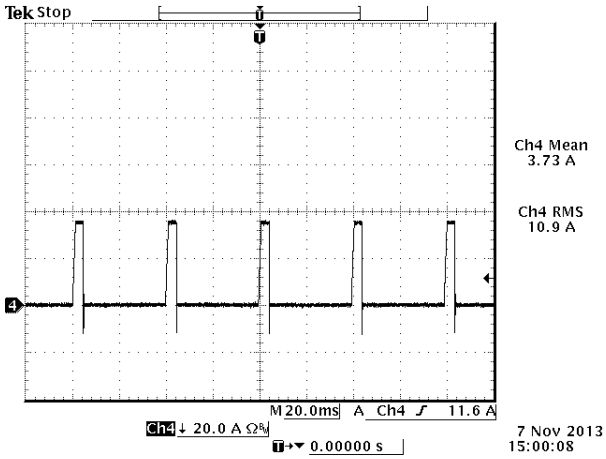

Figure 31. Output current @ SCP, Vin = 12 V Vout = 0.6 V, Ta = 25℃

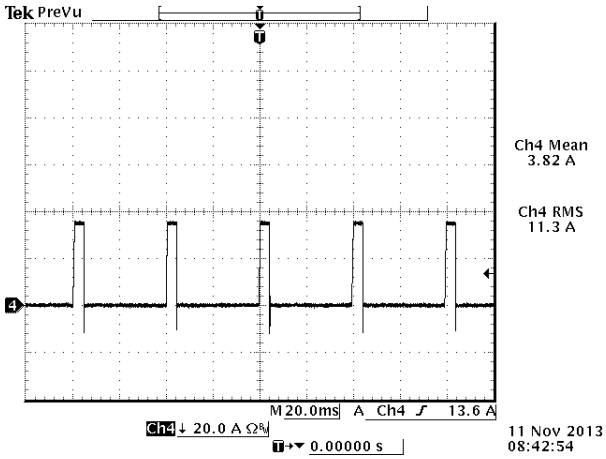

Figure 32. Output current @ SCP, Vin = 12 V Vout = 0.9 V, Ta = 25℃

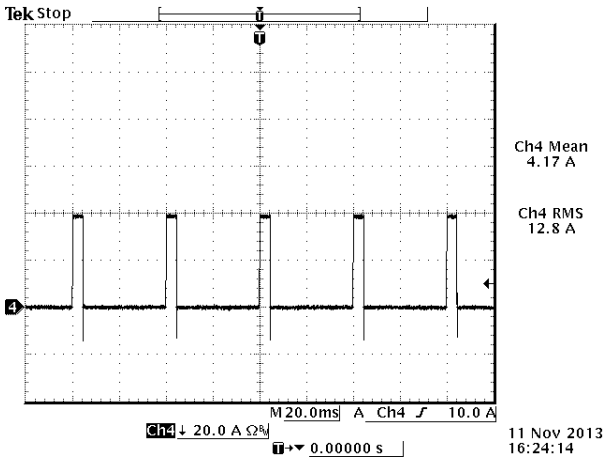

Figure 33. Output current @ SCP, Vin = 12 V Vout = 1.5 V, Ta = 25℃

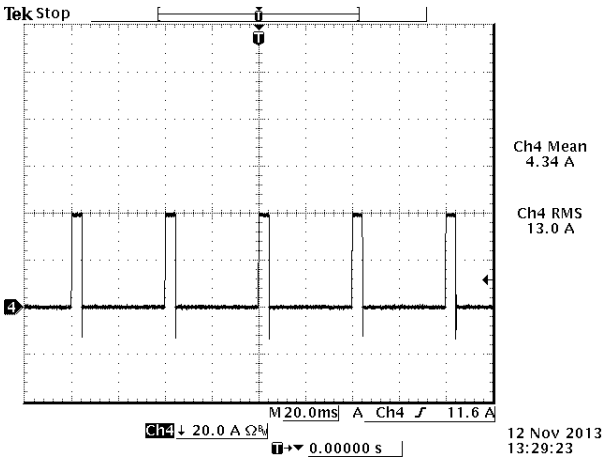

Figure 34. Output current @ SCP, Vin = 12 V Vout = 2.0 V, Ta = 25℃

NOTE: Test condition of the SCP:
With a 10 µF ceramic cap and a 470 µF POSCAP ESR ≤ 12mohm at output.

16. POWER GOOD

1. This module has a power good indicator output. Power good pin used positive logic and is open collector.

2. The maximum voltage pulled up externally on Power Good pin should not exceed 7V.

3. If the output voltage becomes within +10% and –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1ms internal delay.

4. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-μs) internal delay.

5. The pull up resistance must be larger than 10 kΩ.

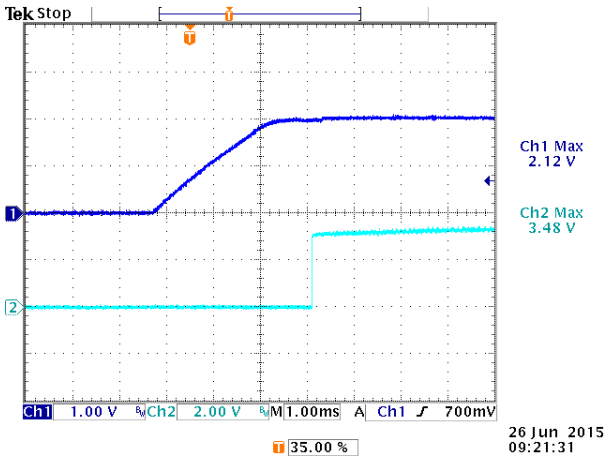

Figure 35. Typical Start-up using Remote on/off,
Vin = 12 V, Vo = 2 V, Io = 0 A
CH1: Vout; CH2: PG

17. SOLDERING INFORMATION

The SRPE-30E1A0 modules are designed to be compatible with reflow soldering process. The suggested Pb-free solder paste is Sn/Ag/Cu(SAC). The recommended reflow profile using Sn/Ag/Cu solder is shown in the following. Recommended reflow peak temperature is 245°C while the part can withstand peak temperature of 260°C maximum for 10 seconds. This profile should be used only as a guideline. Many other factors influence the success of SMT reflow soldering. Since your production environment may differ, please thoroughly review these guidelines with your process engineers.

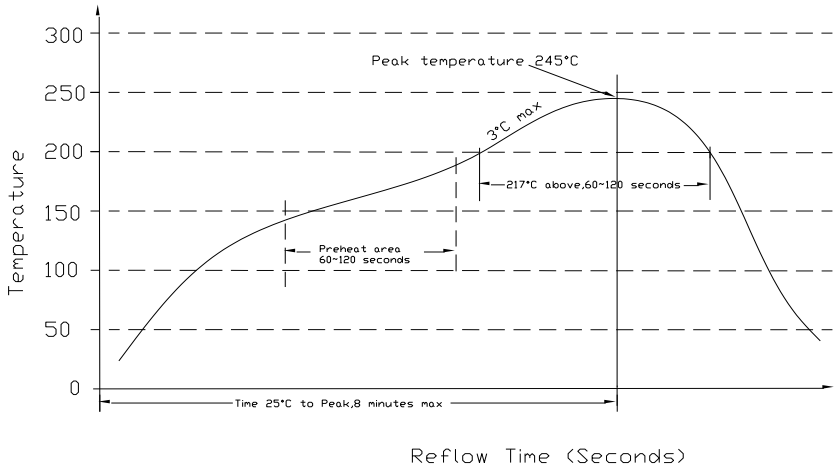

Figure 36. Soldering information

18. MSL RATING

The SRPE-30E1A0 modules have a MSL rating of 3.

19. STORAGE AND HANDLING

The SRPE-30E1A0 modules are designed to be compatible with J-STD-033 Rev: A (Handling, Packing, Shipping and Use of Moisture /Reflow Sensitive surface Mount devices). Moisture barrier bags (MBB) with desiccant are applied. The recommended storage environment and handling procedure is detailed in J-STD-033.

20. PRE-BAKING

This component has been designed, handled, and packaged ready for Pb-free reflow soldering. If the assembly shop follows J-STD-033 guidelines, no pre-bake of this component is required before being reflowed to a PCB. However, if the J-STD-033 guidelines are not followed by the assembler, Bel recommends that the modules should be pre-baked @ 120~125°C for a minimum of 4 hours (preferably 24 hours) before reflow soldering.

21. MECHANICAL OUTLINE

OUTLINE

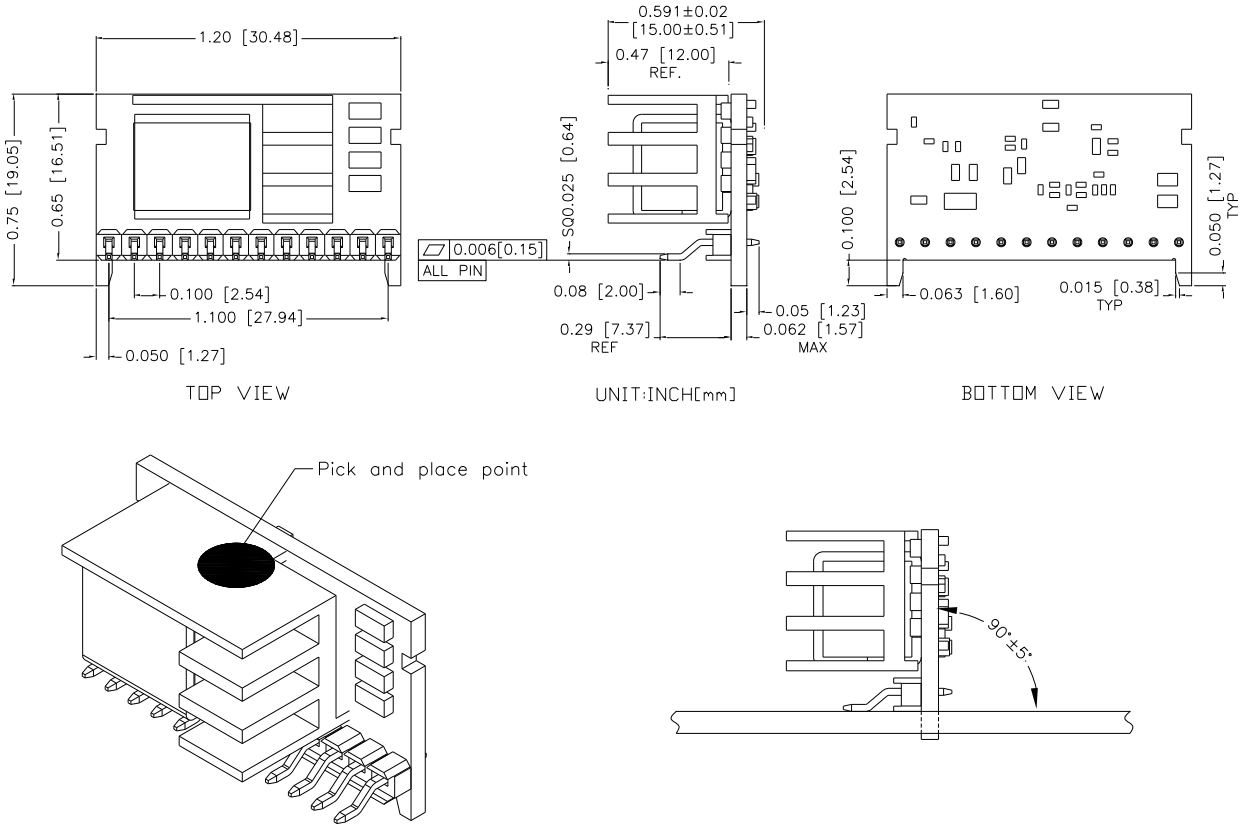

Figure 37. Outline

NOTE: 1) All Pins: Material - Copper Alloy;
Finish – 3 micro inches minimum Gold over 50 micro inches minimum Nickel plate
2) Un-dimensioned components are shown for visual reference only.
3) All dimensions in inch [mm]; Tolerances: x.xx +/-0.02 inch [0.51 mm]; x.xxx +/-0.010 inch [0.25 mm].

PIN DEFINITIONS

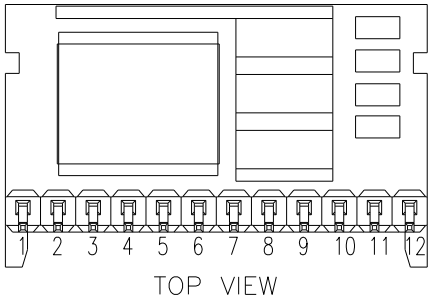

Figure 38. Pins

PIN	FUNCTION	PIN	FUNCTION
1	Vout	7	Trim
2	Vout	8	PGOOD
3	Vout	9	Vsense+
4	GND	10	Vsense-
5	GND	11	GND
6	Enable	12	Vin

RECOMMENDED PAD LAYOUT

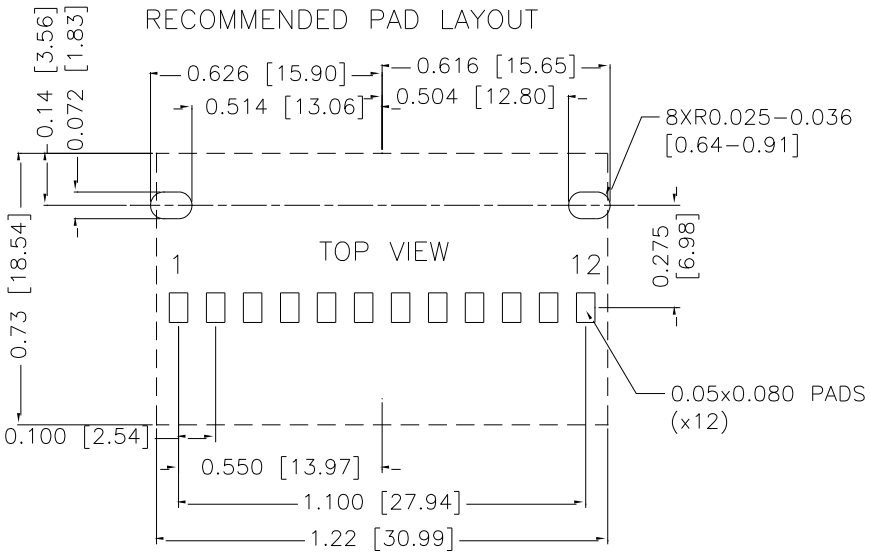

Figure 39. Recommended pad layout

22. REVISION HISTORY

DATE	REVISION	CHANGES DETAIL	APPROVAL
2013-08-19	PA	First release	J.Yan
2013-10-10	PB	Update mechanical drawing	J.Yan
2014-01-10	PC	Update input / output spec, efficiency and remote on/off.	J.Yan
2014-04-14	PD	Update Output Specs, General, Efficiency Data, NR, TR, Startup & Shutdown, OCP	J.Yan
2014-07-03	PE	Update part number explanation, RoHS compliance，Add MD Note.	J.Yan
2014-07-11	PF	Update Cover, MD	J.Yan
2014-07-29	G	Added assembly guide drawing	J.Yan
2014-12-18	H	Added trim resistor equation	J.Yan
2015-07-07	I	Input specs: 1. Change no load input current. 2.Change remoted off input current to 15mA. 3. Change input reflected ripple current (RMS) from 20mA to 30mA. 4. Update turn on voltage threshold: min value 3.8V, typical value 4.3V, max value 5V. 5. Update turn off voltage threshold: min value 3.8V, typical value 4.1V, max value 4.5V. Output specs: 1. Change output voltage set point max to 10%Vo. 2. Change the load/line regulation range as ±5%Vo. 3. Change output ripple and noise max value to 30mV. 4. Update transient response. General: 1. Update the efficiency. Including efficiency data and graphs. 2. Update the weight of module. Update the TD. Add the input noise. Add the PG signal section. Update mechanical drawing, change the thickness of module to 0.591 inch, change the thickness of heatsink to 0.47 inch.	J.Yan
2015-11-16	J	Output specs: Shrink the output voltage set point, line regulation, load regulation rang. Update the waveform of ripple and noise/transient response/Startup&Shutdown; add tilt dimension in mechanical drawing, update recommended pad layout.	J.Yan
2016-01-05	K	Output specs: Shrink the output voltage set point, line regulation, load regulation range.	J.Yan
2016-01-22	L	Update MTBF FIT	J.Yan
2016-02-02	M	Input specs: Update the turn on voltage information	J.Yan
2016-05-17	N	Input specs: Update the turn on voltage information	J.Yan
2021-06-30	AP	Add object ID. Add thermal test airflow direction.	XF.Jiang

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

bel POWER SOLUTIONS & PROTECTION
a bel group

Asia-Pacific +86 755 298 85888
Europe, Middle East +353 61 49 8941
North America +1 866 513 2839

