

HD74HC165

Parallel-load 8-bit Shift Register

REJ03D0581-0300

Rev.3.00

Jan 31, 2006

Description

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the Shift/Load input. Also included is a gated clock input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the Shift/Load input high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

Features

- High Speed Operation: t_{pd} (Clock to Q_H) = 21 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC165P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC165FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs					Internal outputs		Output
Shift/Load	Clock Inhibit	Clock	Serial	Parallel A H	Q_A	Q_B	Q_H
L	X	X	X	a h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L		H	X	H	Q_{An}	Q_{Gn}
H	L		L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Q_{A0} to Q_{H0} = Outputs remain unchanged.

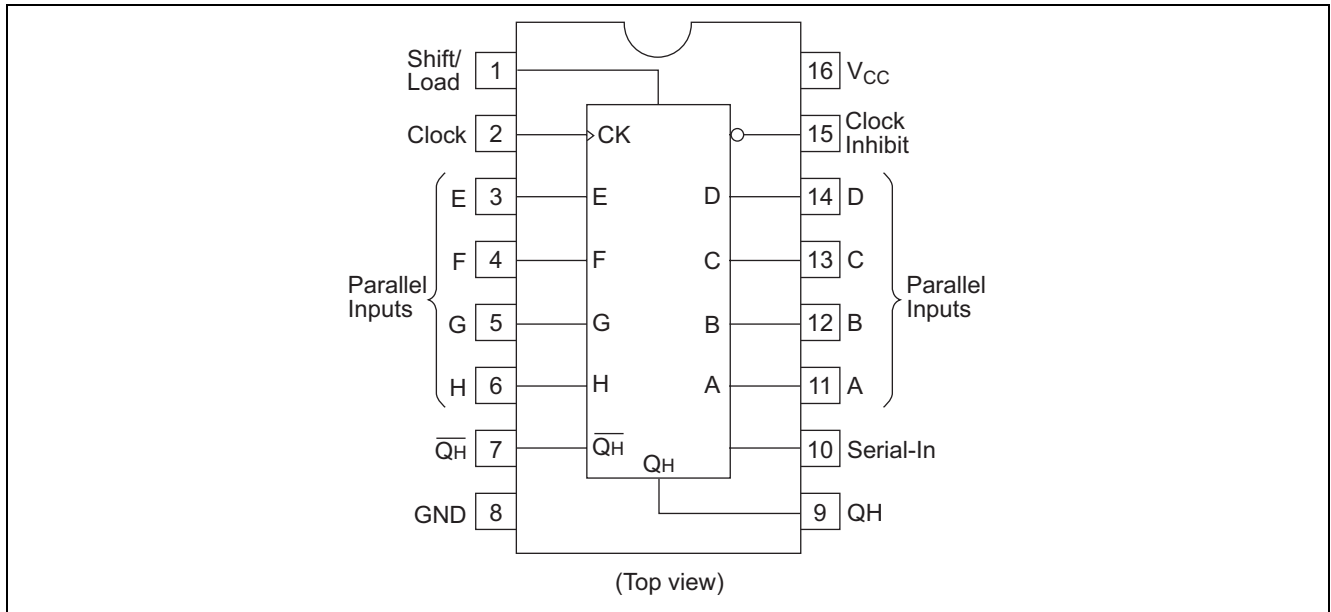
Q_{An} to Q_{Gn} = Data shifted from the previous stage on a positive edge at the clock input.

H : High level

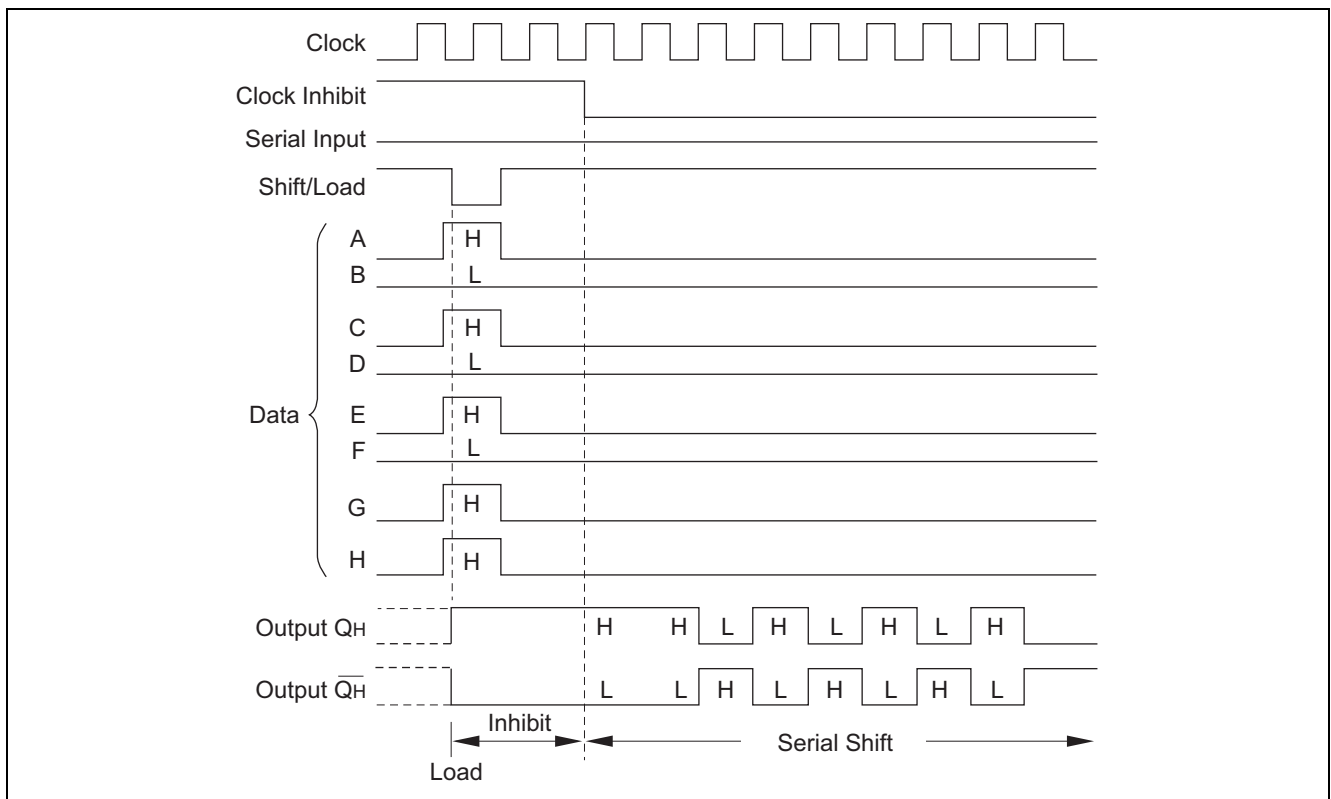
L : Low level

X : Irrelevant

Pin Arrangement



Timing Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{in}, V_{out}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0$ V
		0 to 500		$V_{CC} = 4.5$ V
		0 to 400		$V_{CC} = 6.0$ V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

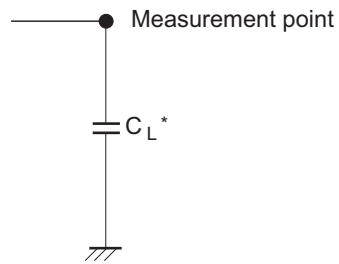
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20$ μA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			$I_{OH} = -4$ mA
		6.0	5.68	—	—	5.63	—			$I_{OH} = -5.2$ mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20$ μA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4$ mA
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2$ mA
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC}$ or GND, $I_{out} = 0$ μA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

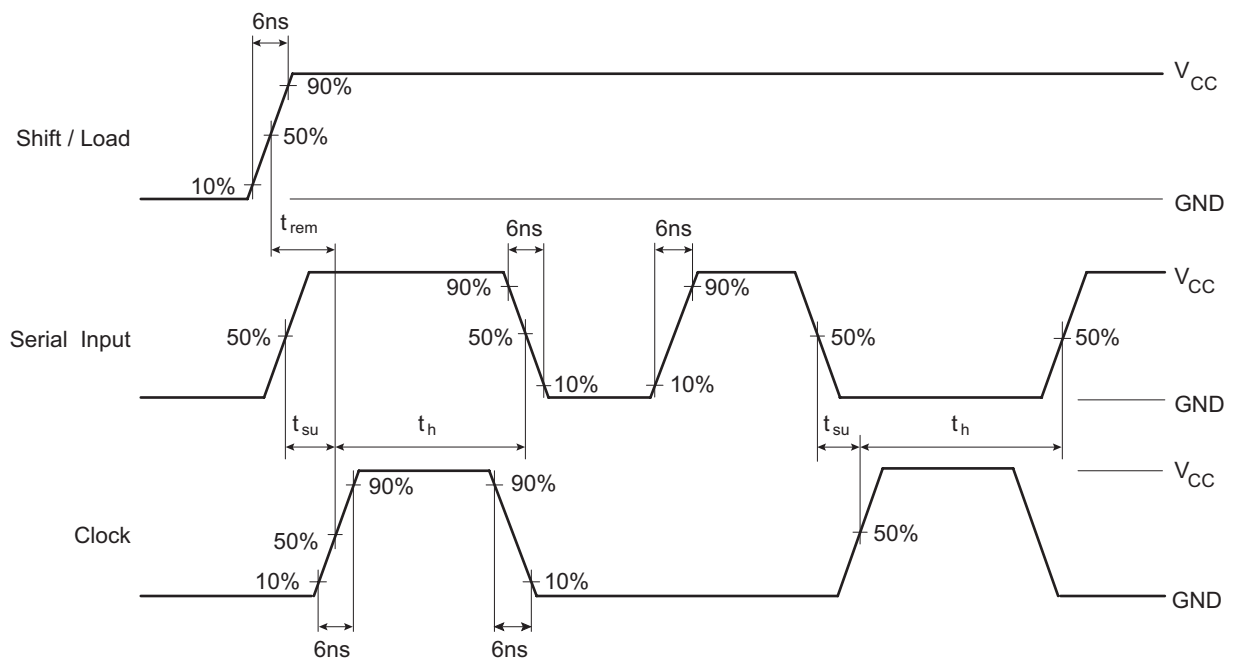
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t _{PLH} , t _{PHL}	2.0	—	—	150	—	190	ns	Clock to Q _H or $\overline{Q}_H$
		4.5	—	21	30	—	38		
		6.0	—	—	26	—	33		
		2.0	—	—	160	—	200	ns	Shift/Load to Q _H or $\overline{Q}_H$
		4.5	—	23	32	—	40		
		6.0	—	—	27	—	34		
		2.0	—	—	150	—	190	ns	H to Q _H or $\overline{Q}_H$
		4.5	—	21	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t _{su}	2.0	100	—	—	125	—	ns	Parallel data inputs to Shift/Load
		4.5	20	-3	—	25	—		
		6.0	17	—	—	21	—		
		2.0	100	—	—	125	—	ns	Serial input to Clock
		4.5	20	3	—	25	—		
		6.0	17	—	—	21	—		
		2.0	100	—	—	125	—	ns	Shift/load to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Removal time	t _{rem}	2.0	100	—	—	125	—	ns	Clock to Clock inhibit or Clock inhibit to Clock
		4.5	20	6	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t _h	2.0	5	—	—	5	—	ns	Shift/Load to parallel data input
		4.5	5	-3	—	5	—		
		6.0	5	—	—	5	—		
		2.0	5	—	—	5	—	ns	Clock to Serial input
		4.5	5	3	—	5	—		
		6.0	5	—	—	5	—		
		2.0	5	—	—	5	—	ns	Clock to Shift/Load
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t _w	2.0	80	—	—	100	—	ns	Clock, Shift/Load
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t _{TLH} , t _{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

Test Circuit

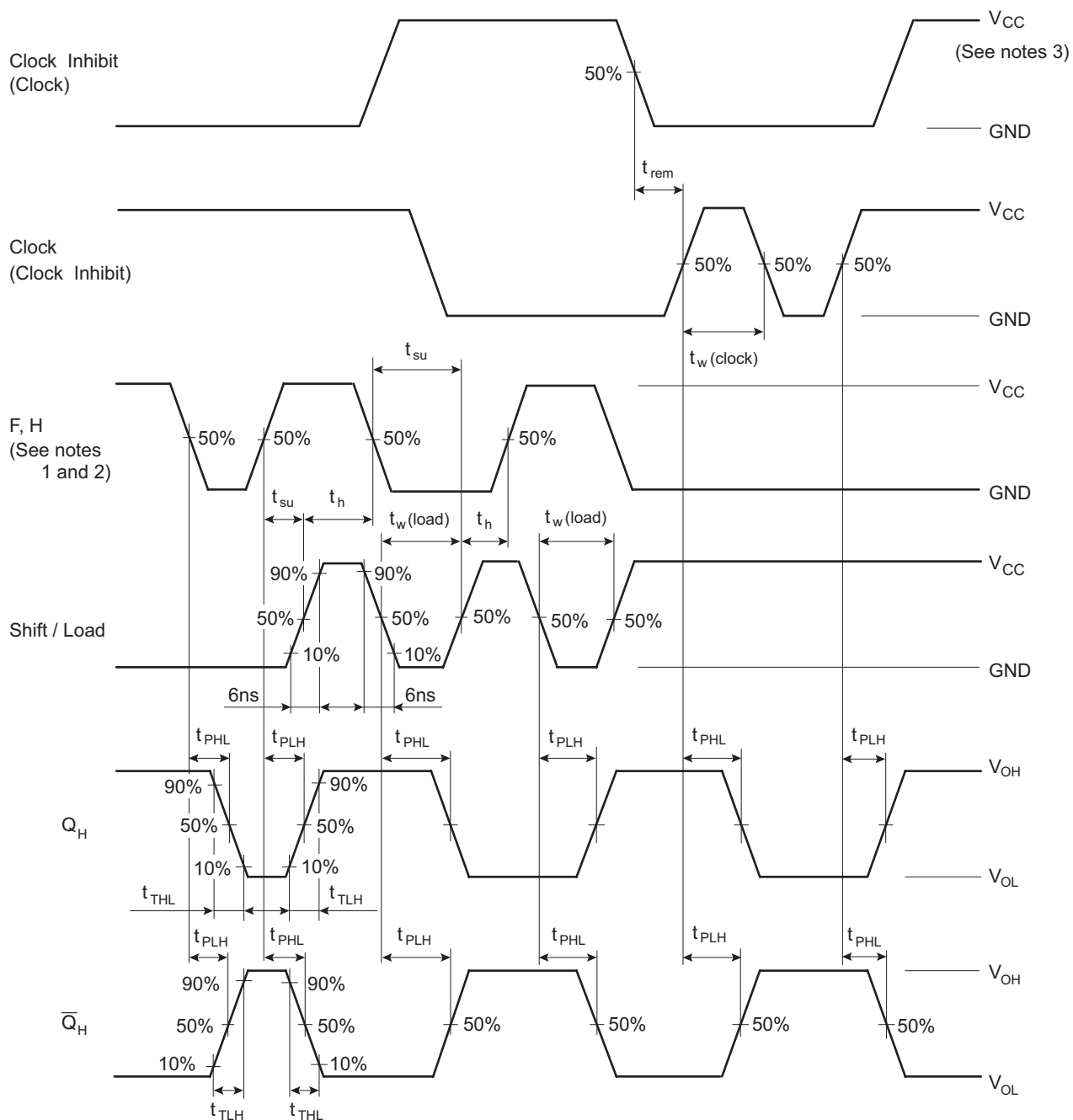


Note: C_L includes the probe and fix capacitance.

Waveforms

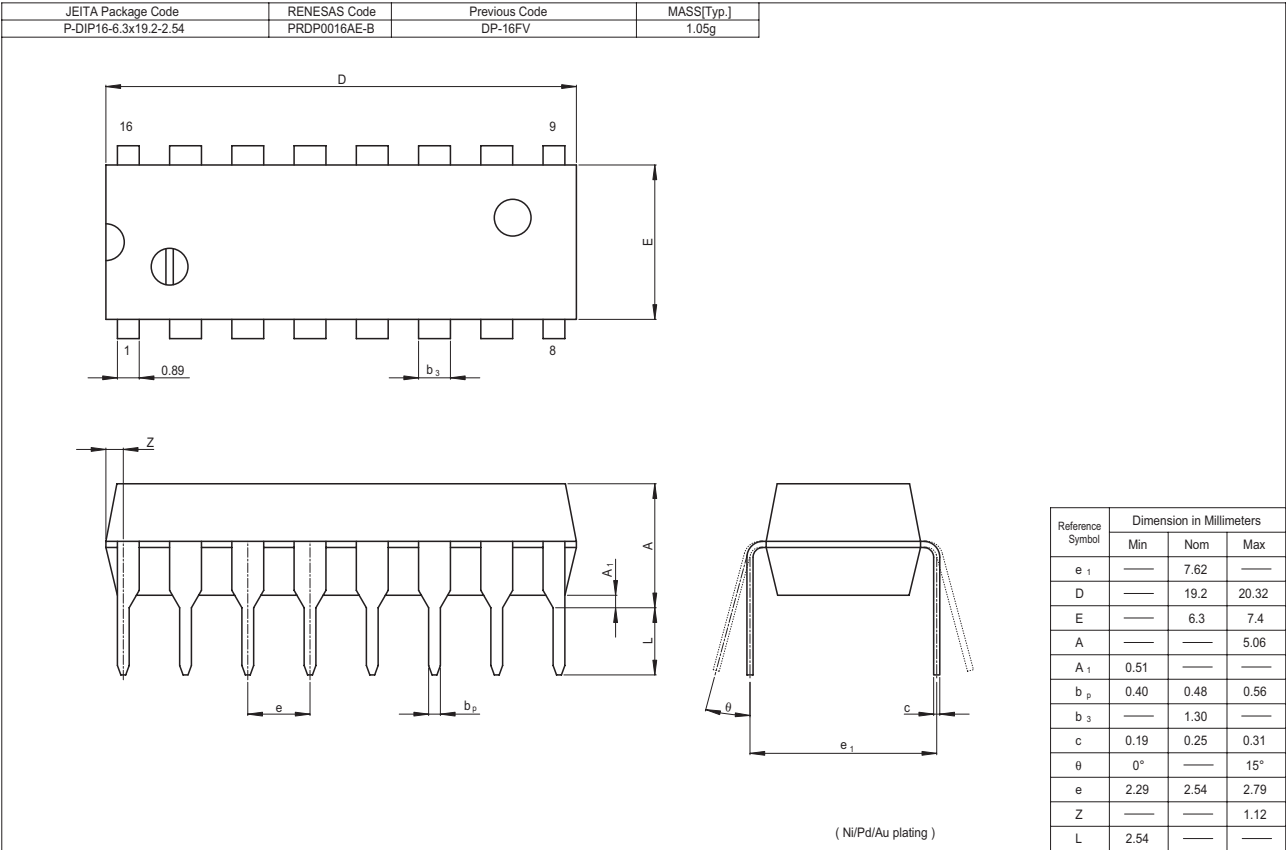
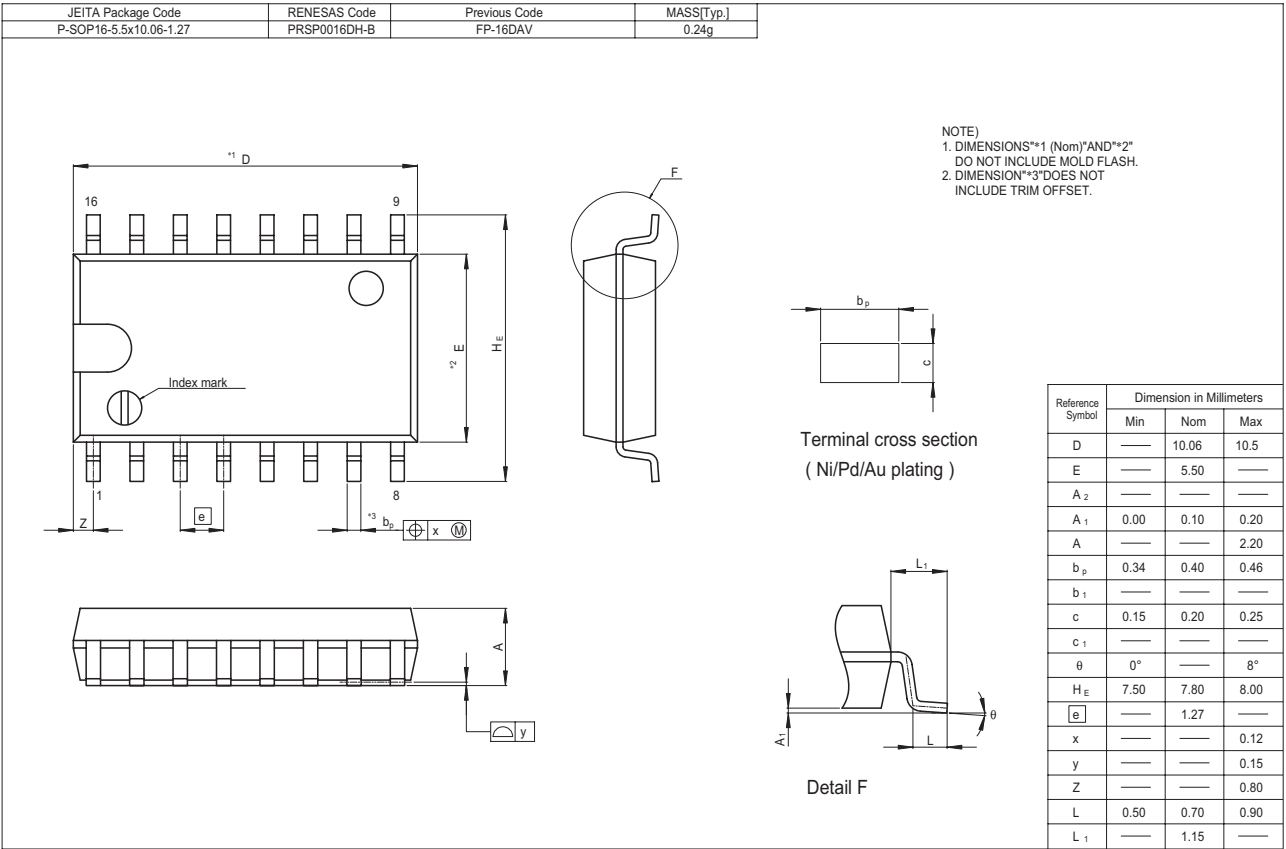


- Notes
1. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_n+7 .
 2. Input pulse : PRR $\leq$ 1MHz, duty cycle 50%



- Notes
1. The remaining six data inputs and the serial input are low.
 2. Prior to test, high-level data is loaded into H input.
 3. Disable while clock is high.
 4. Input pulse : PRR $\leq$ 1MHz, duty cycle 50%

Package Dimensions



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