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TAS5518C
8-Channel Digital Audio PWM Processor

Data Manual

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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1 Introduction

1.1 Features

- General Features
  - Automated Operation With an Easy-to-Use Control Interface
  - I^2C Serial-Control Slave Interface
  - Integrated AM Interference-Avoidance Circuitry
  - Single, 3.3-V Power Supply
  - 64-Pin TQFP Package
  - 5-V Tolerant Inputs
- Audio Input/Output
  - Automatic Master-Clock-Rate and Data-Sample-Rate Detection
  - Eight Serial Audio Input Channels
  - Eight PWM Audio Output Channels Configurable as Six Channels With Stereo Lineout or Eight Channels
  - Line Output Is a PWM Output to Drive an External Differential-Input Operational Amplifier
  - Headphone PWM Output to Drive an External Differential Amplifier Like the TPA112
  - PWM Outputs Support Single-Ended and Bridge-Tied Loads
  - 32-, 38-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz Sampling Rates
  - Data Formats: 16-, 20-, or 24-Bit Left-Justified, I^2S, or Right-Justified Input Data
  - 64-f_S Bit-Clock Rate
  - 128-, 192-, 256-, 384-, 512-, and 768-f_S Master Clock Rates (Up to a Maximum of 50 MHz)
- Audio Processing
  - 48-Bit Processing Architecture With 76 Bits of Precision for Most Audio-Processing Features
  - Volume Control Range 36 dB to –127 dB
    - Master Volume Control Range of 18 dB to –100 dB
    - Eight Individual Channel Volume Control Ranges of 18 dB to –127 dB
  - Programmable Soft Volume and Mute Update Rates
  - Four Bass and Treble Tone Controls With ±18-dB Range, Selectable Corner Frequencies, and Second-Order Slopes
    - L, R, and C
    - LS, RS
    - LR, RR
    - Sub
  - Configurable Loudness Compensation
  - Two Dynamic Range Compressors With Two Thresholds, Two Offsets, and Three Slopes
  - Seven Biquads Per Channel
  - Full 8×8 Input Crossbar Mixer. Each Signal-Processing Channel Input Can Be Any Ratio of the Eight Input Channels.
  - 8×2 Output Mixer, Channels 1–6. Each Output Is a Mix of Any Two Signal-Processed Channels. It Is Recommended to Use the Pass-Through output Mixer Configuration.
  - 8×3 Output Mixer, Channels 7 and 8. Each Output Is a Mix of Any Three Signal-Processed Channels. It Is Recommended to Use the Pass-Through Output Mixer Configuration.
  - Three Coefficient Sets Stored on the Device Can Be Selected Manually or Automatically (Based on Specific Data Rates).
  - DC Blocking Filters
  - Able to Support a Variety of Bass Management Algorithms
- PWM Processing
  - 32-Bit Processing PWM Architecture With 40 Bits of Precision
  - 8× Oversampling With Fifth-Order Noise Shaping at 32 kHz–48 kHz, 4× Oversampling at 88.2 kHz and 96 kHz, and 2× Oversampling at 176.4 kHz and 192 kHz
  - >110-dB Dynamic Range
  - THD+N < 0.1%
  - 20-Hz–20-kHz, Flat Noise Floor for 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz Data Rates
  - Digital De-Emphasis for 32-, 44.1-, and 48-kHz Data Rates
  - Flexible Automute Logic With Programmable Threshold and Duration for Noise-Free Operation
  - Intelligent AM Interference-Avoidance System Provides Clear AM Reception
  - Power-Supply Volume Control (PSVC)

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Support for Enhanced Dynamic Range in High-Performance Applications

- **Adjustable Modulation Limit**

1.2 Overview

The TAS5518C is an 8-channel digital pulse-width modulator (PWM) that provides both advanced performance and a high level of system integration. The TAS5518C is designed to interface seamlessly with most audio digital signal processors. The TAS5518C automatically adjusts control configurations in response to clock and data rate changes and idle conditions. This enables the TAS5518C to provide an easy-to-use control interface with relaxed timing requirements.

The TAS5518C can drive eight channels of H-bridge power stages. Texas Instruments power stage parts TAS5111, TAS5112, or TAS5182 with FETs are designed to work seamlessly with the TAS5518C. The TAS5518C supports either the single-ended or bridge-tied-load configuration. The TAS5518C also provides a high-performance, differential output to drive an external, differential-input, analog headphone amplifier (such as the TPA112).

The TAS5518C uses AD modulation operating at a 384-kHz switching rate for 48-, 96-, and 192-kHz data. The 8× oversampling combined with the fifth-order noise shaper provides a broad, flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

The TAS5518C is a clocked slave-only device. The TAS5518C receives MCLK, SCLK, and LRCLK from other system components. The TAS5518C accepts master clock rates of 128, 192, 256, 384, 512, and 768 f_S. The TAS5518C accepts a 64-f_S bit clock.

The TAS5518C allows for extending the dynamic range by providing a power-supply, volume-control (PSVC) output signal.

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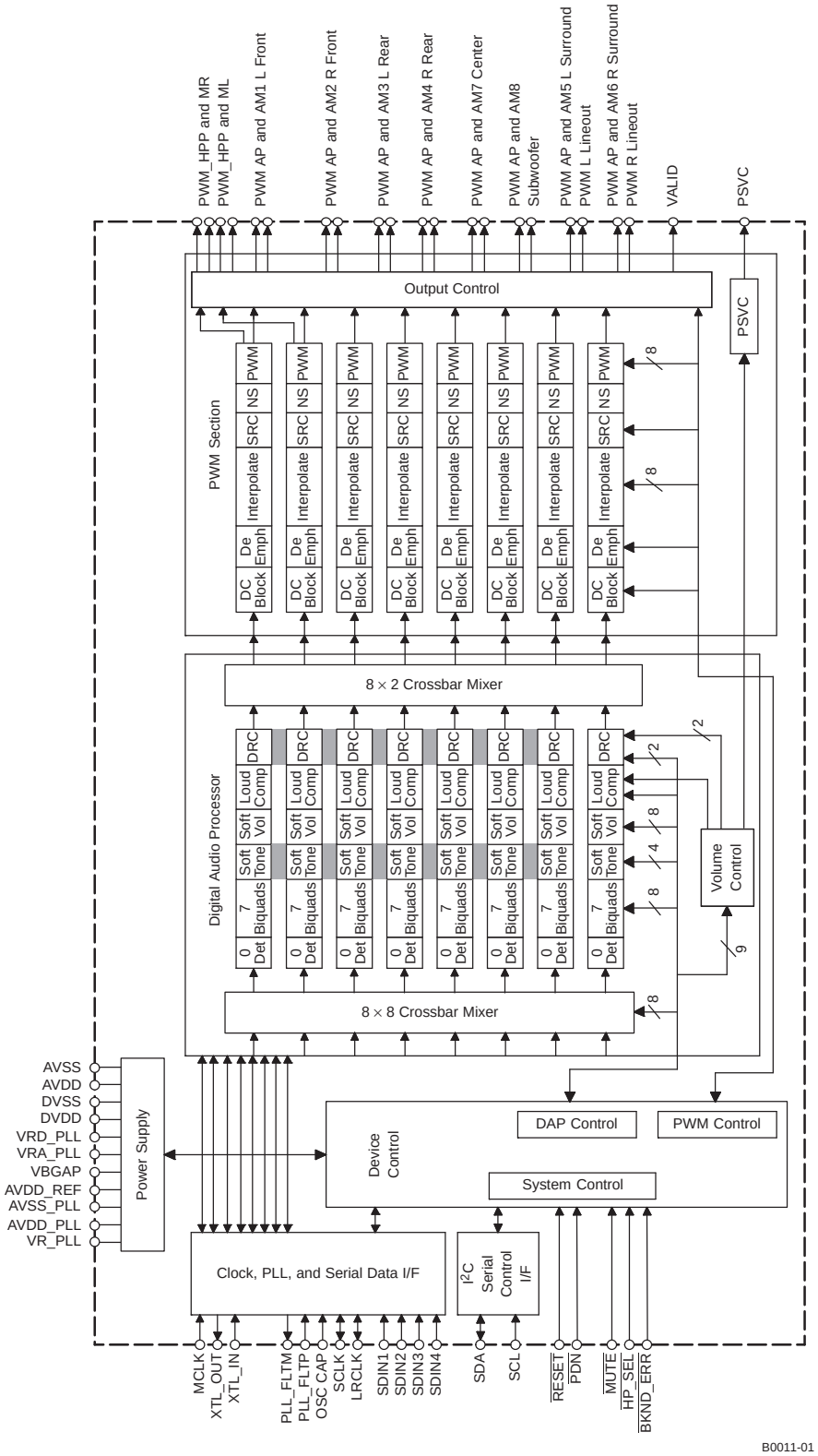

Figure 1-1. TAS5518C Functional Structure

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1.3 Changes From the TAS5518 to the TAS5518C

- High-pass filter is enabled by default (0x03 bit 7)

1.4 TAS5518C System Diagrams

Typical applications for the TAS5518C are 6- to 8-channel audio systems such as DVD or AV receivers. Figure 1-2 shows the basic system diagram of the DVD receiver.

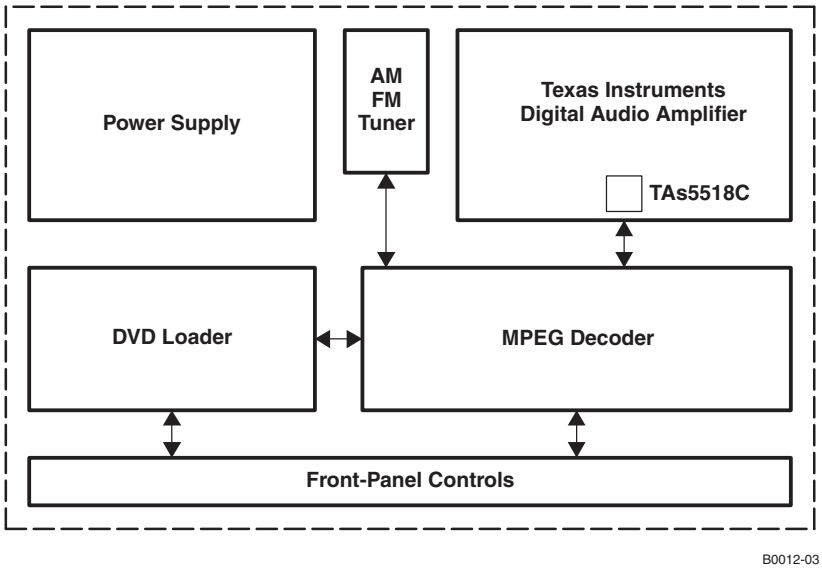

Figure 1-2. Typical TAS5518C Application (DVD Receiver)

Figure 1-3 shows the pass-through output mixer channel configuration when using the TAS5518C.

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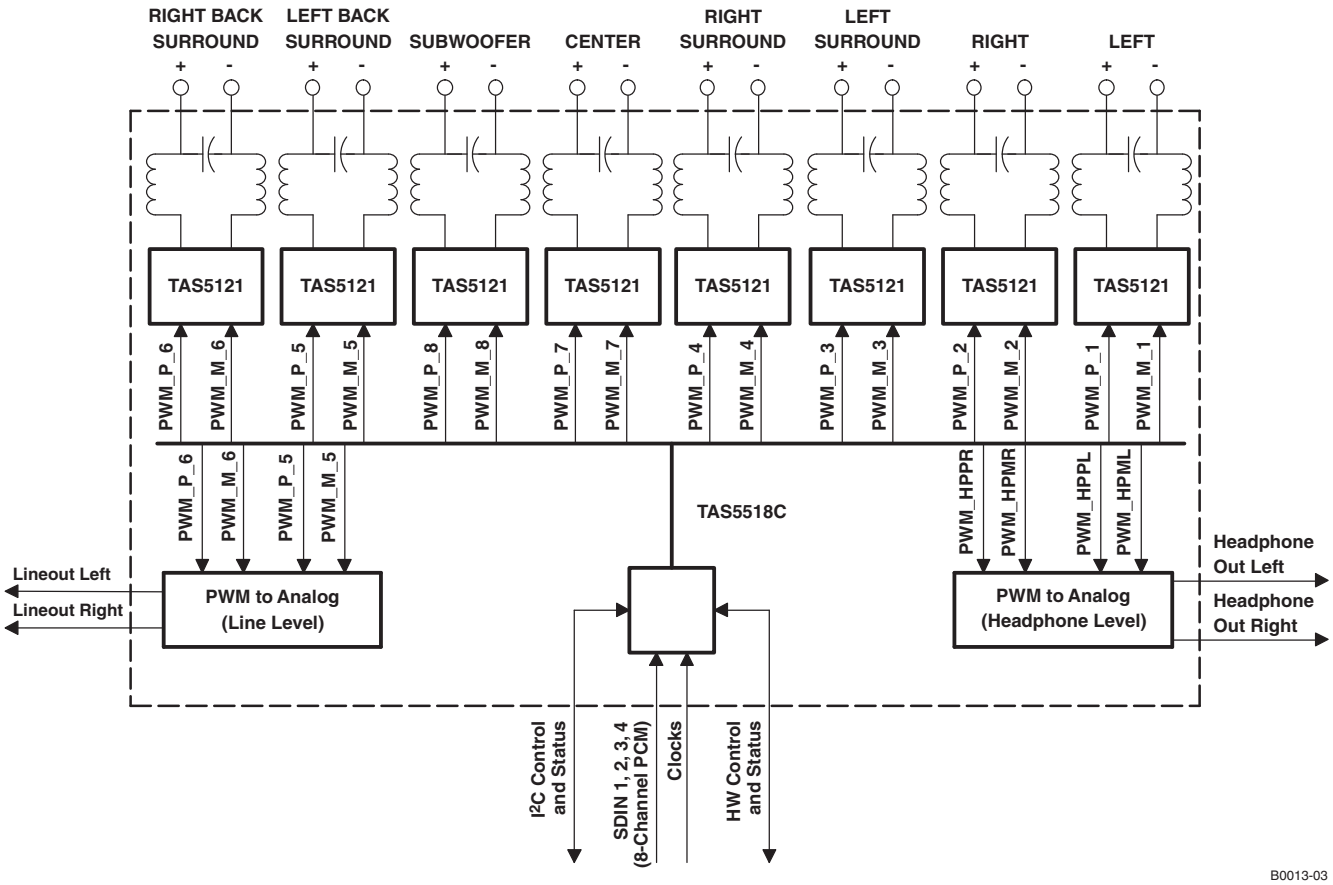

Figure 1-3. Pass-Through Output Mixer TAS5518C Channel Configuration

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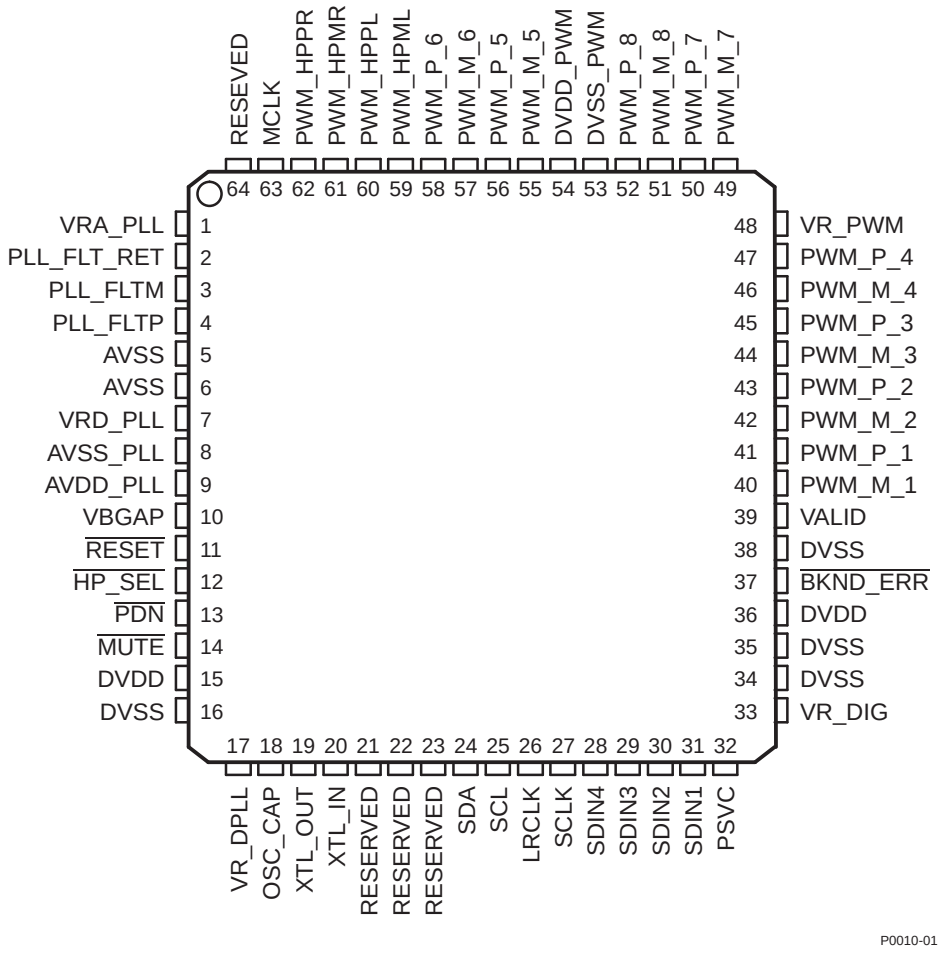
2 Description

2.1 Physical Characteristics

2.1.1 Terminal Assignments

PAG PACKAGE
(TOP VIEW)



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2.1.2 Ordering Information

T_A	PLASTIC 64-PIN PQFP (P/N)
0°C to 70°C	TAS5518CPAG

2.1.3 Terminal Descriptions

TERMINAL		TYPE(1)	5-V TOLERANT	TERMINATION(2)	DESCRIPTION
NAME	NO.				
AVDD_PLL	9	P			3.3-V analog power supply for PLL. This terminal can be connected to the same power source used to drive power terminal DVDD; but to achieve low PLL jitter, this terminal should be bypassed to AVSS_PLL with a 0.1-μF low-ESR capacitor.
AVSS	5, 6	P			Analog ground
AVSS_PLL	8	P			Analog ground for PLL. This terminal should reference the same ground as terminal DVSS; but to achieve low PLL jitter, ground noise at this terminal must be minimized. The availability of the AVSS terminal allows a designer to use optimizing techniques such as star ground connections, separate ground planes, or other quiet ground-distribution techniques to achieve a quiet ground reference at this terminal.
$\overline{\text{BKND_ERR}}$	37	DI		Pullup	Active-low. A back-end error sequence is generated by applying logic low to this terminal. The $\overline{\text{BKND_ERR}}$ results in no change to any system parameters, with all H-bridge drive signals going to a hard-mute state (M-state).
DVDD	15, 36	P			3.3-V digital power supply. It is recommended that decoupling capacitors of 0.1 μF and 10 μF be mounted close to this pin (see application schematics).
DVDD_PWM	54	P			3.3-V digital power supply for PWM
DVSS	16, 34, 35, 38	P			Digital ground
DVSS_PWM	53	P			Digital ground for PWM
$\overline{\text{HP_SEL}}$	12	DI	5 V	Pullup	Headphone in/out selector. When a logic low is applied, the headphone is selected (speakers are off). When a logic high is applied, speakers are selected (headphone is off).
LRCLK	26	DI	5 V		Serial-audio data left/right clock (sampling-rate clock)
MCLK	63	DI	5 V	Pulldown	MCLK is a 3.3-V master clock input. The input frequency of this clock can range from 4 MHz to 50 MHz.
$\overline{\text{MUTE}}$	14	DI	5 V	Pullup	Soft mute of outputs, active-low (muted signal = a logic low, normal operation = a logic high). The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.
OSC_CAP	18	AO			Oscillator capacitor
$\overline{\text{PDN}}$	13	DI	5 V	Pullup	Power down, active-low. $\overline{\text{PDN}}$ powers down all logic and stops all clocks whenever a logic low is applied. The internal parameters are preserved through a power-down cycle, as long as $\overline{\text{RESET}}$ is not active. The duration for system recovery from power down is 100 ms.
PLL_FLT_RET	2	AO			PLL external filter return
PLL_FLTM	3	AO			PLL negative input. Connected to PLL_FLT_RET via an RC network
PLL_FLTP	4	AI			PLL positive input. Connected to PLL_FLT_RET via an RC network
PSVC	32	O			Power-supply volume control PWM output
PWM_HPML	59	DO			PWM left-channel headphone (differential –)
PWM_HPMR	61	DO			PWM right-channel headphone (differential –)
PWM_HPPL	60	DO			PWM left-channel headphone (differential +)
PWM_HPPR	62	DO			PWM right-channel headphone (differential +)
PWM_M_1	40	DO			PWM 1 output (differential –)
PWM_M_2	42	DO			PWM 2 output (differential –)
PWM_M_3	44	DO			PWM 3 output (differential –)
PWM_M_4	46	DO			PWM 4 output (differential –)
PWM_M_5	55	DO			PWM 5 output (lineout L) (differential –)
PWM_M_6	57	DO			PWM 6 output (lineout R) (differential –)
PWM_M_7	49	DO			PWM 7 output (differential –)
PWM_M_8	51	DO			PWM 8 output (differential –)
PWM_P_1	41	DO			PWM 1 output (differential +)
PWM_P_2	43	DO			PWM 2 output (differential +)
PWM_P_3	45	DO			PWM 3 output (differential +)

(1) Type: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output

(2) All pullups are 20-μA weak pullups and all pulldowns are 20-μA weak pulldowns. The pullups and pulldowns are included to ensure proper input logic levels if the terminals are left unconnected (pullups → logic-1 input; pulldowns → logic-0 input). Devices that drive inputs with pullups must be able to sink 20 μA while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 20 μA while maintaining a logic-1 drive level.

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TERMINAL		TYPE(1)	5-V TOLERANT	TERMINATION(2)	DESCRIPTION
NAME	NO.				
PWM_P_4	47	DO			PWM 4 output (differential +)
PWM_P_5	56	DO			PWM 5 output (lineout L) (differential +)
PWM_P_6	58	DO			PWM 6 output (lineout R) (differential +)
PWM_P_7	50	DO			PWM 7 output (differential +)
PWM_P_8	52	DO			PWM 8 output (differential +)
RESERVED	21, 22, 23, 64				Connect to digital ground
$\overline{\text{RESET}}$	11	DI	5 V	Pullup	System reset input, active-low. A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the TAS5518C to its default conditions, sets the valid output low, and places the PWM in the hard-mute state (M-state). Master volume is immediately set to full attenuation. On the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4- to 5-ms device initialization and sets the volume at mute.
SCL	25	DI	5 V		I^2C serial-control clock input/output
SCLK	27	DI	5 V		Serial-audio data clock (shift clock) input
SDA	24	DIO	5 V		I^2C serial-control data-interface input/output
SDIN1	31	DI	5 V	Pulldown	Serial-audio data input 1 is one of the serial-data input ports. SDIN1 supports four discrete (stereo) data formats and is capable of inputting data at 64 f_S.
SDIN2	30	DI	5 V	Pulldown	Serial-audio data input 2 is one of the serial-data input ports. SDIN2 supports four discrete (stereo) data formats and is capable of inputting data at 64 f_S.
SDIN3	29	DI	5 V	Pulldown	Serial-audio data input 3 is one of the serial-data input ports. SDIN3 supports four discrete (stereo) data formats and is capable of inputting data at 64 f_S.
SDIN4	28	DI	5 V	Pulldown	Serial-audio data input 4 is one of the serial-data input ports. SDIN4 supports four discrete (stereo) data formats and is capable of inputting data at 64 f_S.
VALID	39	DO			Output indicating validity of PWM outputs, active-high
VBGAP	10	P			Band-gap voltage reference. A pinout of the internally regulated 1.2-V reference. Typically has a 1-nF low-ESR capacitor between VBGAP and AVSS_PLL. This terminal must not be used to power external devices.
VR_DIG	33	P			Voltage reference for 1.8-V digital core supply. A pinout of the internally regulated 1.8-V power used by digital core logic. A 4.7-µF low-ESR capacitor(3) should be connected between this terminal and DVSS. This terminal must not be used to power external devices.
VR_DPLL	17	P			Voltage reference for 1.8-V digital PLL supply. A pinout of the internally regulated 1.8-V power used by digital PLL logic. A 0.1-µF low-ESR capacitor(3) should be connected between this terminal and DVSS_CORE. This terminal must not be used to power external devices.
VR_PWM	48	P			Voltage reference for 1.8-V digital PWM core supply. A pinout of the internally regulated 1.8-V power used by digital PWM core logic. A 0.1-µF low-ESR capacitor(3) should be connected between this terminal and DVSS_PWM. This terminal must not be used to power external devices.
VRA_PLL	1	P			Voltage reference for 1.8-V PLL analog supply. A pinout of the internally regulated 1.8-V power used by PLL logic. A 0.1-µF low-ESR capacitor(3) should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.
VRD_PLL	7	P			Voltage reference for 1.8-V PLL digital supply. A pinout of the internally regulated 1.8-V power used by PLL logic. A 0.1-µF low-ESR capacitor(3) should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.
XTL_IN	20	AI			XTL_OUT and XTL_IN are the only LVCMOS terminals on the device. They provide a reference clock for the TAS5518C via use of an external fundamental-mode crystal. XTL_IN is the 1.8-V input port for the oscillator circuit. A 13.5-MHz crystal (HCM49) is recommended.
XTL_OUT	19	AO			XTL_OUT and XTL_IN are the only LVCMOS terminals on the device. They provide a reference clock for the TAS5518C via use of an external fundamental-mode crystal. XTL_OUT is the 1.8-V output drive to the crystal. A 13.5-MHz crystal (HCM49) is recommended.

(3) If desired, low-ESR capacitance values can be implemented by paralleling two or more ceramic capacitors of equal value. Paralleling capacitors of equal value provides an extended high-frequency supply decoupling. This approach avoids the potential of producing parallel resonance circuits that have been observed when paralleling capacitors of different values.

Not Recommended For New Designs

2.2 TAS5518C Functional Description

Figure 1-1 shows the TAS5518C functional structure. The following sections describe the TAS5518C functional blocks:

- Power supply
- Clock, PLL, and serial data interface
- I^2C serial-control interface
- Device control
- Digital audio processor (DAP)

2.2.1 Power Supply

The power-supply section contains supply regulators that provide analog and digital regulated power for various sections of the TAS5518C. The analog supply supports the analog PLL, whereas digital supplies support the digital PLL, the digital audio processor (DAP), the pulse-width modulator (PWM), and the output control.

2.2.2 Clock, PLL, and Serial Data Interface

The TAS5518C is a clocked slave-only device that requires the use of an external 13.5-MHz crystal. It accepts MCLK, SCLK, and LRCLK as inputs only.

The TAS5518C uses the external crystal to provide a time base for:

- Continuous data and clock error detection and management
- Automatic data-rate detection and configuration
- Automatic MCLK-rate detection and configuration (automatic bank switching)
- Supporting I^2C operation/communication while MCLK is absent

  The TAS5518C automatically handles clock errors, data-rate changes, and master-clock frequency changes without requiring intervention from an external system controller. This feature significantly reduces system complexity and design.

2.2.2.1 Serial Audio Interface

The TAS5518C operates as a slave-only/receive-only serial data interface in all modes. The TAS5518C has four PCM serial data interfaces to permit eight channels of digital data to be received through the SDIN1, SDIN2, SDIN3, and SDIN4 inputs. The serial audio data is in MSB-first, 2s-complement format.

The serial data input interface of the TAS5518C can be configured in right-justified, I^2S, or left-justified modes. The serial data interface format is specified using the I^2C data-interface control register. The supported formats and word lengths are shown in Table 2-1.

Not Recommended For New Designs

Table 2-1. Serial Data Formats

RECEIVE SERIAL DATA FORMAT	WORD LENGTH
Right-justified	16
Right-justified	20
Right-justified	24
I^2S	16
I^2S	20
I^2S	24
Left-justified	16
Left-justified	20
Left-justified	24

Serial data is input on SDIN1, SDIN2, SDIN3, and SDIN4. The TAS5518C accepts 16-, 20-, or 24-bit serial data at 32, 38, 44.1, 48, 88.2, 96, 176.4, or 192 kHz in left-justified, I^2S, or right-justified format. Data is input using a 64-f_S SCLK clock and an MCLK rate of 128, 192, 256, 384, 512, or 768 f_S, up to a maximum of 50 MHz. The clock speed and serial data format are I^2C configurable.

2.2.3 *I ^{2}C Serial-Control Interface*

The TAS5518C has an I^2C serial-control slave interface (write address = 0x36 and read address = 0x37) to receive commands from a system controller. The serial-control interface supports both normal-speed (100-kHz) and high-speed (400-kHz) operations without wait states. Because the TAS5518C has a crystal time base, this interface operates even when MCLK is absent.

The serial control interface supports both single-byte and multiple-byte read/write operations for status registers and the general control registers associated with the PWM. However, for the DAP data-processing registers, the serial control interface also supports multiple-byte (4-byte) write operations.

The I^2C supports a special mode which permits I^2C write operations to be broken up into multiple data-write operations that are multiples of 4 data bytes. These are 6-byte, 10-byte, 14-byte, 18-byte, etc., write operations that are composed of a device address, read/write bit, subaddress, and any multiple of 4 bytes of data. This permits the system to incrementally write large register values without blocking other I^2C transactions. In order to use this feature, the first block of data is written to the target I^2C address, and each subsequent block of data is written to a special append register (0xFE) until all the data is written and a stop bit is sent. An incremental read operation is not supported.

2.2.4 *Device Control*

The TAS5518C control section provides the control and sequencing for the TAS5518C. The device control provides both high- and low-level control for the serial control interface, clock and serial data interfaces, digital audio processor, and pulse-width modulator sections.

2.2.5 *Digital Audio Processor (DAP)*

The DAP arithmetic unit is used to implement all audio-processing functions: soft volume, loudness compensation, bass and treble processing, dynamic range control, channel filtering, and input and output mixing. Figure 2-1 shows the TAS5518C DAP architecture.

The DAP accepts 24-bit data from the serial data interface and outputs 32-bit data to the PWM section. The DAP supports two configurations, one for 32-kHz to 96-kHz data and one for 176.4-kHz to 192-kHz data.

2.2.5.1 TAS5518C Audio-Processing Configurations

The 32-kHz to 96-kHz configuration supports eight channels of data processing that can be configured either as eight channels, or as six channels with two channels for separate stereo line outputs.

The 176.4-kHz to 192-kHz configuration supports three channels of signal processing with five channels passed through (or derived from the three processed channels).

To support efficiently the processing requirements of both multichannel 32-kHz to 96-kHz data and the 2-channel 176.4-kHz and 192-kHz data, the TAS5518C has separate audio-processing features for 32-kHz to 96-kHz data rates and for 176.4 kHz and 192 kHz. See Table 2-2 for a summary of TAS5518C processing feature sets.

2.2.5.2 TAS5518C Audio Signal-Processing Functions

The DAP provides 10 primary signal-processing functions:

- The data-processing input has a full 8×8 input crossbar mixer. This enables each input to be any mix of the eight input channels.
- Two I^2C programmable threshold detectors in each channel support automute.
- Seven biquads per channel
- Four soft bass and treble tone controls with ±18-dB range, programmable corner frequencies, and second-order slopes. In 8-channel mode, bass and treble controls are normally configured as follows:
  - Bass and treble 1: Channel 1 (left), channel 2 (right), and channel 7 (center)
  - Bass and treble 2: Channel 3 (left surround) and channel 4 (right surround)
  - Bass and treble 3: Channel 5 (left back surround) and channel 6 (right back surround)
  - Bass and treble 4: Channel 8 (subwoofer)
- Individual channel and master volume controls. Each control provides an adjustment range of 18 dB to –109 dB plus mute. This permits a total volume device control range of 36 dB to –109 dB plus mute. The master volume control can be configured to control six or eight channels. The DAP soft volume and mute update interval is I^2C programmable. The update is performed at a fixed rate regardless of the sample rate.
- Programmable loudness compensation that is controlled via the combination of the master and individual volume settings.
- Two dual-threshold, dual-rate, dynamic range compressors (DRCs). The volume gain values provided are used as input parameters using the maximum RMS (master volume × individual channel volume).
- 8×2 output mixer (channels 1–6). Each output is a mix of any two signal-processed channels. It is recommended to use the pass-through output mixer configuration.
- 8×3 output mixer (channels 7 and 8). Each output is a mix of any three signal-processed channels. It is recommended to use the pass-through output mixer configuration.
- The DAP maintains three sets of coefficient banks that are used to maintain separate sets of sample-rate-dependent parameters for the biquad, tone controls, loudness, and DRC in RAM. These can be set to be automatically selected for one or more data sample rates or can be manually selected under I^2C program control. This feature enables coefficients for different sample rates to be stored in the TAS5518C and then selected when needed.

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Table 2-2. TAS5518C Audio-Processing Feature Sets

FEATURE	32 kHz–96 kHz 8-CHANNEL FEATURE SET	32 kHz–96 kHz 6 + 2 LINEOUT FEATURE SET	176.4- and 192-kHz FEATURE SET
Signal-processing channels	8	6 + 2	3
Pass-through channels	N/A		5
Master volume	1 for 8 channels	1 for 6 channels	1 for 8 channels
Individual channel volume controls	8		8
Bass and treble tone controls	Four bass and treble tone controls with ±18-dB range, programmable corner frequencies, and second-order slopes L, R, and C (Ch1, 2, and 7) LS, RS (Ch3 and 4) LBS, RBS (Ch5 and 6) Sub (Ch8)	Four bass and treble tone controls with ±18-dB range, programmable corner frequencies, and second-order slopes L, R, and C (Ch1, 2, and 7) LS, RS (Ch3 and 4) Sub (Ch8) Line L and R (Ch5 and 6)	Two bass and treble tone controls with ±18-dB range, programmable corner frequencies, and second-order slopes L and R (Ch1 and 2) Sub (Ch8)
Biquads	56		21
Dynamic range compressors	DRC1 for seven satellites and DRC2 for sub	DRC1 for five satellites and DRC2 for sub (Ch5 and 6 uncompressed)	DRC1 for two satellites and DRC2 for sub
Input/output mapping/ mixing	Each of the eight signal-processing channel inputs can be any mix of the eight input channels. Each of the eight outputs can be any mix of any two processed channels.		Each of the three signal-processing channels or the five pass-though channel inputs can be any mix of the eight input channels. Each of the eight outputs can be any mix of any of the three processed channels or five bypass channels.
DC-blocking filters (implemented in PWM section)	Eight channels		
Digital de-emphasis (implemented in PWM section)	Eight channels for 32 kHz, 44.1 kHz, and 48 kHz	Six channels for 32 kHz, 44.1 kHz, and 48 kHz	N/A
Loudness	Eight channels	Six channels	Three channels
Number of coefficient sets stored	Three additional coefficient sets can be stored in memory.		

2.3 TAS5518C DAP Architecture

2.3.1 TAS5518C DAP Architecture Diagrams

Figure 2-1 shows the TAS5518C DAP architecture for $f_S \leq 96$ kHz. Note the TAS5518C bass management architecture shown in channels 1, 2, 7, and 8. Note that the I^2C registers are shown to help the designer configure the TAS5518C.

Figure 2-2 shows the TAS5518C architecture for $f_S = 176.4$ kHz or $f_S = 192$ kHz. Note that only channels 1, 2, and 8 contain all the features. Channels 3–7 are pass-through except for volume controls.

Figure 2-3 shows TAS5518C detailed channel processing. The output mixer is 8×2 for channels 1–6 and 8×3 for channels 7 and 8.

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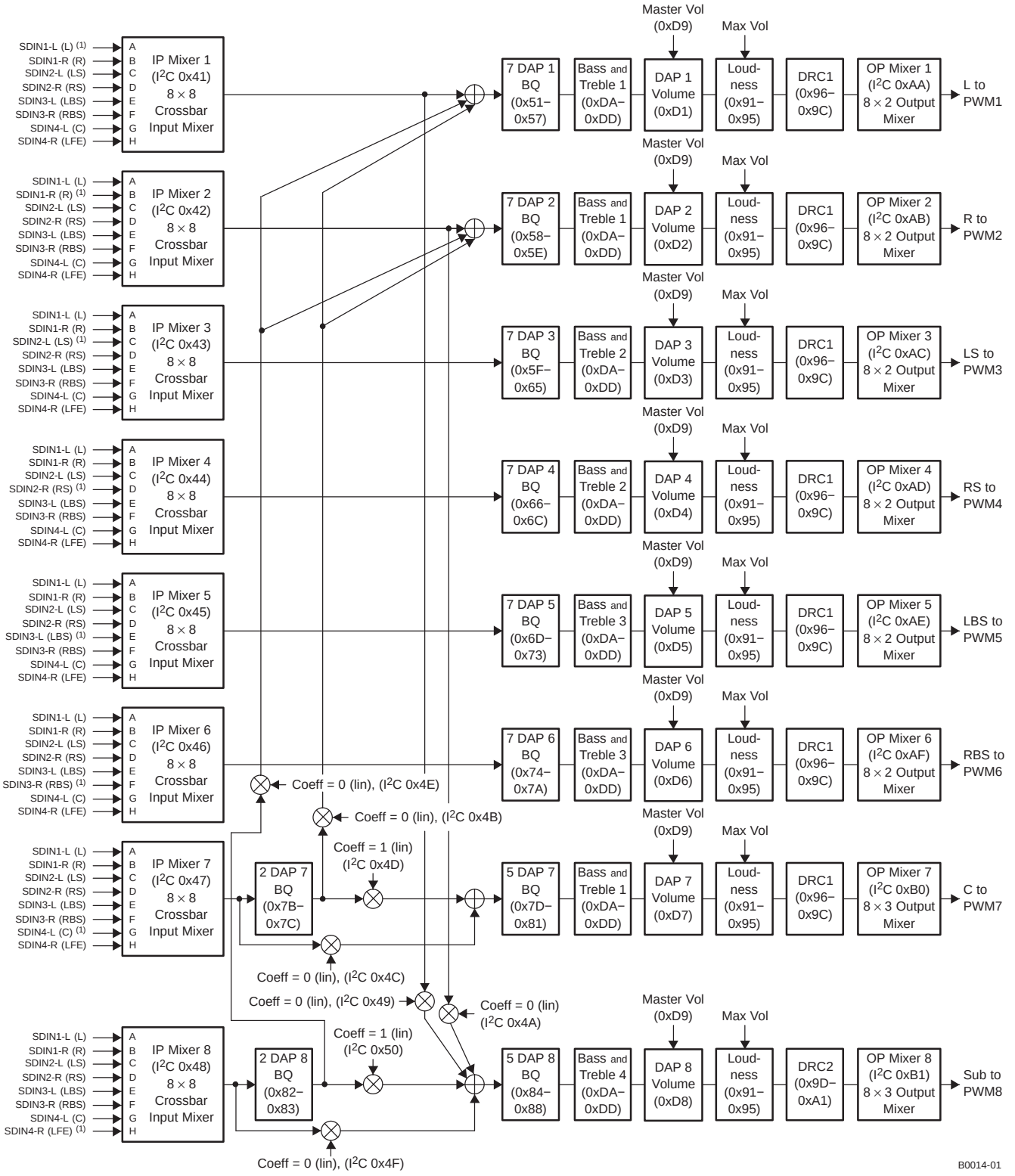
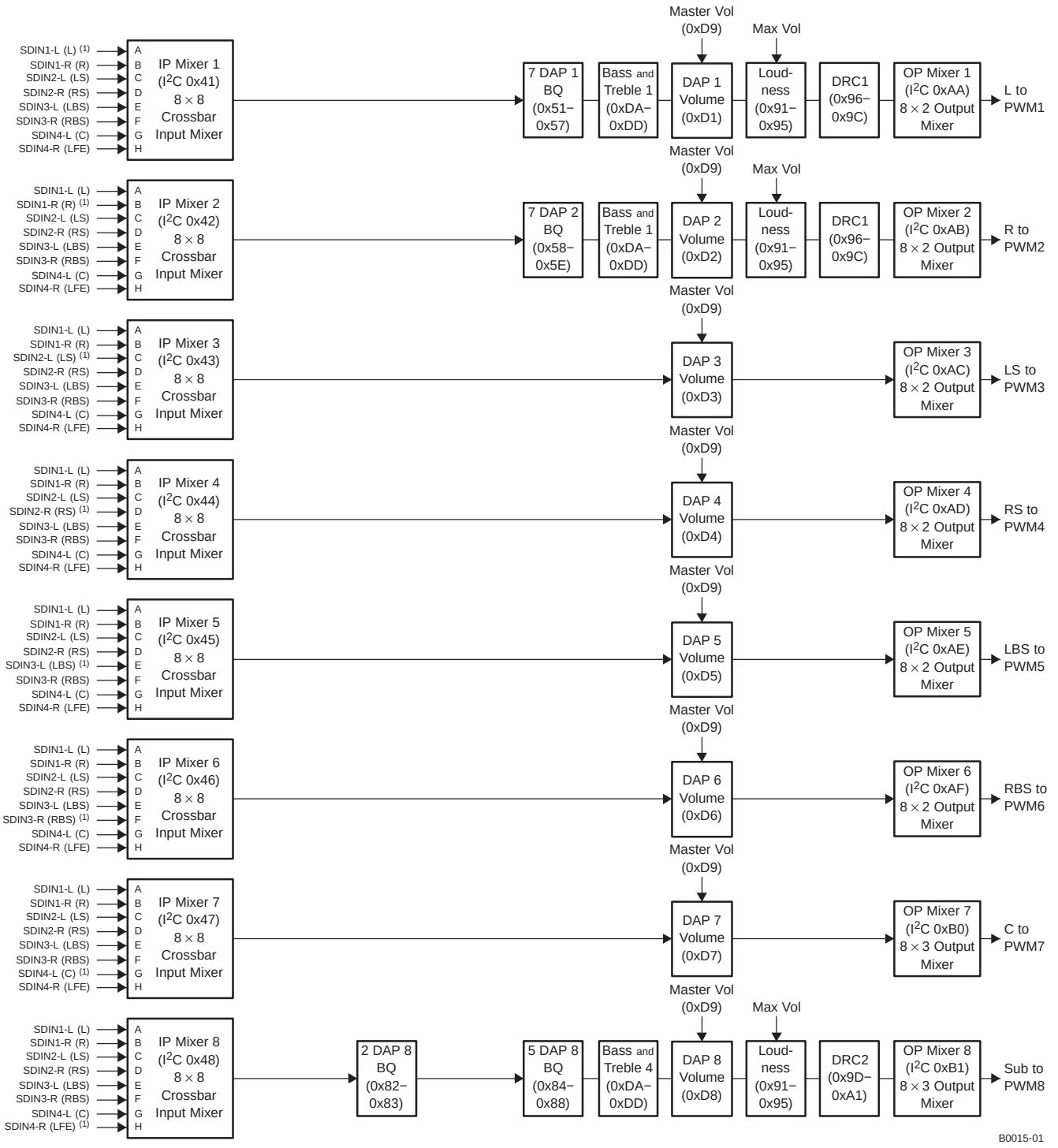


(1) Default inputs

Figure 2-1. TAS5518C DAP Architecture With I²C Registers ($f_S \leq 96$ kHz)

Not Recommended For New Designs



(1) Default inputs

Figure 2-2. TAS5518C Architecture With I²C Registers (f_S = 176.4 kHz or f_S = 192 kHz)

Not Recommended For New Designs

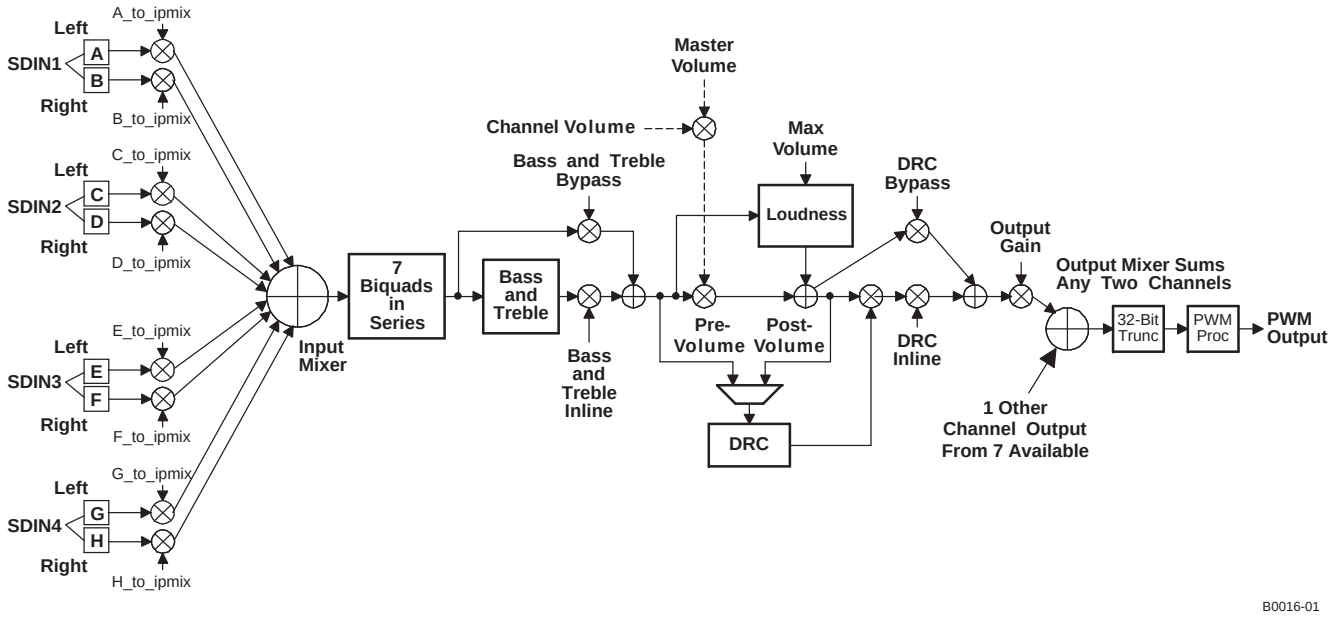


Figure 2-3. TAS5518C Detailed Channel Processing

2.3.2 I²C Coefficient Number Formats

The architecture of the TAS5518C is contained in ROM resources within the TAS5518C and cannot be altered. However, mixer gain, level offset, and filter tap coefficients, which can be entered via the I²C bus interface, provide a user with the flexibility to set the TAS5518C to a configuration that achieves system-level goals.

The firmware is executed in a 48-bit, signed, fixed-point arithmetic machine. The most significant bit of the 48-bit data path is a sign bit, and the 47 lower bits are data bits. Mixer gain operations are implemented by multiplying a 48-bit, signed data value by a 28-bit, signed gain coefficient. The 76-bit, signed output product is then truncated to a signed, 48-bit number. Level offset operations are implemented by adding a 48-bit, signed offset coefficient to a 48-bit, signed data value. In most cases, if the addition results in overflowing the 48-bit, signed number format, saturation logic is used. This means that if the summation results in a positive number that is greater than 0x7FFF FFFF FFFF (the spaces are used to ease the reading of the hexadecimal number), the number is set to 0x7FFF FFFF FFFF. If the summation results in a negative number that is less than 0x8000 0000 0000, the number is set to 0x8000 0000 0000.

2.3.2.1 28-Bit 5.23 Number Format

All mixer gain coefficients are 28-bit coefficients using a 5.23 number format. Numbers formatted as 5.23 numbers have 5 bits to the left of the binary point and 23 bits to the right of the binary point. This is shown in Figure 2-4.

Not Recommended For New Designs

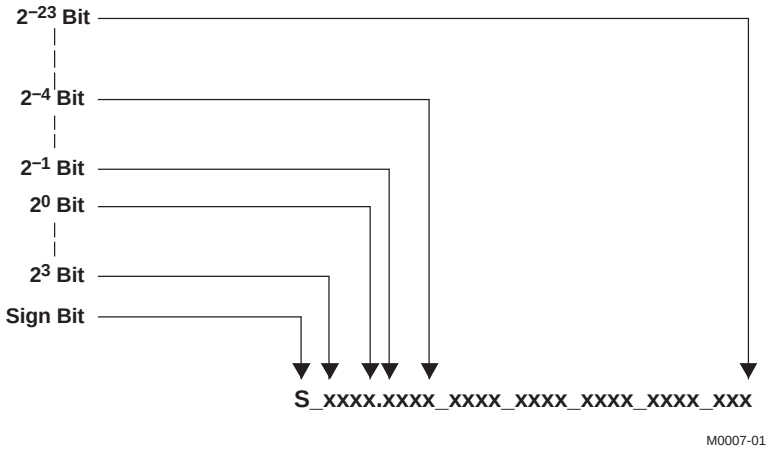


Figure 2-4. 5.23 Format

The decimal value of a 5.23 format number can be found by following the weighting shown in Figure 2-5. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case, every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 2-5 applied to obtain the magnitude of the negative number.

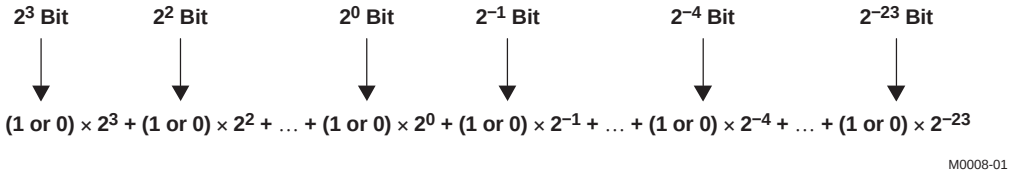


Figure 2-5. Conversion Weighting Factors—5.23 Format to Floating Point

Gain coefficients, entered via the I^2C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 2-6.

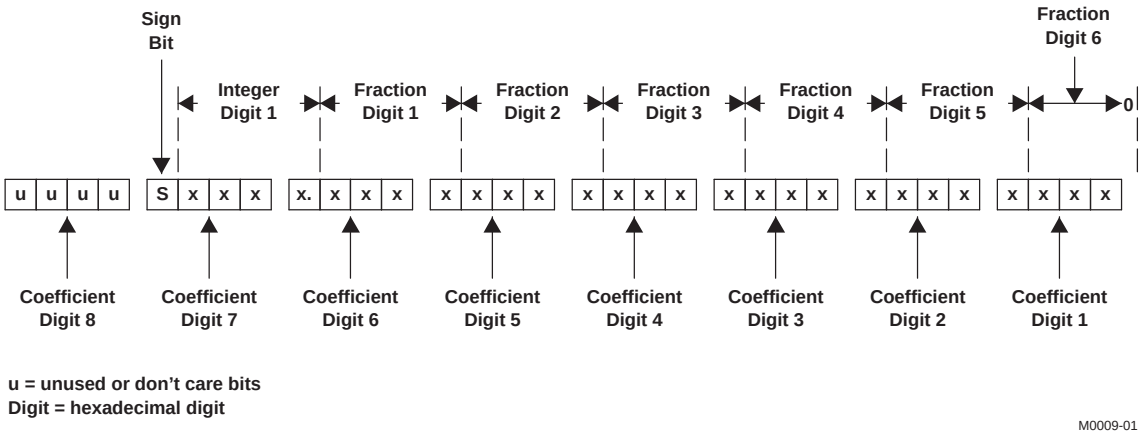


Figure 2-6. Alignment of 5.23 Coefficient in 32-Bit I^2C Word

As Figure 2-6 shows, the hexadecimal (hex) value of the integer part of the gain coefficient cannot be

concatenated with the hex value of the fractional part of the gain coefficient to form the 32-bit I^2C coefficient. The reason is that the 28-bit coefficient contains 5 bits of integer, and thus the integer part of the coefficient occupies all of one hex digit and the most significant bit of the second hex digit. In the same way, the fractional part occupies the lower three bits of the second hex digit, and then occupies the other five hex digits (with the eighth digit being the zero-valued most significant hex digit).

2.3.2.2 48-Bit 25.23 Number Format

All level adjustment and threshold coefficients are 48-bit coefficients using a 25.23 number format. Numbers formatted as 25.23 numbers have 25 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in Figure 2-7.

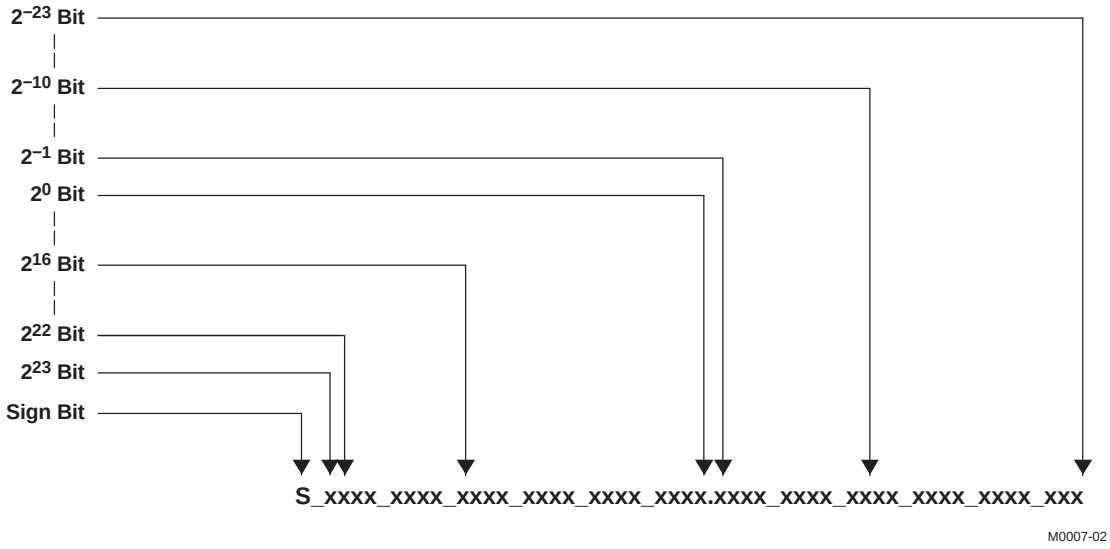


Figure 2-7. 25.23 Format

Figure 2-8 shows the derivation of the decimal value of a 48-bit 25.23 format number.

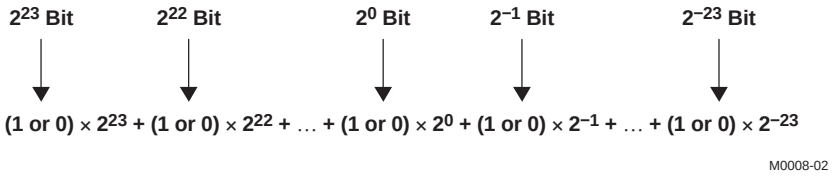


Figure 2-8. Conversion Weighting Factors—25.23 Format to Floating Point

Two 32-bit words must be sent over the I^2C bus to download a level or threshold coefficient into the TAS5518C. The alignment of the 48-bit, 25.23 formatted coefficient in the 8-byte (two 32-bit words) I^2C word is shown in Figure 2-9.

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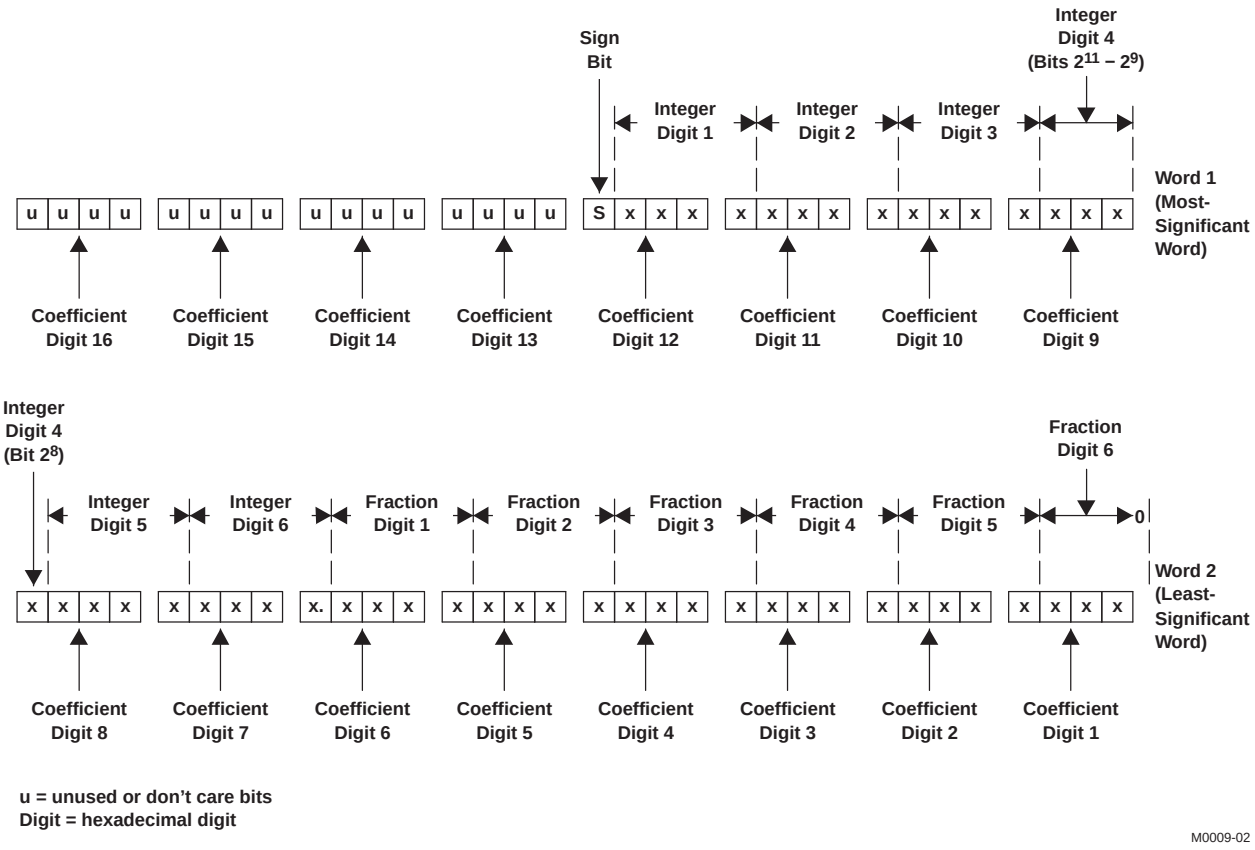

Figure 2-9. Alignment of 25.23 Coefficient in Two 32-Bit I²C Words

2.3.2.3 TAS5518C Audio Processing

The TAS5518C digital audio processing is designed so that noise produced by filter operations is maintained below the smallest signal amplitude of interest, as shown in Figure 2-10. The TAS5518C achieves this low noise level by increasing the precision of the signal representation substantially above the number of bits that are absolutely necessary to represent the input signal.

Similarly, the TAS5518C carries additional precision in the form of overflow bits to permit the value of intermediate calculations to exceed the input precision without clipping. The TAS5518C advanced digital audio processor achieves both of these important performance capabilities by using a high-performance digital audio-processing architecture with a 48-bit data path, 28-bit filter coefficients, and a 76-bit accumulator.

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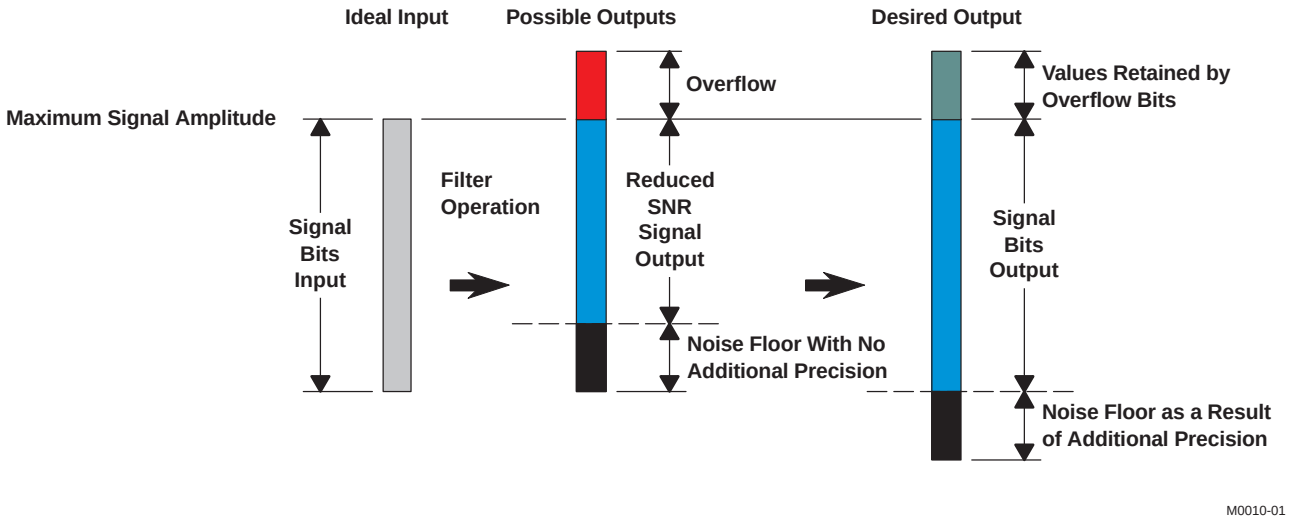

Figure 2-10. TAS5518C Digital Audio Processing

2.4 Input Crossbar Mixer

The TAS5518C has a full 8×8 input crossbar mixer. This mixer permits each signal-processing channel input to be any mix of any of the eight input channels, as shown in Figure 2-11. The control parameters for the input crossbar mixer are programmable via the I^2C interface. See the *Input Mixer Registers, Channels 1–8 (0x41–0x48)*, Section 7.14, for more information.

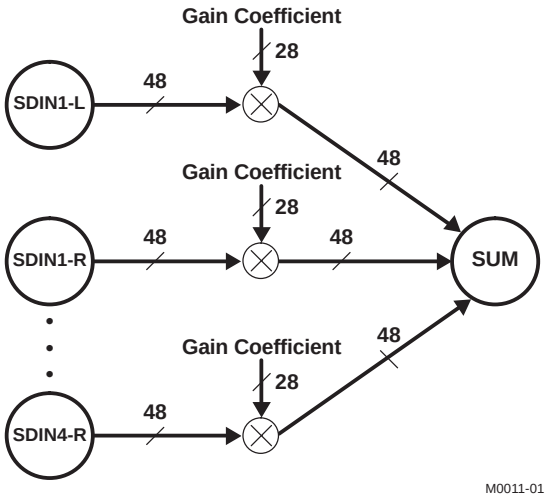

Figure 2-11. Input Crossbar Mixer

2.5 Biquad Filters

For 32-kHz to 96-kHz data, the TAS5518C provides 56 biquads across the eight channels (seven per channel).

For 176.4-kHz and 192-kHz data, the TAS5518C has 21 biquads across the three channels (seven per channel). All of the biquad filters are second-order direct form I structure.

Not Recommended For New Designs

The direct form I structure provides a separate delay element and mixer (gain coefficient) for each node in the biquad filter. Each mixer output is a signed 76-bit product of a signed 48-bit data sample (25.23 format number) and a signed 28-bit coefficient (5.23 format number), as shown in Figure 2-12. The 76-bit ALU in the TAS5518C allows the 76-bit resolution to be retained when summing the mixer outputs (filter products).

The five 28-bit coefficients for the each of the 56 biquads are programmable via the I²C interface. See Table 2-3.

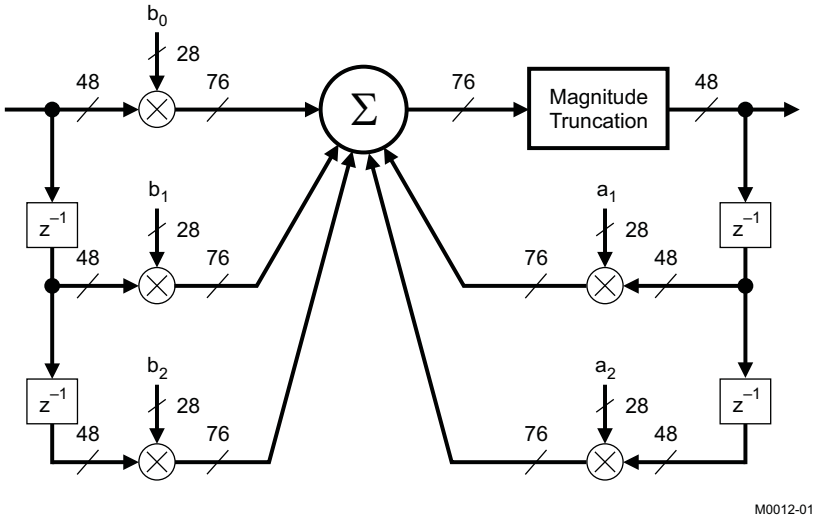

Figure 2-12. Biquad Filter Structure

All five coefficients for one biquad filter structure are written to one I²C register containing 20 bytes (or five 32-bit words). The structure is the same for all biquads in the TAS5518C. Registers 0x51–0x88 show all the biquads in the TAS5518C. Note that u[31:28] bits are unused and default to 0x0.

Table 2-3. Contents of One 20-Byte Biquad Filter Register (Default = All-Pass)

DESCRIPTION	REGISTER FIELD CONTENTS	INITIALIZATION GAIN COEFFICIENT VALUE	
		DECIMAL	HEX
b_0 coefficient	u[31:28], b0[27:24], b0[23:16], b0[15:8], b0[7:0]	**1.0**	**0x00, 0x80, 0x00, 0x00**
b_1 coefficient	u[31:28], b1[27:24], b1[23:16], b1[15:8], b1[7:0]	0.0	0x00, 0x00, 0x00, 0x00
b_2 coefficient	u[31:28], b2[27:24], b2[23:16], b2[15:8], b2[7:0]	0.0	0x00, 0x00, 0x00, 0x00
a_1 coefficient	u[31:28], a1[27:24], a1[23:16], a1[15:8], a1[7:0]	0.0	0x00, 0x00, 0x00, 0x00
a_2 coefficient	u[31:28], a2[27:24], a2[23:16], a2[15:8], a2[7:0]	0.0	0x00, 0x00, 0x00, 0x00

2.6 Bass and Treble Controls

From 32-kHz to 96-kHz data, the TAS5518C has four bass and treble tone controls. Each control has a ±18-dB control range with selectable corner frequencies and second-order slopes. These controls operate four channel groups:

- L, R, and C (channels 1, 2, and 7)
- LS, RS (channels 3 and 4)
- LBS, RBS (alternatively called L and R lineout) (channels 5 and 6)
- Sub (channel 8)

For 176.4-kHz and 192-kHz data, the TAS5518C has two bass and treble tone controls. Each control has a ±18-dB I²C control range with selectable corner frequencies and second-order slopes. These controls operate two channel groups:

- L and R
- Sub

The bass and treble filters use a soft update rate that does not produce artifacts during adjustment.

Table 2-4. Bass and Treble Filter Selections

f_S (kHz)	3-dB CORNER FREQUENCIES, Hz									
	FILTER SET 1		FILTER SET 2		FILTER SET 3		FILTER SET 4		FILTER SET 5	
	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE
32	42	917	83	1833	125	3000	146	3667	167	4333
38	49	1088	99	2177	148	3562	173	4354	198	5146
44.1	57	1263	115	2527	172	4134	201	5053	230	5972
48	63	1375	125	2750	188	4500	219	5500	250	6500
88.2	115	2527	230	5053	345	8269	402	10106	459	11944
96	125	2750	250	5500	375	9000	438	11000	500	13000
176.4	230	5053	459	10106	689	16538	804	20213	919	23888
192	250	5500	500	11000	750	18000	875	22000	1000	26000

The I^2C registers that control bass and treble are:

- Bass and treble bypass register (0x89–0x90, channels 1–8)
- Bass and treble slew rates (0xD0)
- Bass filter sets 1–5 (0xDA)
- Bass filter index (0xDB)
- Treble filter sets 1–5 (0xDC)
- Treble filter index (0xDD)

NOTE

The bass and treble bypass registers (0x89–0x90) are defaulted to the bypass mode. In order to use the bass and treble, these registers must be in the inline (or enabled) mode for each channel using bass and treble.

2.7 Volume, Automute, and Mute

The TAS5518C provides individual channel and master volume controls. Each control provides an adjustment range of 18 dB to –100 dB in 0.25-dB increments. This permits a total volume device control range of 36 dB to –127 dB plus mute. The master volume control can be configured to control six or eight channels.

The TAS5518C has a master soft mute control that can be enabled by a terminal or I^2C command. The device also has individual channel soft mute controls that are enabled via I^2C.

The soft volume and mute update rates are programmable. The soft adjustments are performed using a soft-gain linear update with an I^2C-programmable linear step size at a fixed temporal rate. The linear soft-gain step size can be varied from 0.5 to 0.003906. Table 2-5 lists the linear gain step sizes.

Table 2-5. Linear Gain Step Size

STEP SIZE (GAIN)	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.007813	0.003906
Time to go from 36.124 db to –127 dB in ms	10.67	21.33	42.67	85.34	170.67	341.35	682.70	1365.4
Time to go from 18.062 db to –127 dB in ms	1.33	2.67	5.33	10.67	21.33	42.67	85.33	170.67
Time to go from 0 db to –127 dB in ms	0.17	0.33	0.67	1.33	2.67	5.33	10.67	21.33

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2.8 Automute and Mute Channel Controls

The TAS5518C has individual channel automute controls that are enabled via I^2C register 0x04 bits D5 and D6 (the default setting is **enabled**). Two separate detectors can trigger the automute:

- Input automute (I^2C register 0x14): All channels are muted when all 8 inputs to the TAS5518C are less in magnitude than the input threshold value for a programmable amount of time.
- Output automute (I^2C register 0x15): A single channel is muted when the output of the DAP section is less in magnitude than the input threshold value for a programmable amount of time.

The detection period and thresholds for these two detectors are the same.

This time interval is selectable via I^2C to be from 1 ms to 110 ms. The increments of time are 1, 2, 3, 4, 5, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, and 110 ms. This interval is independent of the sample rate. The default value is mask programmable.

The input threshold value is an unsigned magnitude that is expressed as a bit position. This value is adjustable via I^2C. The range of the input threshold adjustment is from below the LSB (bit position 0) to below bit position 12 in a 24-bit input-data word. This range provides an input threshold that can be adjusted for 12 to 24 bits of data. The default value is mask programmable.

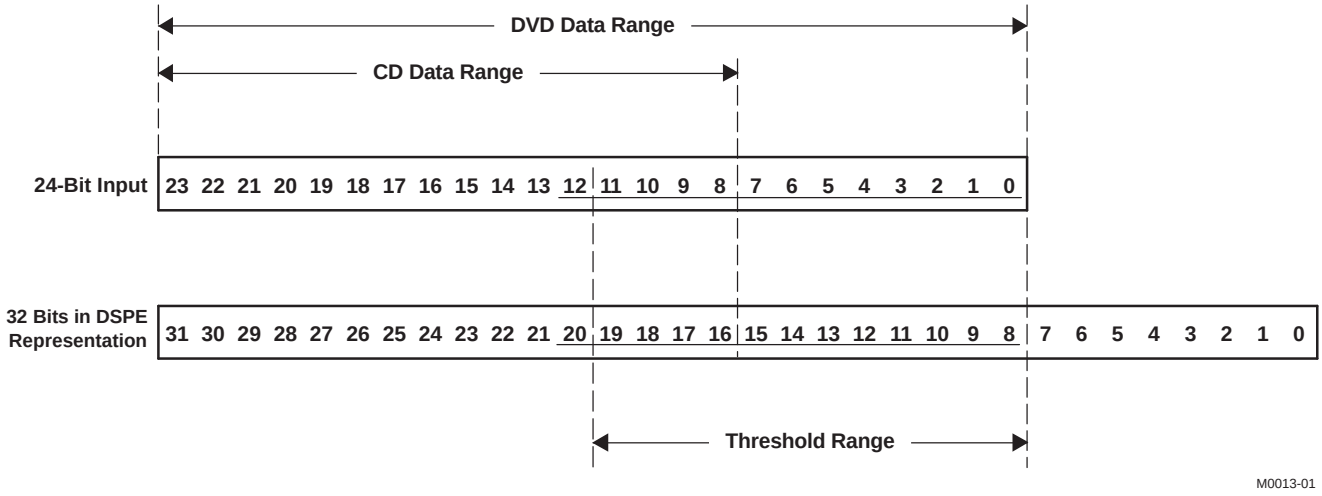

Figure 2-13. Automute Threshold

The automute state is exited when the TAS5518C receives one sample that is greater than the output threshold.

The output threshold can be one of two values:

- Equal to the input threshold
- 6 dB (one bit position) greater than the input threshold

The value for the output threshold is selectable via I^2C. The default value is mask programmable.

The system latency enables the data value that is above the threshold to be preserved and output.

A mute command initiated by automute, master mute, individual I^2C mute, the AM interference mute sequence, or the bank-switch mute sequence overrides an unmute command or a volume command. While a mute command is activated, the commanded channels transition to the mute state. When a channel is unmuted, it goes to the last commanded volume setting that has been received for that channel.

2.9 Loudness Compensation

The loudness compensation function compensates for the Fletcher-Munson loudness curves. The

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TAS5518C loudness implementation tracks the volume control setting to provide spectral compensation for weak low- or high-frequency response at low volume levels. For the volume tracking function, both linear and logarithmic control laws can be implemented. Any biquad filter response can be used to provide the desired loudness curve. The control parameters for the loudness control are programmable via the I^2C interface.

The TAS5518C has a single set of loudness controls for the eight channels. In 6-channel mode, loudness is available to the six speaker outputs and also to the line outputs. The loudness control input uses the maximum individual master volume (V) to control the loudness that is applied to all channels. In the 192-kHz and 176.4-kHz modes, the loudness function is active only for channels 1, 2, and 8.

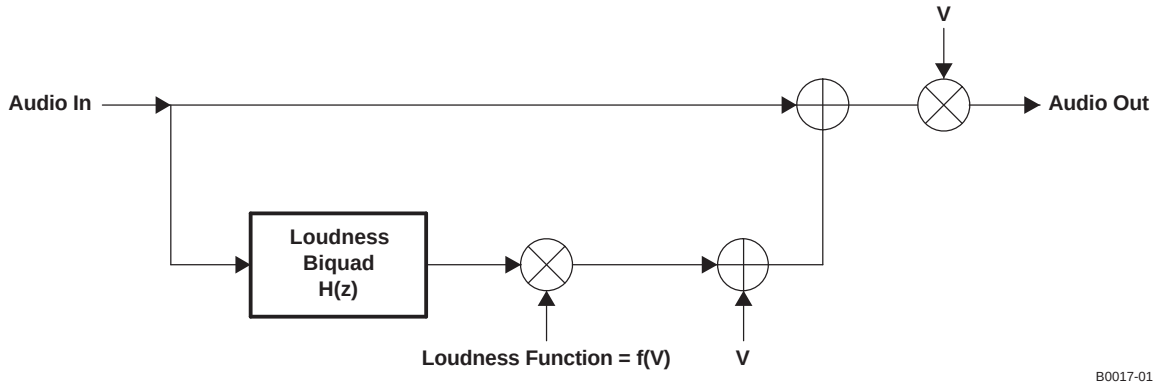

Figure 2-14. Loudness Compensation Functional Block Diagram

Loudness function = f(V) = G × [$2^{(\text{Log V}) \times \text{LG} + \text{LO}}$] + O or alternatively,

Loudness function = f(V) = G × [$V^{LG} \times 2^{LO}$] + O

For example, for the default values LG = –0.5, LO = 0, G = 1, and O = 0, then:

Loudness function = 1/SQRT(V), which is the recommended transfer function for loudness. So,

Audio out = (audio in) × V + H(Z) × SQRT(V). Other transfer functions are possible.

Table 2-6. Default Loudness Compensation Parameters

LOUDNESS TERM	DESCRIPTION	USAGE	DATA FORMAT	I^2C SUB-ADDRESS	DEFAULT	
					HEX	FLOAT
V	Max volume	Gains audio	5.23	NA	NA	NA
Log V	Log_2 (max volume)	Loudness function	5.23	NA	0000 0000	0.0
H(Z)	Loudness biquad	Controls shape of loudness curves	5.23	0x95	b_0 = 0000 D513 b_1 = 0000 0000 b_2 = 0FFF 2AED a_1 = 00FE 5045 a_2 = 0F81 AA27	b_0 = 0.006503 b_1 = 0 b_2 = –0.006503 a_1 = 1.986825 a_2 = –0.986995
LG	Gain (log space)	Loudness function	5.23	0x91	FFC0 0000	–0.5
LO	Offset (log space)	Loudness function	25.23	0x92	0000 0000	0
G	Gain	Switch to enable loudness (ON = 1, OFF = 0)	5.23	0x93	0000 0000	0
O	Offset	Provides offset	25.23	0x94	0000 0000	0

2.9.1 Loudness Example

Problem: Due to the Fletcher-Munson phenomena, compensation for low-frequency attenuation near 60 Hz is desirable. The TAS5518C provides a loudness transfer function with EQ gain = 6, EQ center frequency = 60 Hz, and EQ bandwidth = 60 Hz.

Solution: Using Texas Instruments ALE TAS5518C DSP tool, Matlab™, or other signal-processing tool, develop a loudness function with the parameters listed in Table 2-7.

Table 2-7. Example Loudness Function Parameters

LOUDNESS TERM	DESCRIPTION	USAGE	DATA FORMAT	I^2C SUB-ADDRESS	EXAMPLE	
					HEX	FLOAT
H(Z)	Loudness biquad	Controls shape of loudness curves	5.23	0x95	b_0 = 0000 8ACE b_1 = 0000 0000 b_2 = FFFF 7532 a_1 = FF01 1951 a_2 = 007E E914	b_0 = 0.004236 b_1 = 0 b_2 = –0.004236 a_1 = –1.991415 a_2 = 0.991488
LG	Loudness gain	Loudness function	5.23	0x91	FFC0 0000	–0.5
LO	Loudness offset	Loudness function	25.23	0x92	0000 0000	0
G	Gain	Switch to enable loudness (ON = 1, OFF = 0)	5.23	0x93	0080 0000	1
O	Offset	Offset	25.23	0x94	0000 0000	0

See Figure 2-15 for the resulting loudness function at different gains.

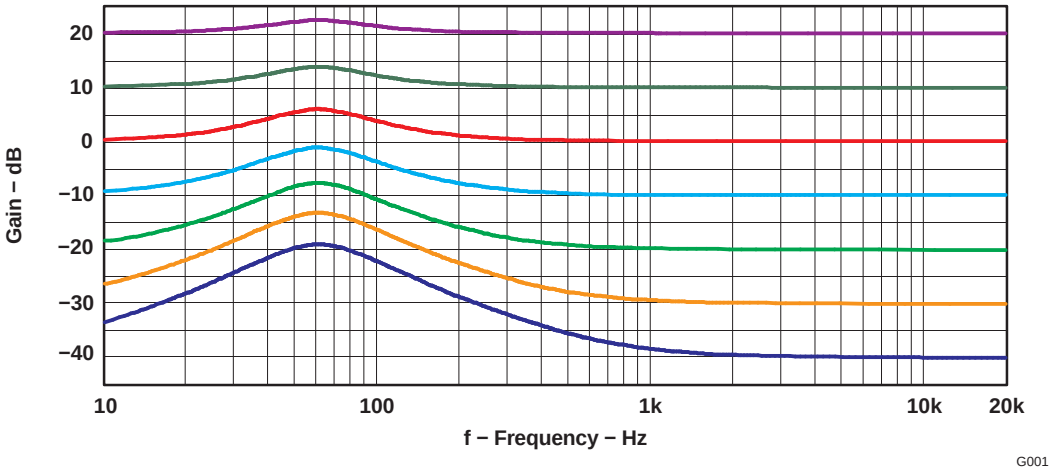

Figure 2-15. Loudness Example Plots

2.10 Dynamic Range Control (DRC)

DRC provides both compression and expansion capabilities over three separate and definable regions of audio signal levels. Programmable threshold levels set the boundaries of the three regions. Within each of the three regions, a distinct compression or expansion transfer function can be established and the slope of each transfer function is determined by programmable parameters. The offset (boost or cut) at the two boundaries defining the three regions can also be set by programmable offset coefficients. The DRC implements the composite transfer function by computing a 5.23-format gain coefficient from each sample output from the rms estimator. This gain coefficient is then applied to a mixer element, whose other input is the audio data stream. The mixer output is the DRC-adjusted audio data.

The TAS5518C has two distinct DRC blocks. DRC1 services channels 1–7 in the 8-channel mode and channels 1–4 and 7 in the 6-channel mode. This DRC computes rms estimates of the audio data streams on all channels that it controls. The estimates are then compared on a sample-by-sample basis and the larger of the estimates is used to compute the compression/expansion gain coefficient. The gain coefficient is then applied to the appropriate channel audio streams. DRC2 services only channel 8. This DRC also computes an rms estimate of the signal level on channel 8 and this estimate is used to compute the compression/expansion gain coefficient applied to the channel-8 audio stream.

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All of the TAS5518C default values for DRC can be used except for the DRC1 decay and DRC2 decay. Table 2-8 shows the recommended time constants and their hex values. If the user wants to implement other DRC functions, Texas Instruments recommends using the automatic loudspeaker equalization (ALE) tool available from Texas Instruments. The ALE tool allows the user to select the DRC transfer function graphically. It then outputs the TAS5518C hex coefficients for download to the TAS5518C.

Table 2-8. DRC Recommended Changes From TAS5518C Defaults

I^2C SUBADDRESS	REGISTER FIELDS	RECOMMENDED TIME CONSTANT (ms)	RECOMMENDED HEX VALUE	DEFAULT HEX
0x98	DRC1 energy	5	0000 883F	0000 883F
	DRC1 (1 – energy)		007F 77C0	007F 77C0
0x9C	DRC1 attack	5	0000 883F	0000 883F
	DRC1 (1 – attack)		007F 77C0	007F 77C0
	DRC1 decay	2	0001 538F	0000 00AE
	DRC1 (1 – decay)		007E AC70	007F FF51
0x9D	DRC2 energy	5	0000 883F	0000 883F
	DRC2 (1 – energy)		007F 77C0	007F 77C0
0xA1	DRC2 attack	5	0000 883F	0000 883F
	DRC2 (1 – attack)		007F 77C0	007F 77C0
	DRC2 decay	2	0001 538F	0000 0056
	DRC2 (1 – decay)		007E AC70	003F FFA8

Recommended DRC setup flow if the defaults are used:

- After power up, load the recommended hex value for DRC1 and DRC2 decay and (1 – decay). See Table 2-8.
- Enable either the pre-volume or post-volume DRC using I^2C registers 0x96 and 0x97. Note that to avoid a potential timing problem, there should be a 10-ms delay between a write to 0x96 and a write to 0x97.

Recommended DRC setup flow if the DRC design uses values different from the defaults:

- After power up, load all DRC coefficients per the DRC design.
- Enable either the pre-volume or post-volume DRC. Note that to avoid a potential timing problem, there should be a 10-ms delay between a write to 0x96 and a write to 0x97.

Figure 2-16 shows the positioning of the DRC block in the TAS5518C processing flow. As seen, the DRC input can come either before or after soft volume control and loudness processing.

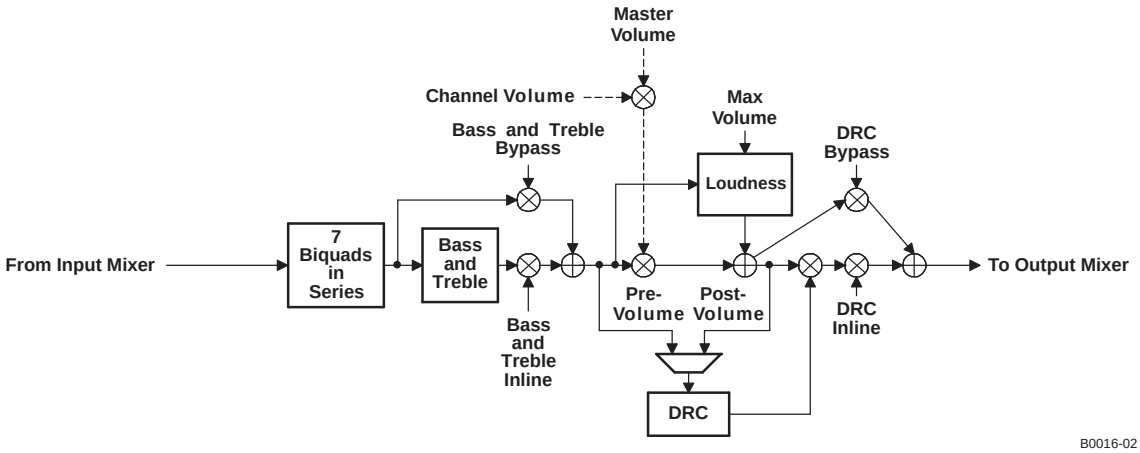

Figure 2-16. DRC Positioning in TAS5518C Processing Flow

Figure 2-17 illustrates a typical DRC transfer function.

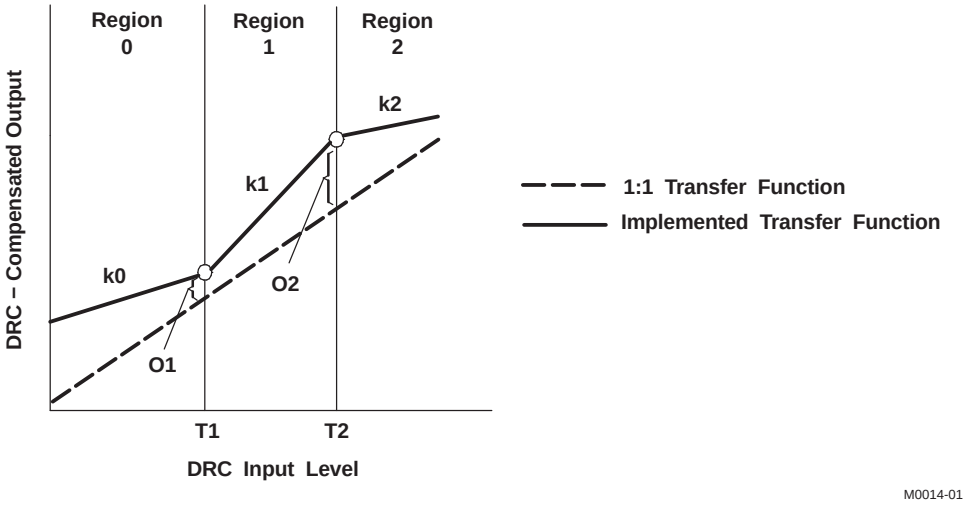

Figure 2-17. Dynamic Range Compression (DRC) Transfer Function Structure

The three regions shown in Figure 2-17 are defined by three sets of programmable coefficients:

- Thresholds T1 and T2 define region boundaries.
- Offsets O1 and O2 define the DRC gain coefficient settings at thresholds T1 and T2, respectively.
- Slopes k0, k1, and k2 define whether compression or expansion is to be performed within a given region. The magnitudes of the slopes define the degree of compression or expansion to be performed.

The three sets of parameters are all defined in logarithmic space and adhere to the following rules:

- The maximum input sample into the DRC is referenced at 0 dB. All values below this maximum value then have negative values in logarithmic (dB) space.
- The samples input into the DRC are 32-bit words and consist of the upper 32 bits of the 48-bit word format used by the digital audio processor (DAP). The 48-bit DAP word is derived from the 32-bit serial data received at the serial-audio receive port by adding 8 bits of headroom above the 32-bit word and 8 bits of computational precision below the 32-bit word. If the audio-processing steps between the SAP input and the DRC input result in no accumulative boost or cut, the DRC operates on the 8 bits of headroom and the 24 MSBs of the audio sample. Under these conditions, a 0-dB (maximum value) audio sample (0x7FFF FFFF) is seen at the DRC input as a –48-dB sample (8 bits × –6 dB/bit = –48 dB).
- Thresholds T1 and T2 define, in dB, the boundaries of the three regions of the DRC, as referenced to the rms value of the data into the DRC. Zero-valued threshold settings reference the maximum-valued rms input into the DRC and negative-valued thresholds reference all other rms input levels. Positive-valued thresholds have no physical meaning and are not allowed. In addition, zero-valued threshold settings are not allowed.

Although the DRC input is limited to 32-bit words, the DRC itself operates using the 48-bit word format of the DAP. The 32-bit samples input into the DRC are placed in the upper 32 bits of this 48-bit word space. This means that the threshold settings must be programmed as 48-bit (25.23 format) numbers.

CAUTION

Zero-valued and positive-valued threshold settings are not allowed and cause unpredictable behavior if used.

- Offsets O1 and O2 define, in dB, the attenuation (cut) or gain (boost) applied by the DRC-derived gain coefficient at the threshold points T1 and T2, respectively. Positive offsets are defined as cuts, and thus boost or gain selections are negative numbers. Offsets must be programmed as 48-bit (25.23 format) numbers.

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- Slopes k0, k1, and k2 define whether compression or expansion is to be performed within a given region, and the degree of compression or expansion to be applied. Slopes are programmed as 28-bit (5.23 format) numbers.

2.10.1 DRC Implementation

The three elements comprising the DRC include: (1) an rms estimator, (2) a compression/expansion coefficient computation engine, and (3) an attack/decay controller.

- RMS estimator—This DRC element derives an estimate of the rms value of the audio data stream into the DRC. For the DRC block shared by Ch1 and Ch2, two estimates are computed—an estimate of the Ch1 audio data stream into the DRC, and an estimate of the Ch2 audio data stream into the DRC. The outputs of the two estimators are then compared, sample-by-sample, and the larger-valued sample is forwarded to the compression/expansion coefficient computation engine.
  Two programmable parameters, ae and (1 – ae), set the effective time window over which the rms estimate is made. For the DRC block shared by Ch1 and Ch2, the programmable parameters apply to both rms estimators. The time window over which the rms estimation is computed can be determined by:

$$t_{window} = \frac{-1}{f_S \, \ell n(1 - ae)}$$

- Compression/expansion coefficient computation—This DRC element converts the output of the rms estimator to a logarithmic number, determines the region where the input resides, and then computes and outputs the appropriate coefficient to the attack/decay element. Seven programmable parameters, T1, T2, O1, O2, k0, k1, and k2, define the three compression/expansion regions implemented by this element.
- Attack/decay control—This DRC element controls the transition time of changes in the coefficient computed in the compression/expansion coefficient computation element. Four programmable parameters define the operation of this element. Parameters ad and (1 – ad) set the decay or release time constant to be used for volume boost (expansion). Parameters aa and (1 – aa) set the attack time constant to be used for volume cuts. The transition time constants can be determined by:

$$t_a = \frac{-1}{f_S \, \ell n(1 - aa)} \qquad t_d = \frac{-1}{f_S \, \ell n(1 - ad)}$$

2.10.2 Compression/Expansion Coefficient Computation Engine Parameters

Seven programmable parameters are assigned to each DRC block: two threshold parameters—T1 and T2, two offset parameters—O1 and O2, and three slope parameters—k0, k1, and k2. The threshold parameters establish the three regions of the DRC transfer curve, the offsets anchor the transfer curve by establishing known gain settings at the threshold levels, and the slope parameters define whether a given region is a compression or an expansion region.

The audio input stream into the DRC must pass through DRC-dedicated programmable input mixers. These mixers are provided to scale the 32-bit input into the DRC to account for the positioning of the audio data in the 48-bit DAP word and the net gain or attenuation in signal level between the SAP input and the DRC. The selection of threshold values must take the gain (attenuation) of these mixers into account. The DRC implementation examples that follow illustrate the effect these mixers have on establishing the threshold settings.

T2 establishes the boundary between the high-volume region and the mid-volume region. T1 establishes the boundary between the mid-volume region and the low-volume region. Both thresholds are set in logarithmic space, and which region is active for any given rms estimator output sample is determined by the logarithmic value of the sample.

Threshold T2 serves as the fulcrum or pivot point in the DRC transfer function. O2 defines the boost (> 0 dB) or cut (< 0 dB) implemented by the DRC-derived gain coefficient for an rms input level of T2. If O2 = 0 dB, the value of the derived gain coefficient is 1 (0x0080 0000 in 5.23 format). k2 is the slope of the DRC transfer function for rms input levels above T2, and k1 is the slope of the DRC transfer function for rms input levels below T2 (and above T1). The labeling of T2 as the fulcrum stems from the fact that there cannot be a discontinuity in the transfer function at T2. The user can, however, set the DRC parameters to realize a discontinuity in the transfer function at the boundary defined by T1. If no discontinuity is desired at T1, the value for the offset term O1 must obey the following equation.

$$O1_{\text{No Discontinuity}} = |T1 - T2| \times k1 + O2 \quad \text{For } (|T1| \geq |T2|)$$

T1 and T2 are the threshold settings in dB, k1 is the slope for region 1, and O2 is the offset in dB at T2. If the user chooses to select a value of O1 that does not obey the above equation, a discontinuity at T1 is realized.

Decreasing in volume from T2, the slope k1 remains in effect until the input level T1 is reached. If, at this input level, the offset of the transfer function curve from the 1 : 1 transfer curve does not equal O1, there is a discontinuity at this input level as the transfer function is snapped to the offset called for by O1. If no discontinuity is wanted, O1 and/or k1 must be adjusted so that the value of the transfer curve at input level T1 is offset from the 1 : 1 transfer curve by the value O1. The examples that follow illustrate both continuous and discontinuous transfer curves at T1.

Decreasing in volume from T1, starting at offset level O1, slope k0 defines the compression/expansion activity in the lower region of the DRC transfer curve.

2.10.2.1 Threshold Parameter Computation

For thresholds,

$$T_{dB} = -6.0206T_{INPUT} = -6.0206T_{SUB_ADDRESS_ENTRY}$$

If, for example, it is desired to set T1 = –64 dB, then the subaddress entry required to set T1 to –64 dB is:

$$T1_{SUB_ADDRESS_ENTRY} = \frac{-64}{-6.0206} = 10.63$$

T1 is entered as a 48-bit number in 25.23 format. Therefore:

T1 = 10.63 = 0 1010.1010 0001 0100 0111 1010 111

= 0x0000 0550 A3D7 in 25.23 format

2.10.2.2 Offset Parameter Computation

The offsets set the boost or cut applied by the DRC-derived gain coefficient at the threshold point. An equivalent statement is that offsets represent the departure of the actual transfer function from a 1 : 1 transfer at the threshold point. Offsets are 25.23-formatted, 48-bit logarithmic numbers. They are computed by the following equation.

$$O_{INPUT} = \frac{O_{DESIRED} + 24.0824\ \text{dB}}{6.0206}$$

Gains or boosts are represented as negative numbers; cuts or attenuations are represented as positive numbers. For example, to achieve a boost of 21 dB at threshold T1, the I^2C coefficient value entered for O1 must be:

$$O1_{INPUT} = \frac{-21\ \text{dB} + 24.0824\ \text{dB}}{6.0206} = 0.51197555$$

$$= 0.1000_0011_0001_1101_0100$$

$$= 0x00000041886A \text{ in } 25.23 \text{ format}$$

Not Recommended For New Designs

2.10.2.3 Slope Parameter Computation

In developing the equations used to determine the subaddress of the input value required to realize a given compression or expansion within a given region of the DRC, the following convention is adopted.

DRC transfer = Input increase : Output increase

If the DRC realizes an output increase of n dB for every dB increase in the rms value of the audio into the DRC, a 1 : n expansion is being performed. If the DRC realizes a 1-dB increase in output level for every n-dB increase in the rms value of the audio into the DRC, an n : 1 compression is being performed.

$k = n - 1$

For n : 1 compression, the slope k can be found by: $k = \frac{1}{n} - 1$

In both expansion (1 : n) and compression (n : 1), n is implied to be greater than 1. Thus, for expansion:

$k = n - 1$ means $k > 0$ for $n > 1$. Likewise, for compression, $k = \frac{1}{n} - 1$ means $-1 < k < 0$ for $n > 1$. Thus, it appears that k must always lie in the range $k > -1$.

The DRC imposes no such restriction and k can be programmed to values as negative as –15.999. To determine what results when such values of k are entered, it is first helpful to note that the compression and expansion equations for k are actually the same equation. For example, a 1 : 2 expansion is also a 0.5 : 1 compression.

$$0.5:1 \text{ compression} \Rightarrow k = \frac{1}{0.5} - 1 = 1$$

$$1:2 \text{ expansion} \Rightarrow k = 2 - 1 = 1$$

As can be seen, the same value for k is obtained either way. The ability to choose values of k less than –1 allows the DRC to implement negative-slope transfer curves within a given region. Negative-slope transfer curves are usually not associated with compression and expansion operations, but the definition of these operations can be expanded to include negative-slope transfer functions. For example, if k = –4

$$\text{Compression equation: } k = -4 = \frac{1}{n} - 1 \Rightarrow n = -\frac{1}{3} \Rightarrow -0.3333:1 \text{ compression}$$

$$\text{Expansion equation: } k = -4 = n - 1 \Rightarrow n = -3 \Rightarrow 1:-3 \text{ expansion}$$

With k = –4, the output decreases 3 dB for every 1 dB increase in the rms value of the audio into the DRC. As the input increases in volume, the output decreases in volume.

2.11 Output Mixer

The TAS5518C provides an 8×2 output mixer for channels 1, 2, 3, 4, 5, and 6. For channels 7 and 8, the TAS5518C provides an 8×3 output mixer. These mixers allow each output to be any mix of any two (or three) signal-processed channels. The control parameters for the output crossbar mixer are programmable via the I^2C interface. All of the TAS5518C features are available when the 8×2 and 8×3 output mixers are configured in the pass-through output mixer configuration, where the audio data from each DAP channel maps directly to the corresponding PWM channel (i.e., DAP channel 1 to PWM channel 1, etc).

When mixing or remapping DAP channels to different PWM output channels there are limitations to consider:

- Individual channel mute should not be used.
- The sum of the minimum channel volume and master volume should not be below –109 dB.

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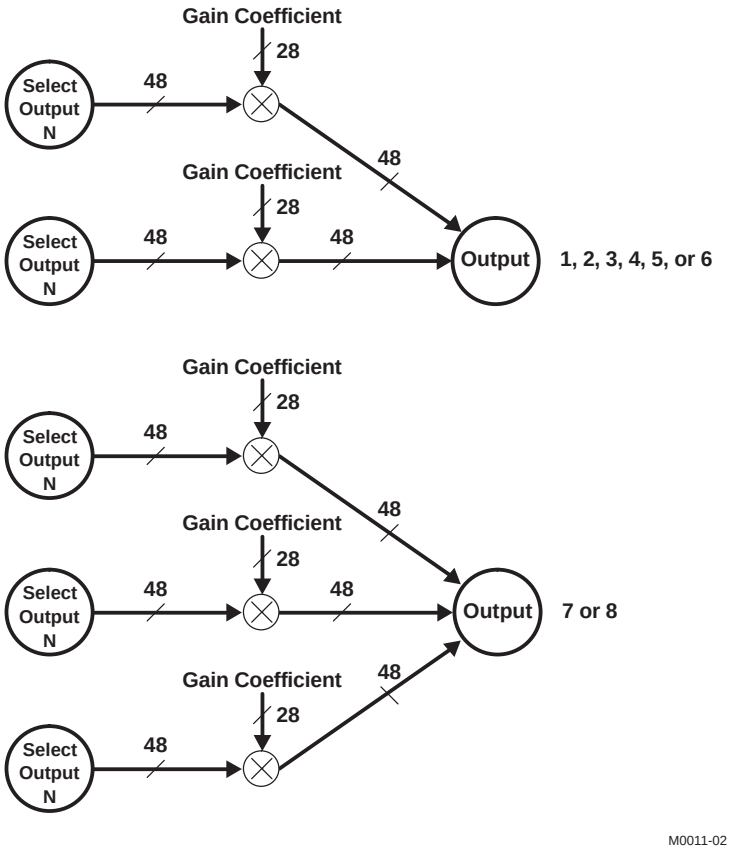

Figure 2-18. Output Mixers

2.12 PWM

The TAS5518C has eight channels of high-performance digital PWM modulators that are designed to drive switching output stages (back ends) in both single-ended (SE) and H-bridge (bridge-tied-load) configurations. The TAS5518C device uses noise-shaping and sophisticated, error-correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The TAS5518C uses an AD1 PWM modulation scheme combined with a fifth-order noise shaper to provide a 102-dB SNR from 20 Hz to 20 kHz.

The PWM section accepts 32-bit PCM data from the DAP and outputs eight PWM audio output channels configurable as either:

- Six channels to drive power stages and two channels to drive a differential-input active filter to provide a separately controllable stereo lineout
- Eight channels to drive power stages

The TAS5518C PWM section output supports both single-ended and bridge-tied loads.

The PWM section provides a headphone PWM output to drive an external differential amplifier like the TPA112. The headphone circuit uses the PWM modulator for channels 1 and 2. The headphone does not operate while the six or eight back-end drive channels are operating. The headphone is enabled via a headphone-select terminal.

The PWM section has individual-channel dc-blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz.

The PWM section has individual-channel de-emphasis filters for 32, 44.1, and 48 kHz that can be enabled and disabled.

Not Recommended For New Designs

The PWM section also contains the power-supply volume control (PSVC) PWM.

The interpolator, noise shaper, and PWM sections provide a PWM output with the following features:

- Up to 8× oversampling
  - 8× at f_S = 44.1 kHz, 48 kHz, 32 kHz, 38 kHz
  - 4× at f_S = 88.2 kHz, 96 kHz
  - 2× at f_S = 176.4 kHz, 192 kHz
- Fifth-order noise shaping
- 110-dB dynamic range 0–20 kHz (TAS5518C + TAS5111 system measured at speaker terminals)
- THD < 0.01%
- Adjustable maximum modulation limit of 93.8% to 99.2%
- 3.3-V digital signal

2.12.1 DC Blocking (High-Pass Filter Enable/Disable)

Each input channel incorporates a first-order, digital, high-pass filter to block potential dc components. The filter –3-dB point is approximately 0.89-Hz at the 44.1-kHz sampling rate. The high-pass filter can be enabled and disabled via the I^2C system control register 1 (0x03 bit D7). The default setting is 1 (high-pass filter enabled).

2.12.2 De-Emphasis Filter

For audio sources that have been pre-emphasized, a precision 50-µs/15-µs de-emphasis filter is provided to support the sampling rates of 32 kHz, 44.1 kHz, and 48 kHz. Figure 2-19 shows a graph of the de-emphasis filtering characteristics. De-emphasis is set using two bits in the system control register.

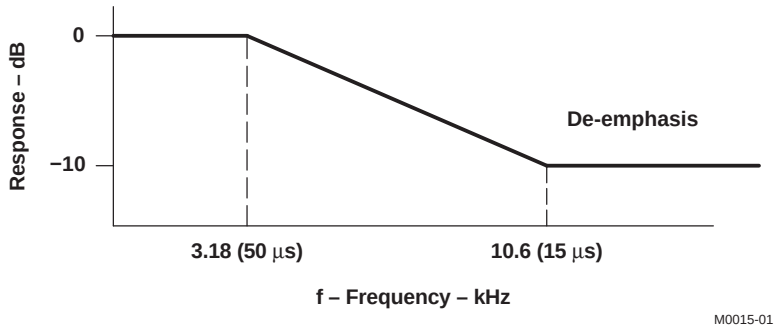

Figure 2-19. De-Emphasis Filter Characteristics

2.12.3 Power-Supply Volume Control (PSVC)

The TAS5518C supports volume control both by conventional digital gain/attenuation and by a combination of digital and analog gain/attenuation. Varying the H-bridge power-supply voltage performs the analog volume control function. The benefits of using power-supply volume control (PSVC) are reduced idle channel noise, improved signal resolution at low volumes, increased dynamic range, and reduced radio frequency emissions at reduced power levels. The PSVC is enabled via I^2C. When enabled, the PSVC provides a PWM output that is filtered to provide a reference voltage for the power supply. The power-supply adjustment range can be set for –-12.04, –18.06, or –24.08 dB, to accommodate a range of variable power-supply designs.

Figure 2-20 and Figure 2-21 show how power-supply and digital gains can be used together.

The volume biquad (0xCF) can be used to implement a low-pass filter in the digital volume control to match the PSVC volume transfer function. Note that if the PVSC function is not used, the volume biquad should be all-pass (default).

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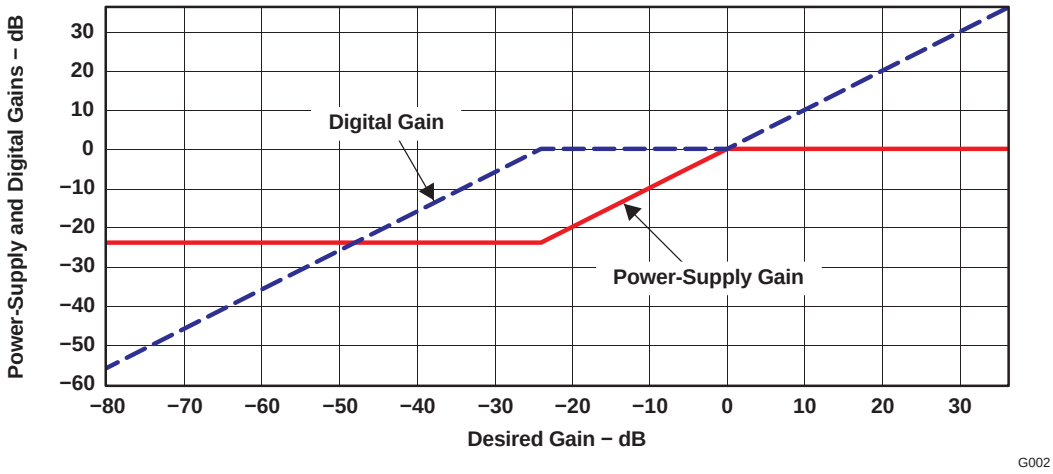

Figure 2-20. Power-Supply and Digital Gains (Linear Space)

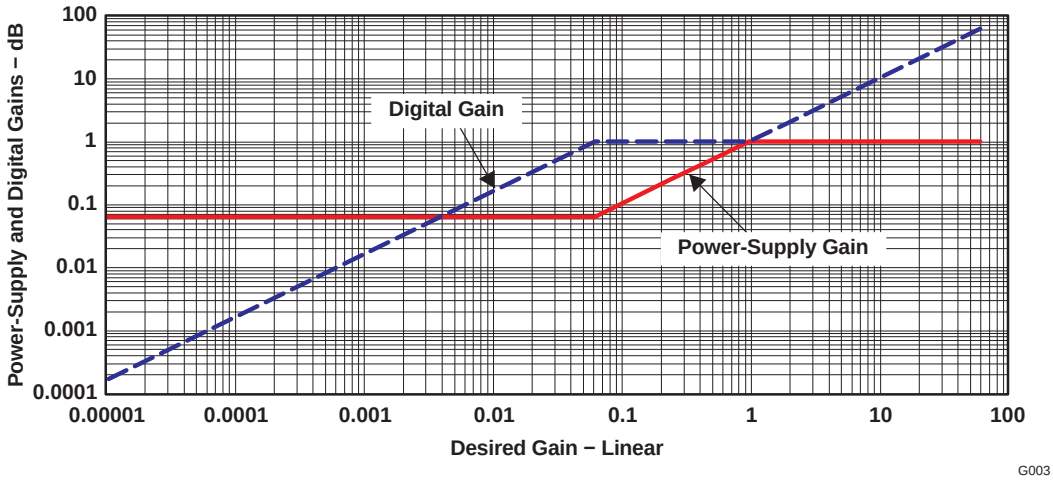

Figure 2-21. Power-Supply and Digital Gains (Log Space)

2.12.4 AM Interference Avoidance

Digital amplifiers can degrade AM reception as a result of their RF emissions. Texas Instruments' patented AM interference-avoidance circuit provides a flexible system solution for a wide variety of digital audio architectures. During AM reception, the TAS5518C adjusts the radiated emissions to provide an emission-clear zone for the tuned AM frequency. The inputs to the TAS5518C for this operation are the tuned AM frequency, the IF frequency, and the sample rate. The sample rate is automatically detected.

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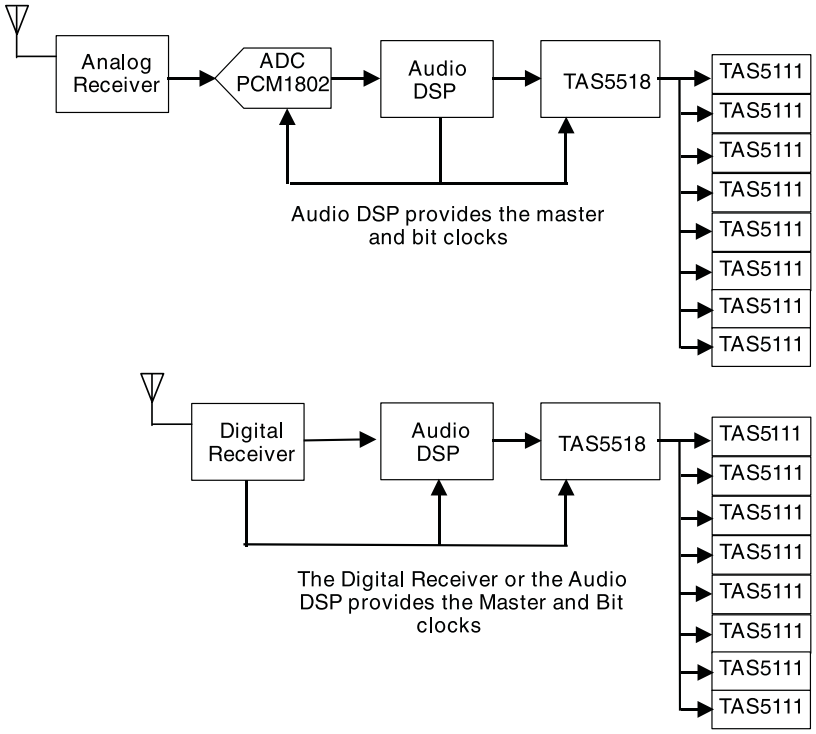

Figure 2-22. Block Diagrams of Typical Systems Requiring TAS5518C Automatic AM Interference-Avoidance Circuit

3 TAS5518C Controls and Status

The TAS5518C provides control and status information from both the I^2C registers and device pins.

This section describes some of these controls and status functions. The I^2C summary and detailed register descriptions are contained in Section 6 and Section 7.

3.1 I^2C Status Registers

The TAS5518C has two status registers that provide general device information. These are the general status register 0 (0x01) and the error status register (0x02).

3.1.1 General Status Register (0x01)

- Device identification code
- Clip indicator – The TAS5518C has a clipping indicator. Writing to the register clears the indicator.

3.1.2 Error Status Register (0x02)

- No internal errors (the valid signal is high)
- A clock error has occurred – These are sticky bits that are cleared by writing to the register.
  - LRCLK error – when the number of MCLKs per LRCLK is incorrect
  - SCLK error – when the number of SCLKS per LRCLK is incorrect
  - Frame slip – when the number of MCLKs per LRCLK changes by more than 10 MCLK cycles
  - PLL phase-lock error
- This error status register is normally used for system development only.

3.2 TAS5518C Pin Controls

The TAS5518C provide a number of terminal controls to manage the device operation. These controls are:

- $\overline{\text{RESET}}$
- $\overline{\text{PDN}}$
- $\overline{\text{BKND_ERR}}$
- $\overline{\text{HP_SEL}}$
- $\overline{\text{MUTE}}$

3.2.1 Reset ($\overline{\text{RESET}}$)

The TAS5518C is placed in the reset mode either by the power-up reset circuitry when power is applied, or by setting the $\overline{\text{RESET}}$ terminal low.

$\overline{\text{RESET}}$ is an asynchronous control signal that restores the TAS5518C to the hard-mute state (M-state). Master volume is immediately set to full attenuation (there is no ramp down). Reset initiates the device reset without an MCLK input. As long as the $\overline{\text{RESET}}$ terminal is held low, the device is in the reset state. During reset, all I^2C and serial data bus operations are ignored.

Table 3-1 shows the device output signals while $\overline{\text{RESET}}$ is active.

Table 3-1. Device Outputs During Reset

SIGNAL	SIGNAL STATE
Valid	Low
PWM P-outputs	Low (M-state)
PWM M-outputs	Low (M-state)
SDA	Signal input (not driven)

Because $\overline{\text{RESET}}$ is an asynchronous signal, clicks and pops produced during the application (the leading edge) of $\overline{\text{RESET}}$ cannot be avoided. However, the transition from the hard-mute state (M-state) to the operational state is performed using a quiet start-up sequence to minimize noise. This control uses the PWM reset and unmute sequence to shut down and start up the PWM. A detailed description of these sequences is contained in the PWM section. If a completely quiet reset or power-down sequence is desired, $\overline{\text{MUTE}}$ should be applied before applying $\overline{\text{RESET}}$.

The rising edge of the reset pulse begins device initialization before the transition to the operational mode. During device initialization, all controls are reset to their initial states. Table 3-2 shows the default control settings following a reset.

Table 3-2. Values Set During Reset

CONTROL	SETTING
Output mixer configuration	0xD0 bit 30 = 0 (remapped output mixer configuration)
High pass	Enabled
Unmute from clock error	Hard unmute
Input automute	Enabled
Output automute	Enabled
De-emphasis	Disabled
Serial data interface format	I^2S, 24-bit
Individual channel mute	No channels are muted
Automute delay	5 ms
Automute threshold 1	< 8 bits
Automute threshold 2	Same as automute threshold 1
Modulation limit	97.7% (Note: Some power stages require a lower modulation index)
Six- or eight-channel configuration	Eight channels
Volume and mute update rate	Volume ramp 88.2 ms
Treble and bass slew rate	Update every 1.31 ms
Bank switching	Manual bank selection is enabled
Biquad coefficients	Set to all pass
Input mixer coefficients	Input N → Channel N, no attenuation
Output mixer coefficients	Channel N → Output N, no attenuation
Subwoofer sum into Ch1 and Ch2	Gain of 0
Ch1 and Ch2 sum in subwoofer	Gain of 0
Bass and treble bypass/inline	Bypass
DRC bypass/inline	Bypass
DRC	Default values
Master volume	Mute
Individual channel volumes	0 dB
All bass and treble indexes	0x12 neutral
Treble filter sets	Filter set 3
Bass filter sets	Filter set 3
Loudness	Loudness disabled, default values
AM interference mode enable	Disabled
AM interference mode IF	455 kHz
AM interference mode select sequence	1
AM interference mode tuned frequency and input mode	0000, BCD

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After the initialization time, the TAS5518C starts the transition to the operational state with the master volume set at mute.

Because the TAS5518C has an external crystal time base, following the release of reset, the TAS5518C sets the MCLK and data rates and performs the initialization sequences. The PWM outputs are held at a mute state until the master volume is set to a value other than mute via I^2C.

3.2.2 Power Down ($\overline{PDN}$)

The TAS5518C can be placed into the power-down mode by holding the $\overline{PDN}$ terminal low. When the power-down mode is entered, both the PLL and the oscillator are shut down. Volume is immediately set to full attenuation (there is no ramp down). This control uses the PWM mute sequence that provides a low click and pop transition to the hard-mute state (M-state).

Power down is an asynchronous operation that does not require MCLK to go into the power-down state. To initiate the power-up sequence requires MCLK to be operational and the TAS5518C to receive five MCLKs prior to the release of $\overline{PDN}$.

As long as the $\overline{PDN}$ terminal is held low, the device is in the power-down state with the PWM outputs in a hard-mute state (M-state). During power down, all I^2C and serial data bus operations are ignored. Table 3-3 shows the device output signals while $\overline{PDN}$ is active.

Table 3-3. Device Outputs During Power Down

SIGNAL	SIGNAL STATE
VALID	Low
PWM P-outputs	M-state = low
PWM M-outputs	M-state = low
SDA	Signal input
PSVC	M-state = low

Following the application of $\overline{PDN}$, the TAS5518C does not perform a quiet shutdown to prevent clicks and pops produced during the application (the leading edge) of this command. The application of $\overline{PDN}$ immediately performs a PWM stop. A quiet stop sequence can be performed by first applying $\overline{MUTE}$ before $\overline{PDN}$.

When $\overline{PDN}$ is released, the system goes to the end state specified by the $\overline{MUTE}$ and $\overline{BKND_ERR}$ pins and the I^2C register settings.

The crystal time base allows the TAS5518C to determine the CLK rates. Once these rates are determined, the TAS5518C unmutes the audio.

3.2.3 Back-End Error ($\overline{BKND_ERR}$)

Back-end error is used to provide error management for back-end error conditions. Back-end error is a level-sensitive signal. Back-end error can be initiated by bringing the $\overline{BKND_ERR}$ terminal low for a minimum of five MCLK cycles. When $\overline{BKND_ERR}$ is brought low, the PWM sets either six or eight channels into the PWM back-end error state. This state is described in Section 2.12. Once the back-end error sequence is initiated, a delay of 5 ms is performed before the system starts the output re-initialization sequence. After the initialization time, the TAS5518C begins normal operation. Back-end error does not affect other PWM modulator operations.

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Table 3-4. Device Outputs During Back-End Error

SIGNAL	SIGNAL STATE
Valid	Low
PWM P-outputs	M-state = low
PWM M-outputs	M-state = low
PWM_HP P-outputs	M-state = low
PWM_HP M-outputs	M-state = low
SDA	Signal input (not driven)

3.2.3.1 $\overline{\text{BKND_ERR}}$ and VALID

The number of channels that are affected by the $\overline{\text{BKND_ERR}}$ signal depends on the setting of bit D1 of I^2C register 0xE0. If the I^2C setting is 0 (8-channel mode), the TAS5518C places all eight PWM outputs in the PWM back-end error state. If the I^2C setting is 1, the TAS5518C is in 6-channel mode. For proper operation in 6-channel mode, the lineout configuration registers (0x09 and 0x0A) must be 0x00 instead of the default of 0xE0. In this case, VALID is pulled LOW, and the TAS5518C brings PWM outputs 1, 2, 3, 4, 7, and 8 to a back-end error state, while not affecting lineout channels 5 and 6. Table 3-4 shows the device output signal states during back-end error.

3.2.4 *Speaker/Headphone Selector ($\overline{\text{HP_SEL}}$)*

The $\overline{\text{HP_SEL}}$ terminal enables the headphone output or the speaker outputs. The headphone output receives the processed data output from DAP and PWM channels 1 and 2.

In 6-channel configuration, this feature does not affect the two lineout channels.

When low, the headphone output is enabled. In this mode, the speaker outputs are disabled. When high, the speaker outputs are enabled and the headphone is disabled.

Changes in the pin logic level result in a state change sequence using soft mute to the hard-mute state (M-state) for both speaker and headphone followed by a soft unmute.

When $\overline{\text{HP_SEL}}$ is low, the configuration of channels 1 and 2 is defined by the headphone configuration register. When $\overline{\text{HP_SEL}}$ is high, the channel-1 and -2 configuration registers define the configuration of channels 1 and 2.

If using the remapped-output mixer configuration (0xD0 bit 30 = 0) in the 6-channel mode, the headphone operation is modified. That is, following the assertion or de-assertion of headphone, mute must be asserted and de-asserted using the $\overline{\text{MUTE}}$ pin.

3.2.5 *Mute ($\overline{\text{MUTE}}$)*

The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume. The TAS5518C has both master and individual channel mute commands. A terminal is also provided for the master mute. The active-low master mute I^2C register and the $\overline{\text{MUTE}}$ terminal are logically ORed together. If either is set to low, a mute on all channels is performed. The master mute command operates on all channels regardless of whether the system is in the 6- or 8-channel configuration.

When mute is invoked, the PWM output stops switching and then goes to an idle state.

The master mute terminal is used to support a variety of other operations in the TAS5518C, such as setting the the biquad coefficients, the serial interface format, and the clock rates. A mute command by the master mute terminal, individual I^2C mute, the AM interference mute sequence, the bank-switch mute sequence, or automute overrides an unmute command or a volume command. While a mute is active, the commanded channels are placed in a mute state. When a channel is unmuted, it goes to the last commanded volume setting that has been received for that channel.

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3.3 Device Configuration Controls

The TAS5518C provides a number of system configuration controls that are set at initialization and following a reset.

- Channel configuration
- Headphone configuration
- Audio system configurations
- Recovery from clock error
- Power-supply volume-control enable
- Volume and mute update rate
- Modulation index limit
- Master-clock and data-rate controls
- Bank controls

3.3.1 Channel Configuration Registers

For the TAS5518C to have full control of the power stages, registers 0x05 to 0x0C must be programmed to reflect the proper power stage and how each one should be controlled. There are eight channel configuration registers, one for each channel. For information on using $\overline{\text{BKND_ERR}}$ and VALID, see Section 3.2.3.1

The primary reason for using these registers is that different power stages require different handling during start-up, mute/unmute, shutdown, and error recovery. The TAS5518C must select the sequence that gives the best click and pop performance and ensures that the bootstrap capacitor is charged correctly during start-up. This sequence depends on which power stage is present at the TAS5518C output.

Table 3-5. Description of the Channel Configuration Registers (0x05 to 0x0C)

BIT	DESCRIPTION
D7	Enable/disable error recovery sequence. In case the $\overline{\text{BKND_ERR}}$ pin is pulled low, this register determines if this channel is to follow the error recovery sequence or to continue with no interruption.
D6	Determines if the power stage needs the TAS5518C VALID pin to go low to reset the power stage. Some power stages can be reset by a combination of PWM signals. For these devices, it is recommended to set this bit low, because the VALID pin is shared for power stages. This provides better control of each power stage.
D5	Determines if the power stage needs the TAS5518C VALID pin to go low to mute the power stage. Some power stages can be muted by a combination of PWM signals. For these devices, it is recommended to set this bit low, because the VALID pin is shared for power stages. This provides better control of each power stage.
D4	Inverts the PWM output. Inverting the PWM output can be an advantage if the power stage input pin is opposite the TAS5518C PWM pinout. This makes routing on the PCB easier. To keep the phase of the output, the speaker terminals must also be inverted.
D3	When using the TAS5182 power stage this bit must be set.
D2	Can be used to handle click and pop for some applications.
D1	This bit is normally used together with D2. For some power stages, both PWM signals must be high to get the desired operation of both speaker outputs to be low. This bit sets the PWM outputs high-high during mute.
D0	Not used

Table 3-6 lists the optimal setting for each output-stage configuration. Note that the default value is applicable in all configurations except the TAS5182 SE/BTL configuration.

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Table 3-6. Recommended TAS5518C Configurations for Texas Instruments Power Stages

DEVICE	ERROR RECOVERY	CONFIGURATION	D7	D6	D5	D4	D3	D2	D1	D0
TAS5111 (default)	**RES**	**BTL**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
		SE	1	1	1	0	0	0	0	0
	AUT	BTL	0	1	1	0	0	0	0	0
		SE	0	1	1	0	0	0	0	0
TAS5112	RES	BTL	1	1	0	0	0	0	0	0
		SE	1	1	0	0	0	0	0	0
	AUT	BTL	0	1	0	0	0	0	0	0
		SE	0	1	0	0	0	0	0	0
TAS5182	RES	BTL	1	1	1	0	1	0	0	0
		SE	1	1	1	0	1	0	0	0

RES: To recover from a shutdown, the output stage requires $\overline{\text{VALID}}$ to go low.

AUT: The power stage can auto-recover from a shutdown.

BTL: Bridge-tied load configuration

SE: Single-ended configuration

3.3.2 Headphone Configuration Registers

The headphone configuration controls are identical to the speaker configuration controls. The headphone configuration control settings are used in place of the speaker configuration control settings for channels 1 and 2 when the headphones are selected. However, only one configuration setting for headphones is used, and that is the default setting.

3.3.3 Audio System Configurations

The TAS5518C can be configured to comply with various audio systems: 5.1-channel system, 6-channel system, 7.1-channel system, and 8-channel system.

The audio system configuration is set in the general control register (0xE0). Bits D31–D4 must be zero and D0 is *don't care*.

D3 Must always be 0 (default). Note that subwoofer cannot be used as lineout when PSVC is enabled. (D3 is a write-only bit)

D2 Enables/disables power-supply volume control

D1 Sets number of speakers in the system, including possible line outputs

D3–D1 must be configured for the audio system in the application, as shown in Table 3-7.

Table 3-7. Audio System Configuration (General Control Register 0xE0)

Audio System	D31–D4	D3	D2	D1	D0
6 channels or 5.1 not using PSVC	0	0	0	1	X
6 channels using PSVC	0	0	1	1	X
5.1 system using PSVC	0	0	1	1	X
8 channels or 7.1 not using PSVC (default)	**0**	**0**	**0**	**0**	**X**
8 channels using PSVC	0	0	1	0	X
7.1 system using PSVC	0	0	1	0	X

3.3.3.1 Using Line Outputs in 6-Channel Configurations

The audio system can be configured for a 6-channel configuration (with 2 lineouts) by writing a 1 to bit D1 of register 0xE0 (general control register). In this configuration, channel-5 and -6 processing are exactly the same as the other channels, except that the master volume and the loudness function have no effect on the signal.

Note that in 6-channel configuration, channels 5 and 6 are unaffected by back-end error ($\overline{\text{BKND_ERR}}$ goes low).

To use channels 5 and 6 as unprocessed lineouts, the following setup is recommended:

- Channel-5 volume and channel-6 volume should be set for a constant output, such as 0 dB.
- Bass and treble for channels 5 and 6 can be used if desired.
- DRC1 should be bypassed for channels 5 and 6.
- If a down mix is desired on channels 5 and 6 as lineout, the down mixing can be performed using the channel-5 and channel-6 input mixers.
- The operation of the channel-5 and -6 biquads is unaffected by the 6-/8-channel configuration setting.

3.3.4 Recovery from Clock Error

The TAS5518C can be set either to perform a volume ramp up during the recovery sequence of a clock error or simply to come up in the last state (or desired state if a volume or tone update was in progress). This feature is enabled via I^2C system control register 0x03.

3.3.5 Power-Supply Volume-Control Enable

The power-supply volume control (PSVC) can be enabled and disabled via I^2C register 0xE0. The subwoofer PWM output is always controlled by the PSVC. When using PSVC the subwoofer cannot be used as lineout.

3.3.6 Volume and Mute Update Rate

The TAS5518C has fixed soft volume and mute ramp durations. The ramps are linear. The soft volume and mute ramp rates are adjustable by programming the I^2C register 0xD0 for the appropriate number of steps to be 512, 1024, or 2048. The update is performed at a fixed rate regardless of the sample rate.

- In normal speed, the update rate is 1 step every $4/f_S$ seconds.
- In double speed, the update is 1 step every $8/f_S$ seconds.
- In quad speed, the update is 1 step every $16/f_S$ seconds.

Because of processor loading, the update rate can increase for some increments by one step every $1/f_S$ to $3/f_S$. However, the variance of the total time to go from 18 dB to mute is less than 25%.

Table 3-8. Volume Ramp Periods in ms

NUMBER OF STEPS	SAMPLE RATE (kHz)	
	44.1, 88.2, 176.4	32, 48, 96, 192
512	46.44	42.67
1024	92.88	85.33
2048	185.76	170.67

3.3.7 Modulation Index Limit

PWM modulation is a linear function of the audio signal. When the audio signal is 0, the PWM modulation is 50%. When the audio signal increases toward full scale, the PWM modulation increases toward 100%. For negative signals, the PWM modulations fall below 50% toward 0%.

However, the maximum possible modulation does have a limit. During the offtime period, the power stage

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connected to the TAS5518C output needs to get ready for the next on-time period. The maximum possible modulation is then set by the power stage requirements. The default modulation index limit setting is 97.7%; however, some power stages may require a lower modulation limit. See the applicable power stage data sheet for details on setting the modulation index limit. The default setting of 97.7% can be changed in the modulation index register (0x16).

3.4 Master Clock and Serial Data Rate Controls

The TAS5518C functions only as a receiver of the MCLK (master clock), SCLK (shift clock), and LRCLK (left/right clock) signals that control the flow of data on the four serial data interfaces. The 13.5-MHz external crystal allows the TAS5518C to detect MCLK and the data rate automatically.

The MCLK frequency can be 64 f_S, 128 f_S, 196 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S.

The TAS5518C operates with the serial data interface signals LRCLK and SCLK synchronized to MCLK. However, the phase relationship of these signals has no constraint. The TAS5518C accepts a 64 f_S SCLK rate and a 1 f_S LRCLK.

If the phase of SCLK or LRCLK drifts more than ±10 MCLK cycles since the last reset, the TAS5518C senses a clock error and resynchronizes the clock timing.

The clock and serial data interface have several control parameters:

- MCLK ratio (64 f_S, 128 f_S, 196 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S) – I^2C parameter
- Data rate (32, 38, 44.1, 48, 88.2, 96, 176.4, 192 kHz) – I^2C parameter
- AM mode enable/disable – I^2C parameter

During AM interference avoidance, the clock control circuitry uses three other configuration inputs:

- Tuned AM frequency (for AM interference avoidance) (550 kHz to 1750 kHz) – I^2C parameter
- Frequency set select (1–4) – I^2C parameter
- Sample rate – I^2C parameter or auto-detected

3.4.1 PLL Operation

The TAS5518C uses two internal clocks generated by two internal phase-locked loops (PLLs), the digital PLL (DPLL) and the analog PLL (APLL). The APLL provides the reference clock for the PWM. The DPLL provides the reference clock for the digital audio processor and the control logic.

The master clock MCLK input provides the input reference clock for the APLL. The external 13.5-MHz crystal provides the input reference clock for the DPLL. The crystal provides a time base to support a number of operations, including the detection of the MCLK ratio, the data rate, and clock error conditions. The crystal time base provides a constant rate for all controls and signal timing.

Even if MCLK is not present, the TAS5518C can receive and store I^2C commands and provide status.

3.5 Bank Controls

The TAS5518C permits the user to specify and assign sample-rate-dependent parameters for biquad, loudness, DRC, and tone in one of three banks that can be manually selected or selected automatically based on the data sampling rate. Each bank can be enabled for one or more specific sample rates via I^2C bank control register 0x40. Each bank set holds the following values:

- Coefficients for seven biquads ($7 \times 5 = 35$ coefficients) for each of the eight channels (registers 0x51–0x88)
- Coefficients for one loudness biquad (register 0x95)
- DRC1 energy and (1 – energy) values (register 0x98)
- DRC1 attack, (1 – attack), decay, (1 – decay) values (register 0x9C)
- DRC2 energy and (1 – energy) values (register 0x9D)
- DRC2 attack, (1 – attack), decay, (1 – decay) values (register 0xA1)

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- Five bass filter-set selections (register 0xDA)
- Five treble filter-set selections (register 0xDC)

The default selection for bank control is manual bank with bank 1 selected. Note that if bank switching is used, bank 2 and bank 3 must be programmed on power up, because the default values are all zeroes. If bank switching is used and bank 2 and bank 3 are not programmed correctly, then the output of the TAS5518C could be muted when switching to those banks.

3.5.1 Manual Bank Selection

The three bank-selection bits of the bank control register allow the appropriate bank to be manually selected (000 = bank 1, 001 = bank 2, 010 = bank 3). In the manual mode, when a write occurs to the biquad, DRC, or loudness coefficients, the currently selected bank is updated. If audio data is streaming to the TAS5518C during a manual bank selection, the TAS5518C first performs a mute sequence, then performs the bank switch, and finally restores the volume using an unmute sequence.

A mute command initiated by the bank-switch mute sequence overrides an unmute command or a volume command. While a mute is active, the commanded channels are muted. When a channel is unmuted, the volume level goes to the last commanded volume setting that has been received for that channel.

If MCLK or SCLK is stopped, the TAS5518C performs a bank-switch operation. If the clocks start up once the manual bank-switch command has been received, the bank-switch operation is performed during the 5-ms, silent-start sequence.

3.5.2 Automatic Bank Selection

To enable automatic bank selection, a value of 3 is written into the bank-selection bits of the bank control register. Banks are associated with one or more sample rates by writing values into the bank 1 or bank 2 data-rate selection registers. The automatic bank selection is performed when a frequency change is detected according to the following scheme:

1. The system scans bank-1 data-rate associations to see if bank 1 is assigned for that data rate.
2. If bank 1 is assigned, then the bank-1 coefficients are loaded.
3. If bank 1 is not assigned, the system scans bank 2 to see if bank 2 is assigned for that data rate.
4. If bank 2 is assigned, the bank-2 coefficients are loaded.
5. If bank 2 is not assigned, the system loads the bank-3 coefficients.

The default is that all frequencies are enabled for bank 1. This default is expressed as a value of all 1s in the bank-1 auto-selection byte and all 0s in the bank-2 auto-selection byte.

3.5.2.1 Coefficient Write Operations While Automatic Bank Switch Is Enabled

In automatic mode, if a write occurs to the tone, EQ, DRC, or loudness coefficients, the bank that is written to is the current bank.

3.5.3 Bank Set

Bank set is used to provide a secure way to update the bank coefficients in both the manual and automatic switching modes without causing a bank switch to occur. Bank-set mode does not alter the current bank register mapping. It simply enables any bank coefficients to be updated while inhibiting any bank switches from taking place. In manual mode, this enables the coefficients to be set without switching banks. In automatic mode, this prevents a clock error or data-rate change from corrupting a bank coefficient write.

To update the coefficients of a bank, a value of 4, 5, or 6 is written into in the bank-selection bits of the bank control register. This enables the tone, EQ, DRC, and loudness coefficient values of bank 1, 2, or 3, respectively, to be updated.

Once the coefficients of the bank have been updated, the bank-selection bits are then returned to the desired manual or automatic bank-selection mode.

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3.5.4 Bank-Switch Timeline

After a bank switch is initiated (manual or automatic), no I^2C writes to the TAS5518C should occur before a minimum of 186 ms. This value is determined by the volume ramp rates for a particular sample rate.

3.5.5 Bank-Switching Example 1

Problem: The audio unit containing a TAS5518C needs to handle different audio formats with different sample rates. Format #1 requires f_S = 32 kHz, format #2 requires f_S = 44.1 kHz, and format #3 requires f_S = 48 kHz. The sample-rate-dependent parameters in the TAS5518C require different coefficients and data depending on the sample rate.

Strategy: Use the TAS5518C bank-switching feature to allow for managing and switching three banks associated with the three sample rates, 32 kHz (bank 1), 44.1 kHz (bank 2), and 48 kHz (bank 3).

One possible algorithm is to generate, load, and automatically manage bank switching for this problem:

1. Generate bank-related coefficients for sample rates of 32 kHz, 44.1 kHz, and 48 kHz, and include the same in the microprocessor-based TAS5518C I^2C firmware.
2. On TAS5518C power up or reset, the microprocessor runs the following TAS5518C initialization code:
   a. Update bank 1 (write 0x0004 8040 to register 0x40).
   b. Write bank-related I^2C registers with appropriate values for bank 1.
   c. Write bank 2 (write 0x0005 8040 to register 0x40).
   d. Load bank-related I^2C registers with appropriate values for bank 2.
   e. Write bank 3 (write 0x0006 8040 to register 0x40).
   f. Load bank-related I^2C registers with appropriate values for bank 3.
   g. Select automatic bank switching (write 0x0003 8040 to register 0x40).
3. When the audio media changes, the TAS5518C automatically detects the incoming sample rate and automatically switches to the appropriate bank.

In this example, any sample rates other than 32 kHz and 44.1 kHz use bank 3. If other sample rates are used, then the banks must be set up differently.

3.5.6 Bank-Switching Example 2

Problem: The audio system uses all of the sample rates supported by the TAS5518C. How can the automatic bank switching be set up to handle this situation?

Strategy: Use the TAS5518C bank-switching feature to allow for managing and switching three banks associated with sample rates as follows:

- Bank 1: Coefficients for 32 kHz, 38 kHz, 44.1 kHz, and 48 kHz
- Bank 2: Coefficients for 88.2 kHz and 96 kHz
- Bank 3: Coefficients for 176.4 kHz and 192 kHz

One possible algorithm is to generate, load, and automatically manage bank switching for this problem:

1. Generate bank-related coefficients for sample rates 48 kHz (bank 1), 96 kHz (bank 2), and 192 kHz (bank 3) and include the same in the microprocessor-based TAS5518C I^2C firmware.
2. On TAS5518C power up or reset, the microprocessor runs the following TAS5518C initialization code:
   a. Update bank 1 (write 0x0004 F00C to register 0x40).
   b. Write bank-related I^2C registers with appropriate values for bank 1.
   c. Write bank 2 (write 0x0005 F00C to register 0x40).
   d. Load bank-related I^2C registers with appropriate values for bank 2.
   e. Write bank 3 (write 0x0006 F00C to register 0x40).
   f. Load bank-related I^2C registers with appropriate values for bank 3.
   g. Select automatic bank switching (write 0x0003 F00C to register 0x40).
3. When the audio media changes, the TAS5518C automatically detects the incoming sample rate and automatically switches to the appropriate bank.

Not Recommended For New Designs

4 Electrical Specifications

4.1 Absolute Maximum Ratings(1)

	Supply voltage, DVDD and DVD_PWM		–0.3 V to 3.6 V
	Supply voltage, AVDD_PLL		–0.3 V to 3.6 V
	Input voltage	3.3-V digital input	–0.5 V to DVDD + 0.5 V
		5-V tolerant(2) digital input	–0.5 V to 6 V
		1.8-V LVCMOS(3)	–0.5 V to VREF(4) + 0.5 V
I_{IK}	Input clamp current (V_I < 0 or V_I > 1.8 V		±20 µA
I_{OK}	Output clamp current (V_O < 0 or V_O > 1.8 V)		±20 µA
T_A	Operating free-air temperature		0°C to 70°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are RESET, PDN, MUTE, HP_SEL, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDIN3, SDIN4, SDA, and SCL.
(3) VRA_PLL, VRD_PLL, VR_DPLL, VR_DIG, VR_PWM
(4) VREF is a 1.8-V supply derived from regulators internal to the TAS5518C chip. VREF is on terminals VRA_PLL, VRD_PLL, VR_DPLL, VR_DIG, and VR_PWM. These terminals are provided to permit use of external filter capacitors, but should not be used to source power to external devices.

4.1.1 Dissipation Rating Table (High-k Board, 105°C Junction)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PAG	1869 mW	23.36 mW/°C	818 mW

4.2 Dynamic Performance

at recommended operating conditions at 25°C

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Dynamic range	TAS5518C + TAS5182 A-weighted (f_S = 48 kHz)		110		dB
Total harmonic distortion	TAS5182 at 1 W		0.1%		
	TAS5518C output		0.01%		
Frequency response	32-kHz to 96-kHz sample rates		±0.1		dB
	176.4, 192-kHz sample rates		±0.2		

Not Recommended For New Designs

4.3 Recommended Operating Conditions

over 0°C to 70°C

			MIN	NOM	MAX	UNIT
	Digital supply voltage, DVDD and DVDD_PWM		3	3.3	3.6	V
	Analog supply voltage, AVDD_PLL		3	3.3	3.6	V
V_{IH}	High-level input voltage	3.3 V	2			V
		5-V tolerant(1)	2			
		1.8-V LVCMOS (XTL_IN)	1.26			
V_{IL}	Low-level input voltage	3.3 V			0.8	V
		5-V tolerant(1)			0.8	
		1.8-V (XTL_IN)			0.54	
T_A	Operating ambient-air temperature range		–20	25	70	°C
T_J	Operating junction temperature range		–20		105	°C

(1) 5-V tolerant inputs are SDA, SCL, $\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, $\overline{\text{HP_SEL}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDIN3, and SDIN4

4.4 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL and 5-V(1) tolerant	I_{OH} = –4 mA	2.4			V
		1.8-V LVCMOS (XTL_OUT)	I_{OH} = –0.55 mA	1.44			
V_{OL}	Low-level output voltage	3.3-V TTL and 5-V(1) tolerant	I_{OL} = 4 mA			0.5	V
		1.8-V LVCMOS (XTL_OUT)	I_{OL} = 0.75 mA			0.5	
I_{OZ}	High-impedance output current	3.3-V TTL				±20	µA
I_{IL}	Low-level input current	3.3-V TTL	$V_I = V_{IL}$			±1	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IL}$			±1	
		5-V tolerant(2)	V_I = 0 V, DVDD = 3 V			±1	
I_{IH}	High-level input current	3.3-V TTL	$V_I = V_{IH}$			±1	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IH}$			±1	
		5-V tolerant(2)	V_I = 5.5 V, DVDD = 3 V			±1	
I_{DD}	Input supply current	Digital supply voltage, DVDD	f_S = 48 kHz		140		mA
			f_S = 96 kHz		150		
			f_S = 192 kHz		155		
			Power down		8		
		Analog supply voltage, AVDD	Normal		6		
			Power down		1		

(1) 5-V tolerant outputs are SCL and SDA.
(2) 5-V tolerant inputs are $\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, $\overline{\text{HP_SEL}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDIN3, SDIN4, SDA, and SCL.

4.5 PWM Operation

at recommended operating conditions over 0°C to 70°C

PARAMETER	TEST CONDITIONS	MODE	VALUE	UNIT
Output sample rate 1×–8× oversampled	32-kHz data rate ±4%	12× sample rate	384	kHz
	44.1-, 88.2-, 176.4-kHz data rate ±4%	8×, 4×, or 2× sample rate	352.8	kHz
	48-, 96-, 192-kHz data rate ±4%	8×, 4×, or 2× sample rate	384	kHz

4.6 Switching Characteristics

4.6.1 Clock Signals

PLL input parameters and external filter components over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{XTALI}	Frequency, XTAL IN	Only use 13.5-MHz crystal ≤1000 ppm		13.5		MHz
f_{MCLKI}	Frequency, MCLK ($1/t_{cyc2}$)		2		50	MHz
	MCLK duty cycle		40%	50%	60%	
	MCLK minimum high time	≥2-V MCLK = 49.152 MHz, within the min and max duty cycle constraints	5			ns
	MCLK minimum low time	≤0.8-V MCLK = 49.152 MHz, within the min and max duty cycle constraints	5			ns
	LRCLK allowable drift before LRCLK reset				10	MCLKs
	External PLL filter capacitors C11 and C12	SMD 0603 Y5V		100		nF
	External PLL filter capacitors C10 and C13	SMD 0603 Y5V		10		nF
	External PLL filter resistors R10 and R11	SMD 0603, metal film		200		Ω
	External VRA_PLL decoupling C14	SMD, Y5V		100		nF

(1) See the *TAS5518C Example Application Schematic*, Section 8.

4.6.2 Serial Audio Port

Serial audio port slave mode over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	SCLK input frequency	C_L = 30 pF	2.048		12.288	MHz
t_{su1}	Setup time, LRCLK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCLK rising edges		64		64	SCLK edges
	LRCLK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period

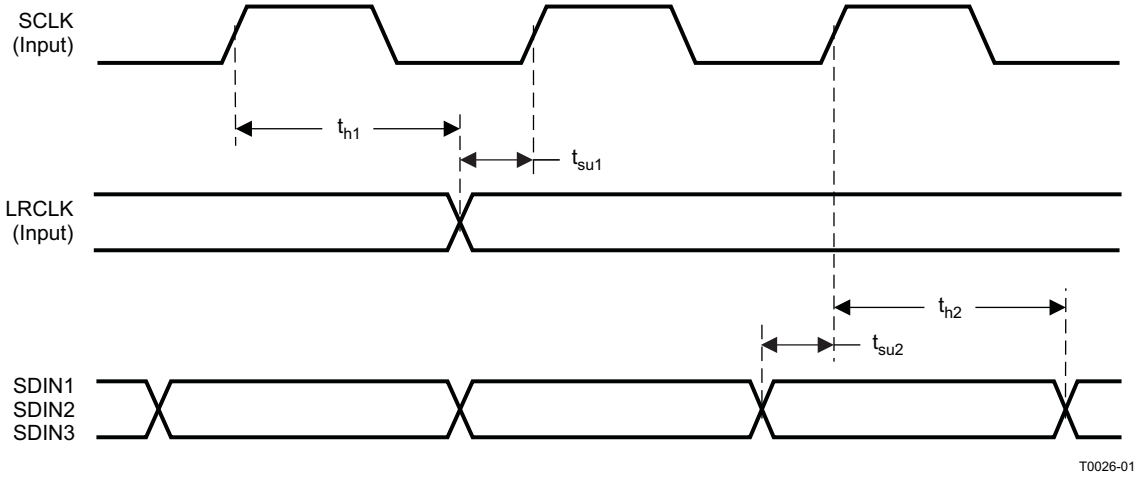


Figure 4-1. Slave Mode Serial Data Interface Timing

Not Recommended For New Designs

4.6.3 I^2C Serial Control Port Operation

Timing Characteristics for I^2C Interface Signals over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4		0.6		µs
t_{LOW}	LOW period of the SCL clock		4.7		1.3		µs
t_{HIGH}	HIGH period of the SCL clock		4		0.6		µs
t_{SU-STA}	Setup time for repeated START		4.7		0.6		µs
t_{SU-DAT}	Data setup time		250		100		µs
t_{HD-DAT}	Data hold time (1)(2)		0	3.45	0	0.9	µs
t_r	Rise time of both SDA and SCL			1000	20 + 0.1 C_b (3)	500 (4)	ns
t_f	Fall time of both SDA and SCL			300	20 + 0.1 C_b (3)	300	ns
t_{SU-STO}	Setup time for STOP condition		4		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		µs
C_b	Capacitive loads for each bus line			400		400	pF
VnL	Noise margin at the LOW level for each connected device (including hysteresis)		$0.1 \times V_{DD}$		$0.1 \times V_{DD}$		V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)		$0.2 \times V_{DD}$		$0.2 \times V_{DD}$		V

(1) Note that SDA does not have the standard I^2C specification 300-ns hold time and that SDA must be valid by the rising and falling edges of SCL. TI recommends that a 3.3-kW pullup resistor be used to avoid potential timing issues.
(2) A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU-DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r-max} + t_{SU-DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I^2C bus specification) before the SCL line is released.
(3) C_b = total capacitance of one bus line in pF.
(4) Rise time varies with pullup resistor.

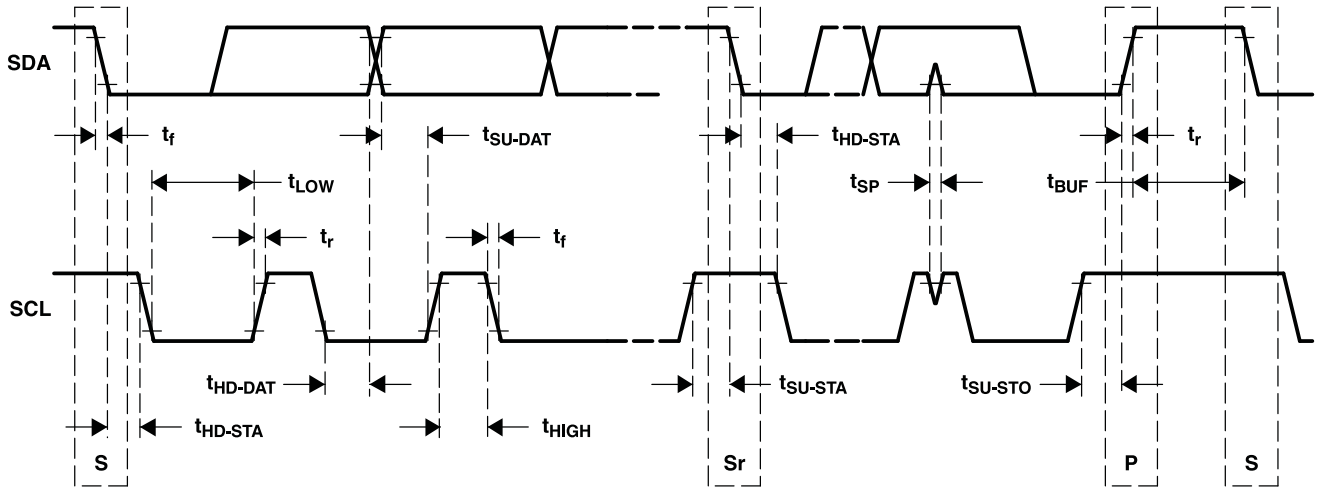


Figure 4-2. SCL and SDA Timing

Not Recommended For New Designs

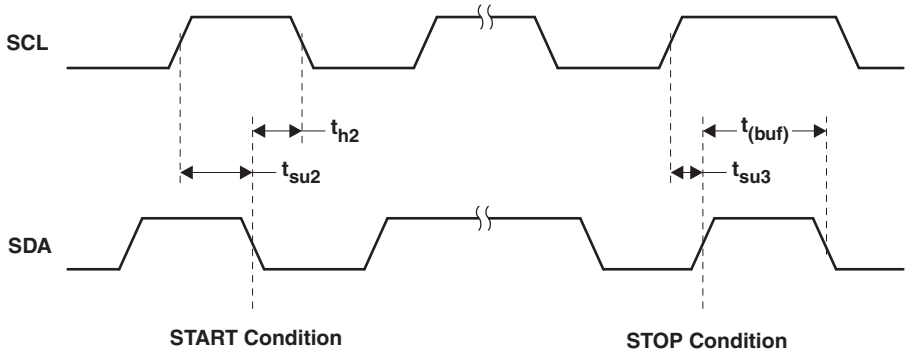


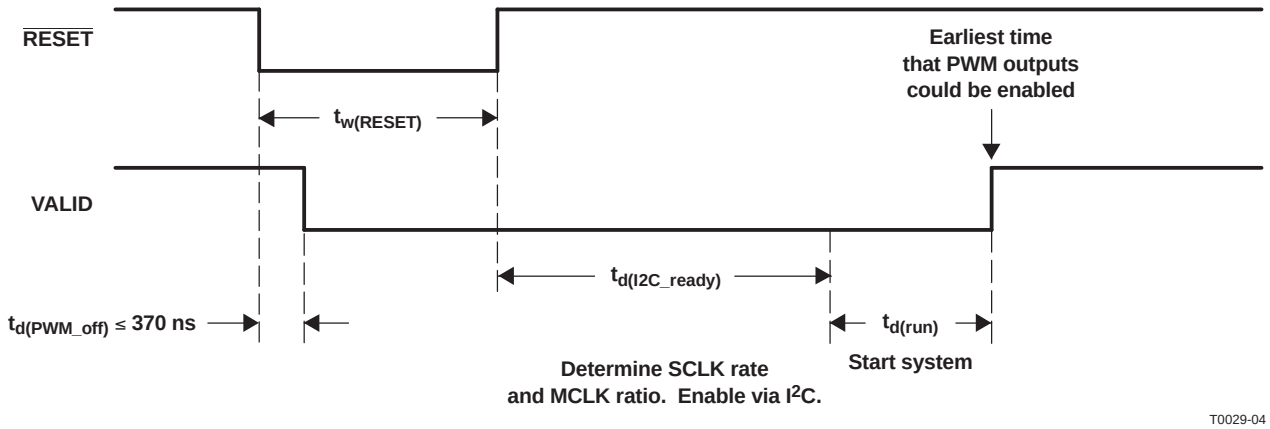
Figure 4-3. START and STOP Conditions Timing

Not Recommended For New Designs

4.6.4 Reset Timing ($\overline{RESET}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{r(DMSTATE)}$	Time to $\overline{M\text{-}STATE}$ low			370	ns
$t_{w(RESET)}$	Pulse duration, $\overline{RESET}$ active	400		None	ns
$t_{r(I2C_ready)}$	Time to enable I^2C		3		ms
$t_{r(run)}$	Device startup time	10			ms



NOTE: Since a crystal time base is used, the system determines the CLK rates. Once the data rate and master clock ratio is determined, the system outputs audio if a master volume command is issued.

Figure 4-4. Reset Timing

4.6.5 Power-Down ($\overline{PDN}$) Timing

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{p(DMSTATE)}$	Time to $\overline{M\text{-}STATE}$ low			300	µs
	Number of MCLKs preceding the release of $\overline{PDN}$	5			
t_{su}	Device startup time		120		ms

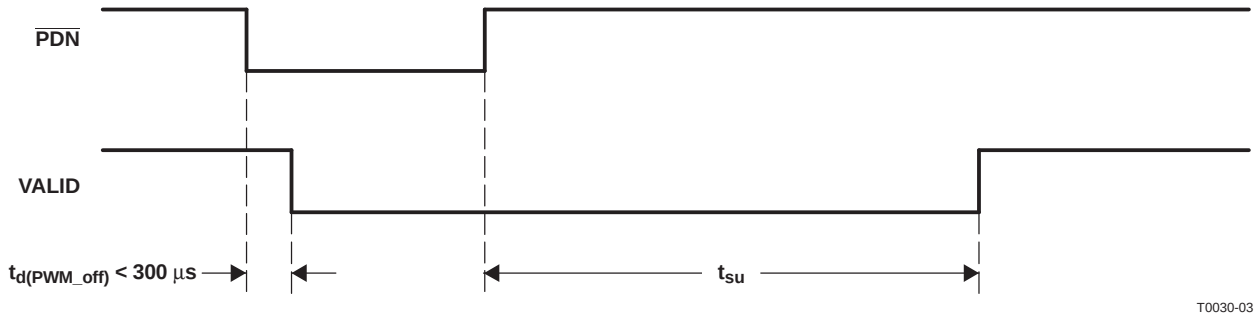


Figure 4-5. Power-Down Timing

Not Recommended For New Designs

4.6.6 Back-End Error ($\overline{BKND_ERR}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(ER)}$	Pulse duration, $\overline{BKND_ERR}$ active	350		None	ns
$t_{p(valid_low)}$				<100	µs
$t_{p(valid_high)}$	I^2C programmable to be between 1 to 10 ms	–25		25	% of interval

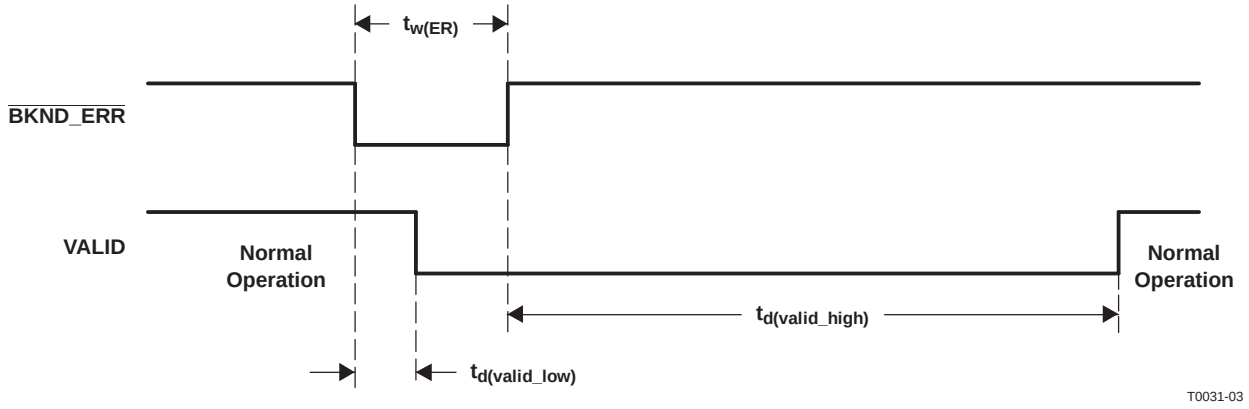


Figure 4-6. Error-Recovery Timing

4.6.7 Mute Timing ($\overline{MUTE}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VOL)}$	Volume ramp time		Defined by rate setting (1)		ms

(1) See the *Volume, Treble, and Base Slew Rates Register (0xD0)* section, Section 7.27.

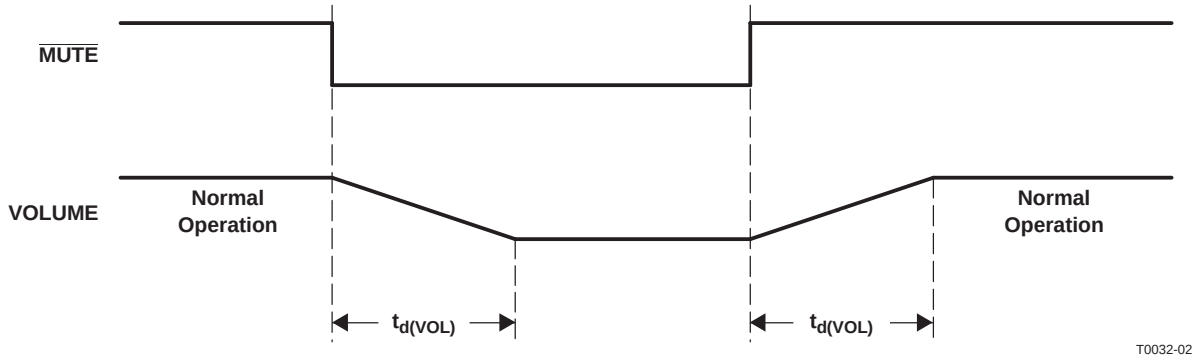


Figure 4-7. Mute Timing

Not Recommended For New Designs

4.6.8 Headphone Select ($\overline{HP_SEL}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(\overline{HP_SEL})}$	Pulse duration, $\overline{HP_SEL}$ active	350	None	ns
$t_{d(VOL)}$	Soft volume update time	Defined by rate setting (1)		ms
$t_{(SW)}$	Switchover time	0.2	1	ms

(1) See the*Volume, Treble, and Base Slew Rates Register (0xD0)* section.Section 7.27.

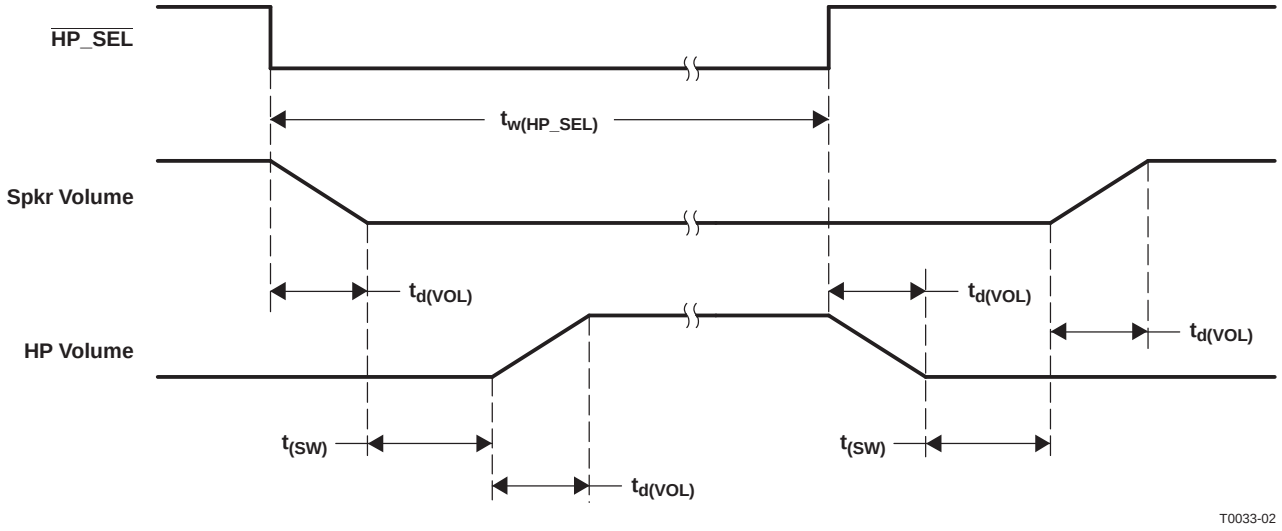


Figure 4-8. $\overline{HP_SEL}$ Timing

4.6.9 Volume Control

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Maximum attenuation before mute	Individual volume, master volume, or a combination of both		–127	dB
Maximum gain	Individual volume, master volume		18	dB
Maximum volume before the onset of clipping	0-dB input, any modulation limit		0	dB
PSVC range	PSVC enabled	12, 18, or 24		dB
PSVC rate		f_S		
PSVC modulation		Single sided		
PSVC quantization		2048		Steps
PSVC PWM modulation limits	PSVC range = 24 dB	6% (120 : 2048)	95% (1944 : 2048)	dB

Not Recommended For New Designs

4.7 Serial Audio Interface Control and Timing

4.7.1 I^2S Timing

I^2S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 64 f_S is used to clock in the data. From the time the LRCLK signal changes state to the first bit of data on the data lines is a delay of one bit clock. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS5518C masks unused trailing data bit positions.

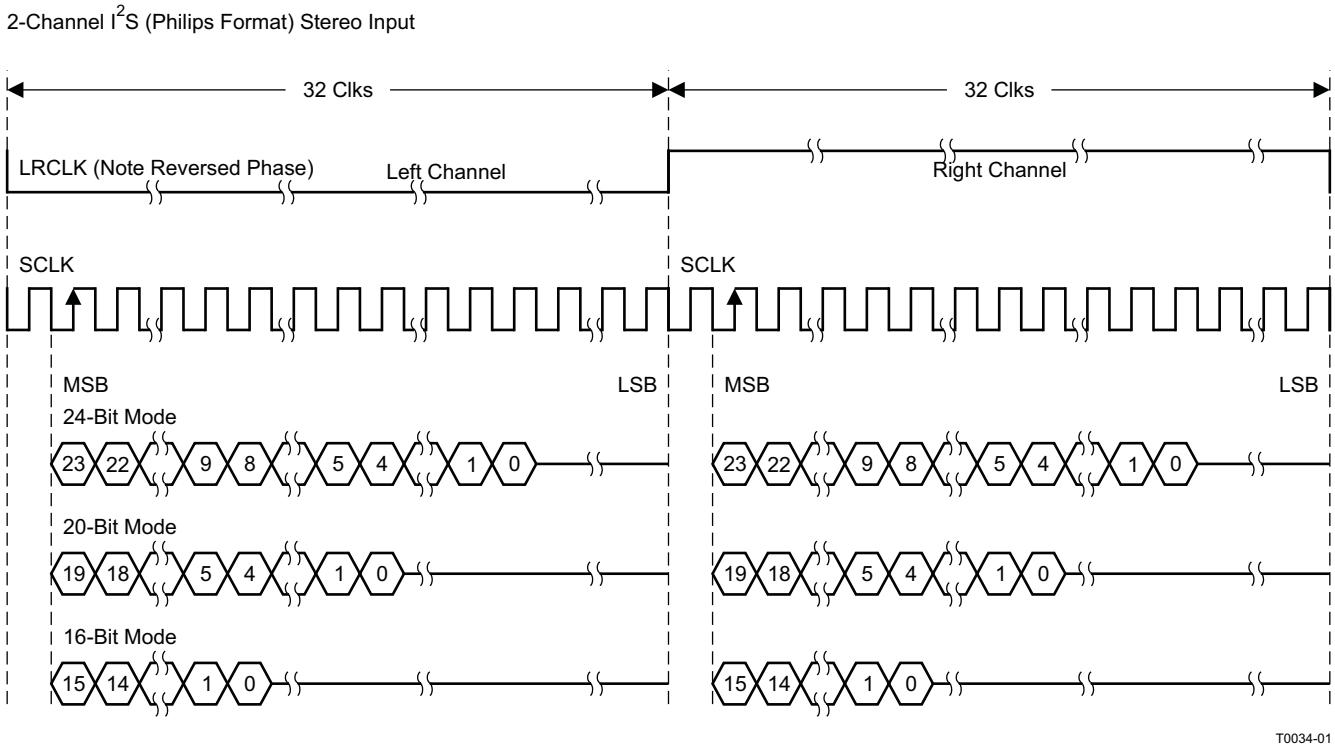


Figure 4-9. I^2S 64-f_S Format

Not Recommended For New Designs

4.7.2 Left-Justified Timing

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 64 f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS5518C masks unused trailing data bit positions.

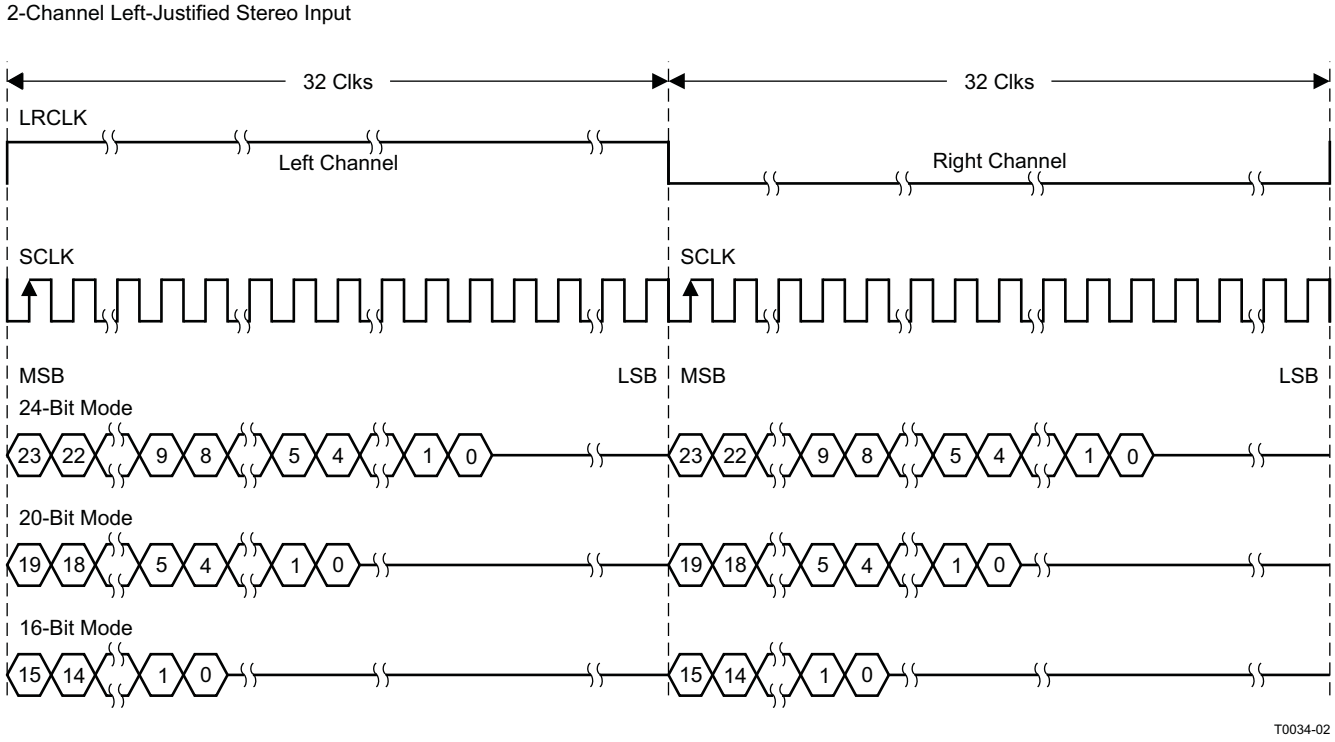


Figure 4-10. Left-Justified 64-f_S Format

Not Recommended For New Designs

4.7.3 Right-Justified Timing

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 64 f_S is used to clock in the data. The first bit of data appears on the data lines eight bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS5518C masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

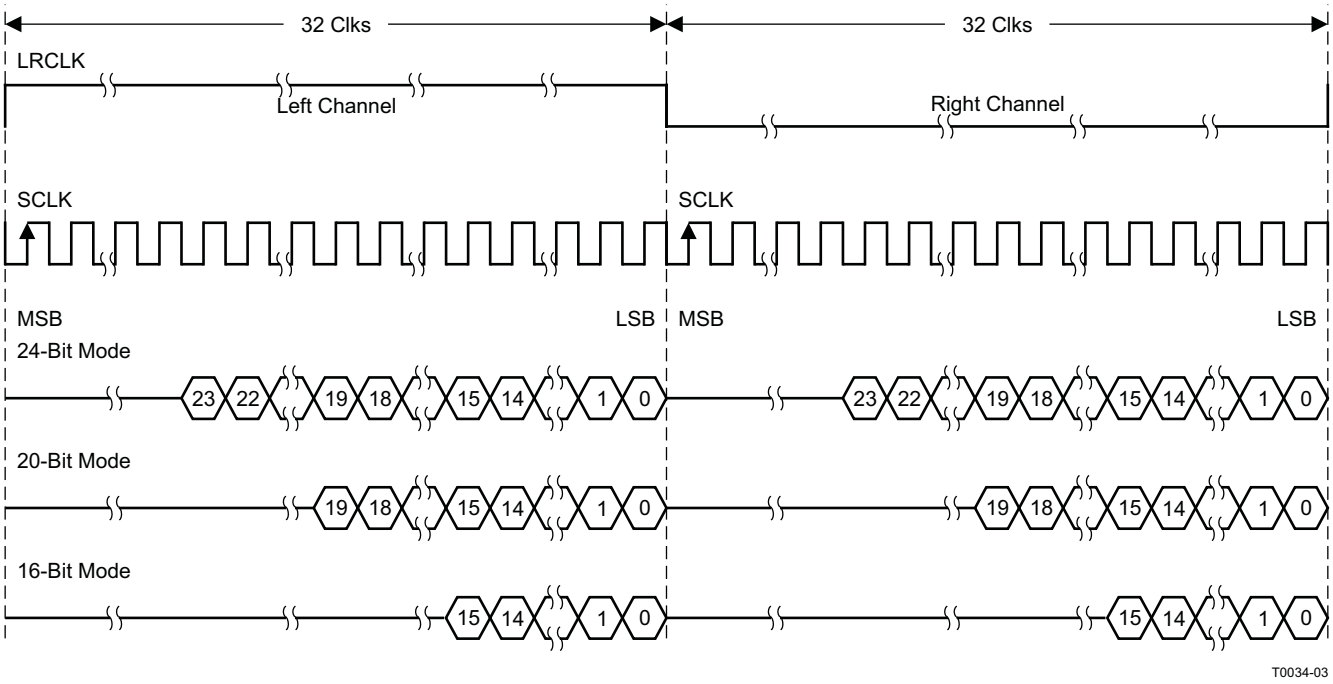


Figure 4-11. Right-Justified 64-f_S Format

Not Recommended For New Designs

5 I²C Serial-Control Interface (Slave Addresses 0x36 and 0x37)

The TAS5518C has a bidirectional I²C interface that is compatible with the Inter-IC (I²C) bus protocol and supports both 100-kbps and 400-kbps data transfer rates for single- and multiple-byte write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The TAS5518C supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The TAS5518C performs all I²C operations without I²C wait cycles.

The I²C write address is 0x36 and the I²C read address is 0x37.

5.1 General I²C Operation

The I²C bus employs two signals—SDA (data) and SCL (clock)—to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on SDA while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 5-1. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5518C holds SDA low during the acknowledge clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

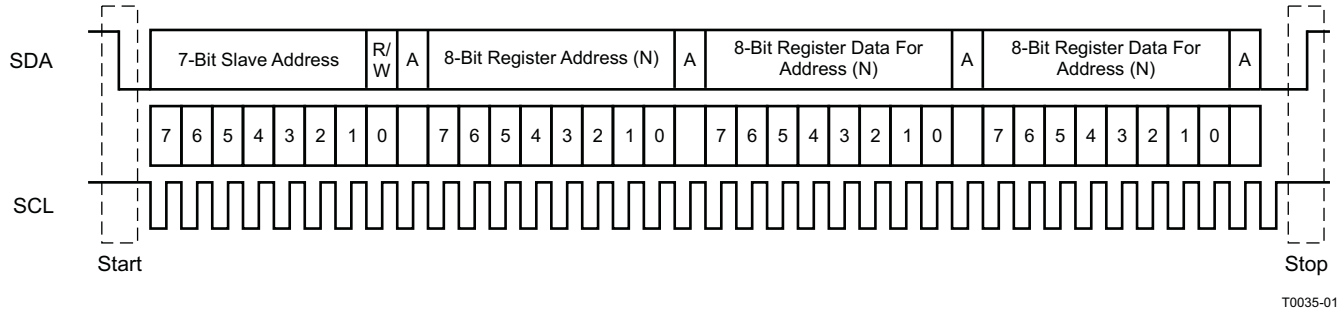


Figure 5-1. Typical I²C Sequence

The number of bytes that can be transmitted between start and stop conditions is unlimited. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 5-1.

The 7-bit address for the TAS5518C is 0011011. When the R/$\overline{W}$ bit is added as the LSB, the I²C write address is 0x36 and the I²C read address is 0x37.

Not Recommended For New Designs

5.2 Single- and Multiple-Byte Transfers

The serial-control interface supports both single-byte and multiple-byte read/write operations for status registers and the general control registers associated with the PWM. However, for the DAP data processing registers, the serial-control interface supports only multiple-byte (four-byte) read/write operations.

During multiple-byte read operations, the TAS5518C responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the TAS5518C compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. If a write command is received for a biquad subaddress, the TAS5518C expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded. Similarly, if a write command is received for a mixer coefficient, the TAS5518C expects to receive one 32-bit word.

Supplying a subaddress for each subaddress transaction is referred to as random I^2C addressing. The TAS5518C also supports sequential I^2C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I^2C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5518C. For I^2C sequential write transactions, the subaddress then serves as the start address and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As is true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

5.3 Single-Byte Write

As shown in Figure 5-2, a single-byte, data-write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I^2C device address and the read/write bit, the TAS5518C device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5518C internal memory address being accessed. After receiving the address byte, the TAS5518C again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5518C again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte, data-write transfer.

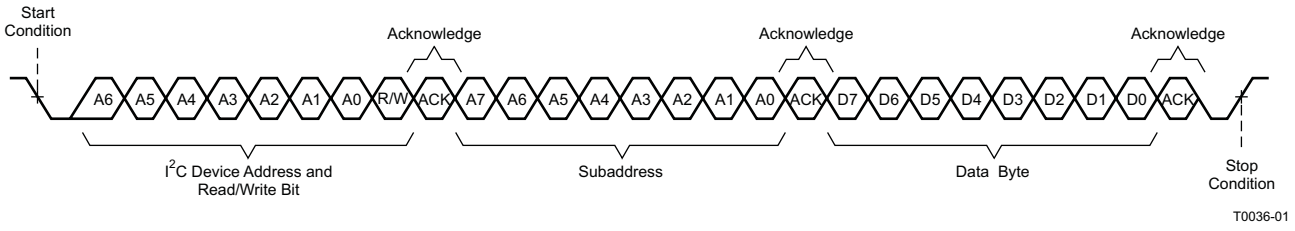


Figure 5-2. Single-Byte Write Transfer

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5.4 Multiple-Byte Write

A multiple-byte, data-write transfer is identical to a single-byte, data-write transfer except that multiple data bytes are transmitted by the master device to TAS5518C, as shown in Figure 5-3. After receiving each data byte, the TAS5518C responds with an acknowledge bit.

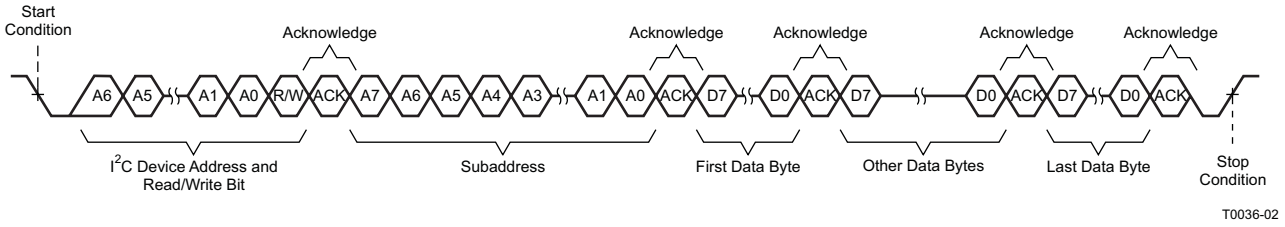

Figure 5-3. Multiple-Byte Write Transfer

5.5 Incremental Multiple-Byte Write

The I^2C supports a special mode which permits I^2C write operations to be broken up into multiple data write operations that are multiples of four data bytes. These are 6-byte, 10-byte, 14-byte, 18-byte, etc., write operations that are composed of a device address, read/write bit, subaddress, and any multiple of four bytes of data. This permits the system to write large register values incrementally without blocking other I^2C transactions.

This feature is enabled by the append subaddress function in the TAS5518C. This function enables the TAS5518C to append four bytes of data to a register that was opened by a previous I^2C register write operation but has not received its complete number of data bytes. Because the length of the long registers is a multiple of four bytes, using four-byte transfers has only an integral number of append operations.

When the correct number of bytes has been received, the TAS5518C starts processing the data.

The procedure to perform an incremental multibyte-write operation is as follows:

1. Start a normal I^2C write operation by sending the device address, write bit, register subaddress, and the first four bytes of the data to be written. At the end of that sequence, send a stop condition. At this point, the register has been opened and accepts the remaining data that is sent by writing four-byte blocks of data to the append subaddress (0xFE).
2. At a later time, one or more append data transfers are performed to incrementally transfer the remaining number of bytes in sequential order to complete the register write operation. Each of these append operations is composed of the device address, write bit, append subaddress (0xFE), and four bytes of data followed by a stop condition.
3. The operation is terminated due to an error condition, and the data is flushed:
   a. If a new subaddress is written to the TAS5518C before the correct number of bytes are written.
   b. If more or fewer than four bytes are data written at the beginning or during any of the append operations.
   c. If a read bit is sent.

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5.6 Single-Byte Read

As shown in Figure 5-4, a single-byte, data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data-read transfer, both a write and then a read are actually performed. Initially, a write is performed to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the TAS5518C address and the read/write bit, the TAS5518C responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5518C address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the TAS5518C address and the read/write bit, the TAS5518C again responds with an acknowledge bit. Next, the TAS5518C transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte, data-read transfer.

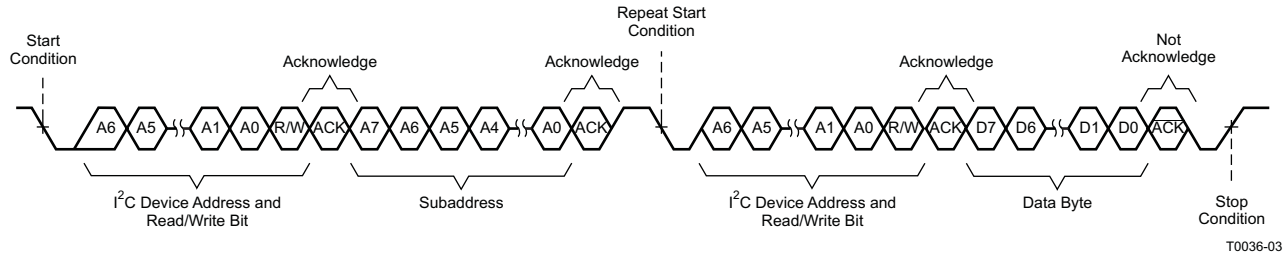

Figure 5-4. Single-Byte Read Transfer

5.7 Multiple-Byte Read

A multiple-byte, data-read transfer is identical to a single-byte, data-read transfer except that multiple data bytes are transmitted by the TAS5518C to the master device, as shown in Figure 5-5. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

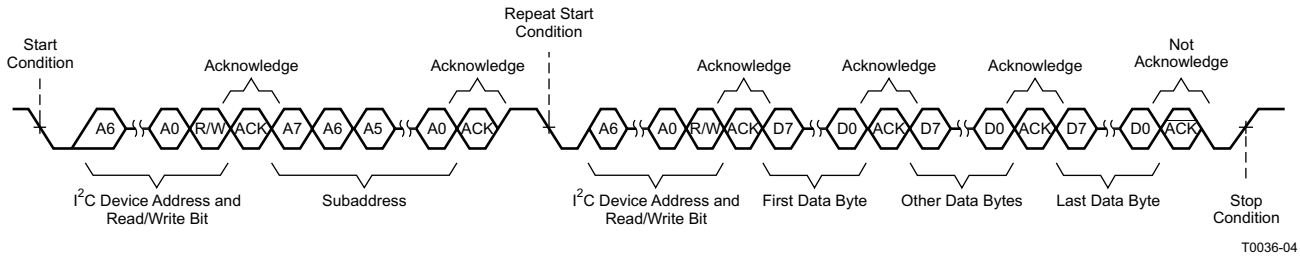

Figure 5-5. Multiple-Byte Read Transfer

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6 Serial-Control I²C Register Summary

The TAS5518C slave write address is 0x36 and the read address is 0x37. See *Serial-Control Interface Register Definitions*, Section 7 for complete bit definitions.

Note that u indicates unused bits.

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x00	1	Clock control register	Set data rate and MCLK frequency	1. f_S = 48 kHz 2. MCLK = 256 f_S = 12.288 MHz
0x01	1	General status register	Clip indicator and ID code for the TAS5518C	0x03
0x02	1	Error status register	PLL, SCLK, LRCLK, and frame slip errors	No errors
0x03	1	System control register 1	PWM high pass, clock set, unmute select, PSVC select	1. PWM (dc blocking) high-pass filter enabled 2. Auto clock set 3. Hard unmute on clock error recovery 4. PSVC Hi-Z disabled
0x04	1	System control register 2	Automute and de-emphasis control	1. Automute time-out disabled 2. Post-DAP detection automute enabled 3. 8-Ch device input detection automute enabled 4. Unmute threshold 6 dB over input 5. No de-emphasis
0x05–0x0C	1/reg.	Channel configuration control registers	Configure channels 1, 2, 3, 4, 5, 6, 7, and 8	1. Enable back-end reset. 2. VALID low for reset 3. VALID low for mute 4. Normal BEPolarity 5. Do not remap the output for the TAS5182 6. Do not go low-low in mute. 7. Do not remap Hi-Z state to low-low state.
0x0D	1	Headphone configuration control register	Configure headphone output	1. Disable back-end reset sequence. 2. VALID does not have to be low for reset. 3. VALID does not have to be low for mute. 4. Normal BEPolarity 5. Do not remap output to comply with TAS5182. 6. Do not go low-low in mute. 7. Do not remap Hi-Z state to low-low state.
0x0E	1	Serial data interface control register	Set serial data interface to right-justified, I²S, or left-justified.	24-bit I²S
0x0F	1	Soft mute register	Soft mute for channels 1, 2, 3, 4, 5, 6, 7, and 8	Unmute all channels.
0x10–0x13			Reserved	
0x14	1	Automute control register	Set automute delay and threshold.	1. Set automute delay = 5 ms. 2. Set automute threshold less than bit 8.
0x15	1	Automute PWM threshold and back-end reset period register	Set PWM automute threshold; set back-end reset period.	1. Set the PWM threshold the same as the TAS5518C input threshold. 2. Set back-end reset period = 5 ms.
0x16	1	Modulation index limit register	Set modulation index.	97.7%
0x17–0x1A			Reserved	
0x24–0x3F			Reserved	
0x40	4	Bank-switching command register	Set up DAP coefficients bank switching for banks 1, 2, and 3	Manual selection – bank 1

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x41–0x48	32/reg.	Input mixer registers, Ch1–Ch8	8×8 input crossbar mixer setup	SDIN1 – left to input mixer 1 SDIN1 – right to input mixer 2 SDIN2 – left to input mixer 3 SDIN2 – right to input mixer 4 SDIN3 – left to input mixer 5 SDIN3 – right to input mixer 6 SDIN4 – left to input mixer 7 SDIN4 – right to input mixer 8
0x49	4	ipmix_1_to_ch8	Input mixer 1 to Ch8 mixer coefficient	0.0
0x4A	4	ipmix_2_to_ch8	Input mixer 2 to Ch8 mixer coefficient	0.0
0x4B	4	ipmix_7_to_ch2	Input mixer 7 to Ch2 mixer coefficient	0.0
0x4C	4	Ch7_bp_bq2	Bypass Ch7 biquad 2 coefficient	0.0
0x4D	4	Ch7_bq2	Ch7 biquad 2 coefficient	1.0
0x4E	4	ipmix_8_to_ch12	Ch8 biquad 2 output to Ch1 mixer and Ch2 mixer coefficient	0.0
0x4F	4	Ch8_bp_bq2	Bypass Ch8 biquad 2 coefficient	0.0
0x50	4	Ch8_bq2	Ch8 biquad 2 coefficient	1.0
0x51–0x88	20/reg.	Biquad filter register	Ch1–Ch8 biquad filter coefficients	All biquads = All pass for all channels
0x89–0x90	8	Bass and treble bypass register, Ch1–Ch8	Bypass bass and treble for Ch1–Ch8	Bass and treble bypassed for all channels
0x91	4	Loudness Log2 LG	Loudness Log2 LG	0.5
0x92	8	Loudness Log2 LO	Loudness Log2 LO	0.0
0x93	4	Loudness G	Loudness G	0.0
0x94	8	Loudness O	Loudness O	0.0
0x95	20	Loudness biquad	Loudness biquad coefficient b0	0x00, 0x00, 0xD5, 0x13
			Loudness biquad coefficient b1	0x00, 0x00, 0x00, 0x00
			Loudness biquad coefficient b2	0x0F, 0xFF, 0x2A, 0xED
			Loudness biquad coefficient a0	0x00, 0xFE, 0x50, 0x45
			Loudness biquad coefficient a1	0x0F, 0x81, 0xAA, 0x27
0x96	4	DRC1 control Ch1–Ch7	DRC1 control Ch1–Ch7	DRC1 disabled in Ch1–Ch7
0x97	4	DRC2 control register, Ch8	DRC2 control Ch8	DRC2 disabled in Ch8
0x98	8	Ch1–Ch7, DRC1 energy	DRC1 energy	0.0041579
		Ch1–Ch7, DRC1 (1 – energy)	DRC1 (1 – energy)	0.9958421
0x99	16	Ch1–Ch7 DRC1 threshold T1	DRC1 threshold (T1) – upper 2 bytes	0x00, 0x00, 0x00, 0x00
			DRC1 threshold (T1) – lower 4 bytes	0x0B, 0x20, 0xE2, 0xB2
		Ch1–Ch7 DRC1 threshold T2	DRC1 threshold (T2) – upper 2 bytes	0x00, 0x00, 0x00, 0x00
			DRC1 threshold (T2) – lower 4 bytes	0x06, 0xF9, 0xDE, 0x58
0x9A	12	Ch1–Ch7 , DRC1 slope k0	DRC1 slope (k0)	0x0F, 0xC0, 0x00, 0x00
		Ch1–Ch7, DRC1 slope k1	DRC1 slope (k1)	0x0F, 0xC0, 0x00, 0x00
		Ch1–Ch7 DRC1 slope k2	DRC1 slope (k2)	0x0F, 0x90, 0x00, 0x00
0x9B	16	Ch1–Ch7 DRC1 offset 1	DRC1 offset 1 (O1) – upper 2 bytes	0x00, 0x00, 0xFF, 0xFF
			DRC1 offset 1 (O1) – lower 4 bytes	0xFF, 0x82, 0x30, 0x98
		Ch1–Ch7 DRC1 offset 2	DRC1 offset 2 (O2) – upper 2 bytes	0x00, 0x00, 0x00, 0x00
			DRC1 offset 2 (O2) – lower 4 bytes	0x01, 0x95, 0xB2, 0xC0
0x9C	16	Ch1–Ch7 DRC1 attack	DRC1 attack	0x00, 0x00, 0x88, 0x3F
		Ch1–Ch7 DRC1 (1 – attack)	DRC1 (1 – attack)	0x00, 0x7F, 0x77, 0xC0
		Ch1–Ch7 DRC1 decay	DRC1 decay	0x00, 0x00, 0x00, 0xAE
		Ch1–Ch7 DRC1 (1 – decay)	DRC1 (1 – decay)	0x00, 0x7F, 0xFF, 0x51
0x9D	8	Ch8 DRC2 energy	DRC2 energy	0x00, 0x00, 0x88, 0x3F
		Ch8 DRC2 (1 – energy)	DRC2 (1 – energy)	0x00, 0x7F, 0x77, 0xC0
0x9E	16	Ch8 DRC2 threshold T1	DRC2 threshold (T1) – upper 2 bytes	0x00, 0x00, 0x00, 0x00
			DRC2 threshold (T1) – lower 4 bytes	0x0B, 0x20, 0xE2, 0xB2
		Ch8 DRC2 threshold T2	DRC2 threshold (T2) – upper 2 bytes	0x00, 0x00, 0x00, 0x00
			DRC2 threshold (T2) – lower 4 bytes	0x06, 0xF9, 0xDE, 0x58

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I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x9F	12	Ch8 DRC2 slope k0	DRC2 slope (k0)	0x00, 0x40, 0x00, 0x00
		Ch8 DRC2 slope k1	DRC2 slope (k1)	0x0F, 0xC0, 0x00, 0x00
		Ch8 DRC2 slope k2	DRC2 slope (k2)	0x0F, 0x90, 0x00, 0x00
0xA0	16	Ch8 DRC2 offset 1	DRC2 offset (O1) – upper 2 bytes	0x00, 0x00, 0xFF, 0xFF
			DRC2 offset (O1) – lower 4 bytes	0xFF, 0x82, 0x30, 0x98
		Ch8 DRC2 offset 2	DRC2 offset (O2) – upper 2 bytes	0x00, 0x00, 0x00, 0x00
			DRC2 offset (O2) – lower 4 bytes	0x01, 0x95, 0xB2, 0xC0
0xA1	16	Ch8 DRC2 attack	DRC 2 attack	0x00, 0x00, 0x88, 0x3F
		Ch8 DRC2 (1 – attack)	DRC2 (1 – attack)	0x00, 0x7F, 0x77, 0xC0
		Ch8 DRC2 decay	DRC2 decay	0x00, 0x00, 0x00, 0xAE
		Ch8 DRC2 (1 – decay)	DRC2 (1 – decay)	0x00, 0x7F, 0xFF, 0x51
0xA2	8	DRC bypass 1	Ch1 DRC1 bypass coefficient	1.0
		DRC inline 1	Ch1 DRC1 inline coefficient	0.0
0xA3	8	DRC bypass 2	Ch2 DRC1 bypass coefficient	1.0
		DRC inline 2	Ch2 DRC1 inline coefficient	0.0
0xA4	8	DRC bypass 3	Ch3 DRC1 bypass coefficient	1.0
		DRC inline 3	Ch3 DRC1 inline coefficient	0.0
0xA5	8	DRC bypass 4	Ch4 DRC1 bypass coefficient	1.0
		DRC inline 4	Ch4 DRC1 inline coefficient	0.0
0xA6	8	DRC bypass 5	Ch5 DRC1 bypass coefficient	1.0
		DRC inline 5	Ch5 DRC1 inline coefficient	0.0
0xA7	8	DRC bypass 6	Ch6 DRC1 bypass coefficient	1.0
		DRC inline 6	Ch6 DRC1 inline coefficient	0.0
0xA8	8	DRC bypass 7	Ch7 DRC1 bypass coefficient	1.0
		DRC inline 7	Ch7 DRC1 inline coefficient	0.0
0xA9	8	DRC bypass 8	Ch8 DRC2 bypass coefficient	1.0
		DRC inline 8	Ch8 DRC2 inline coefficient	0.0
0xAA	8	sel op1–8 and mix to PWM1	Select 0 to 2 of eight channels to output mixer 1	Select Channel 1 to PWM1.
0xAB	8	sel op1–8 and mix to PWM2	Select 0 to 2 of eight channels to output mixer 2	Select Channel 2 to PWM2.
0xAC	8	sel op1–8 and mix to PWM3	Select 0 to 2 of eight channels to output mixer 3	Select Channel 3 to PWM3.
0xAD	8	sel op1–8 and mix to PWM4	Select 0 to 2 of eight channels to output mixer 4	Select Channel 4 to PWM4.
0xAE	8	sel op1–8 and mix to PWM5	Select 0 to 2 of eight channels to output mixer 5	Select Channel 5 to PWM5.
0xAF	8	sel op1–8 and mix to PWM6	Select 0 to 2 of eight channels to output mixer 6	Select Channel 6 to PWM6.
0xB0	12	sel op1–8 and mix to PWM7	Select 0 to 3 of eight channels to output mixer 7	Select Channel 7 to PWM7.
0xB1	12	sel op1–8 and mix to PWM8	Select 0 to 3 of eight channels to output mixer 8	Select Channel 8 to PWM8.
0xB2–0xCE			Reserved	
0xCF	20	Volume biquad	Volume biquad	All pass
0xD0	4	Volume, treble, and bass slew rates register	u [31:24], u [23:16], u [15:12] VSR[11:8], TBSR[7:0]	0x00, 0x00, 0x01, 0x3F
0xD1	4	Ch1 volume	Ch1 volume	0 dB
0xD2	4	Ch2 volume	Ch2 volume	0 dB
0xD3	4	Ch3 volume	Ch3 volume	0 dB
0xD4	4	Ch4 volume	Ch4 volume	0 dB
0xD5	4	Ch5 volume	Ch5 volume	0 dB
0xD6	4	Ch6 volume	Ch6 volume	0 dB
0xD7	4	Ch7 volume	Ch7 volume	0 dB
0xD8	4	Ch8 volume	Ch8 volume	0 dB

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I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0xD9	4	Master volume	Master volume	Mute
0xDA	4	Bass filter set register	Bass filter set (all channels)	Filter set 3
0xDB	4	Bass filter index register	Bass filter level (all channels)	0 dB
0xDC	4	Treble filter set register	Treble filter set (all channels)	Filter set 3
0xDD	4	Treble filter index register	Treble filter level (all channels)	0 dB
0xDE	4	AM mode register	Set up AM mode for AM-interference reduction	AM mode disabled Select sequence 1 IF frequency = 455 kHz Use BCD-tuned frequency
0xDF	4	PSVC range register	Set PSVC control range	12-dB control range
0xE0	4	General control register	6- or 8-channel configuration, PSVC enable	8-channel configuration Power-supply volume control disabled
0xE1–0xFD			Reserved	
0xFE	4 (min)	Multiple-byte write-append register	Special register	N/A
0xFF			Reserved	

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7 Serial-Control Interface Register Definitions

Unless otherwise noted, the I^2C register default values are in **bold** font.

Note that u indicates unused bits.

7.1 Clock Control Register (0x00)

Bit D1 is *don't care*.

Table 7-1. Clock Control Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–	X	–	32-kHz data rate
0	0	1	–	–	–	X	–	38-kHz data rate
0	1	0	–	–	–	X	–	44.1-kHz data rate
0	**1**	**1**	**–**	**–**	**–**	X	**–**	**48-kHz data rate**
1	0	0	–	–	–	X	–	88.2-kHz data rate
1	0	1	–	–	–	X	–	96-kHz data rate
1	1	0	–	–	–	X	–	176.4-kHz data rate
1	1	1	–	–	–	X	–	192-kHz data rate
–	–	–	0	0	0	X		MCLK frequency = 64
–	–	–	0	0	1	X		MCLK frequency = 128
–	–	–	0	1	0	X		MCLK frequency = 192
–	**–**	**–**	**0**	**1**	**1**	X		**MCLK frequency = 256**
–	–	–	1	0	0	X		MCLK frequency = 384
–	–	–	1	0	1	X		MCLK frequency = 512
–	–	–	1	1	0	X		MCLK frequency = 768
–	–	–	1	1	1	X		Reserved
–	–	–	–	–	–	X	1	Clock register is valid (read-only)
–	**–**	**–**	**–**	**–**	**–**	X	**0**	**Clock register is not valid (read-only)**

7.2 General Status Register 0 (0x01)

Table 7-2. General Status Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	Clip indicator
–	1	–	–	–	–	–	–	Bank switching busy
–	**–**	**0**	**0**	**0**	**0**	**0**	**1**	**Identification code for TAS5518C**

7.3 Error Status Register (0x02)

Note that the error bits are sticky bits that are not cleared by the hardware. This means that the software must clear the register (write zeroes) and than read them to determine if there are any persistent errors.

Table 7-3. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	PLL phase lock error
–	1	–	–	–	–	–	–	PLL auto lock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip

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Table 7-3. Error Status Register (0x02) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No errors

7.4 System Control Register 1 (0x03)

Bits D6, D5, D2, D1, and D0 are *don't care*.

Table 7-4. System Control Register-1 Format

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	**–**	–	**–**	**–**	–	–	–	PWM high pass disabled
1	–	–	–	–	–	–	–	**PWM high pass enabled**
–	–	–	0	–	–	–	–	Soft unmute on recovery from clock error
–	**–**	–	**1**	–	–	–	–	**Hard unmute on recovery from clock error**
–	–	–	–	1	–	–	–	PSVC Hi-Z enabled
–	**–**	–	**–**	**0**	–	–	–	**PSVC Hi-Z disabled**

7.5 System Control Register 2 (0x04)

Bits D3 and D2 are *don't care*.

Table 7-5. System Control Register-2 Format

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	**–**	**–**	**–**			**–**	**–**	**Reserved**
–	**0**	**–**	**–**			**–**	**–**	**PWM output automute detection enabled**
–	1	–	–			–	–	PWM output automute detection disabled
–	–	**0**	**–**			**–**	**–**	**8-channel device input detection automute enabled**
–	–	1	–			–	–	8-channel device input detection automute disabled
–	**–**	**–**	**0**			**–**	**–**	**Unmute threshold 6 dB over input threshold**
–	–	–	1			–	–	Unmute threshold equal to input threshold
–	**–**	**–**	**–**			**0**	**0**	**No de-emphasis**
–	–	–	–			0	1	De-emphasis for f_S = 32 kHz
–	–	–	–			1	0	De-emphasis for f_S = 44.1 kHz
–	–	–	–			1	1	De-emphasis for f_S = 48 kHz

7.6 Channel Configuration Control Registers (0x05–0x0C)

Channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, and 0x0C, respectively.

Table 7-6. Channel Configuration Control Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–		Disable back-end reset sequence for a channel.
1	–	–	–	–	–	–		**Enable back-end reset sequence for a channel.**
–	0	–	–	–	–	–		Valid does not have to be low for this channel to be reset.
–	**1**	–	–	–	–	–		**Valid must be low for this channel to be reset.**
–	–	0	–	–	–	–		Valid does not have to be low for this channel to be muted.
–	–	**1**	–	–	–	–		**Valid must be low for this channel to be muted.**
–	–	–	**0**	–	–	–		**Normal BEPolarity**
–	–	–	1	–	–	–		Switches PWM+ and PWM– and inverts audio signal

Not Recommended For New Designs

Table 7-6. Channel Configuration Control Register Format (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	**0**	–	–		**Do not remap output to comply with 5182 interface.**
–	–	–	–	1	–	–		Remap output to comply with 5182 interface.
–	–	–	–	–	**0**	–		**Do not go to low-low in mute.**
–	–	–	–	–	1	–		Go to low-low in mute.
–	–	–	–	–	–	**0**		**Do not remap Hi-Z state to low-low state.**
–	–	–	–	–	–	1		Remap Hi-Z state to low-low state.

Not Recommended For New Designs

7.7 Headphone Configuration Control Register (0x0D)

Bit D0 is *don't care*.

Table 7-7. Headphone Configuration Control Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–		**Disable back-end reset sequence for a channel.**
1	–	–	–	–	–	–		Enable back-end reset sequence for a channel.
–	**0**	–	–	–	–	–		**Valid does not have to be low for this channel to be reset.**
–	1	–	–	–	–	–		Valid must be low for this channel to be reset.
–	–	**0**	–	–	–	–		**Valid does not have to be low for this channel to be muted.**
–	–	1	–	–	–	–		Valid must be low for this channel to be muted.
–	–	–	**0**	–	–	–		**Normal BEPolarity**
–	–	–	1	–	–	–		Switches PWM+ and PWM– and inverts audio signal
–	–	–	–	**0**	–	–		**Do not remap output to comply with 5182 interface.**
–	–	–	–	1	–	–		Remap output to comply with 5182 interface.
–	–	–	–	–	**0**	–		**Do not go to low-low in mute.**
–	–	–	–	–	1	–		Go to low-low in mute.
–	–	–	–	–	–	**0**		**Do not remap Hi-Z state to low-low state.**
–	–	–	–	–	–	1		Remap Hi-Z state to low-low state.

7.8 Serial Data Interface Control Register (0x0E)

Nine serial modes can be programmed via the I^2C interface.

Table 7-8. Serial Data Interface Control Register Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTHS	D7–D4	D3	D2	D1	D0
Right-justified	16	0000	0	0	0	0
Right-justified	20	0000	0	0	0	1
Right-justified	24	0000	0	0	1	0
I^2S	16	0000	0	0	1	1
I^2S	20	0000	0	1	0	0
I^2S	**24**	0000	**0**	**1**	**0**	**1**
Left-justified	16	0000	0	1	1	0
Left-justified	20	0000	0	1	1	1
Left-justified	24	0000	1	0	0	0
Illegal		0000	1	0	0	1
Illegal		0000	1	0	1	0
Illegal		0000	1	0	1	1
Illegal		0000	1	1	0	0
Illegal		0000	1	1	0	1
Illegal		0000	1	1	1	0
Illegal		0000	1	1	1	1

Not Recommended For New Designs

7.9 Soft Mute Register (0x0F)

Do not use this register if using the remapped output mixer configuration.

Table 7-9. Soft Mute Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	–	–	1	Soft mute channel 1
–	–	–	–	–	–	1	–	Soft mute channel 2
–	–	–	–	–	1	–	–	Soft mute channel 3
–	–	–	–	1	–	–	–	Soft mute channel 4
–	–	–	1	–	–	–	–	Soft mute channel 5
–	–	1	–	–	–	–	–	Soft mute channel 6
–	1	–	–	–	–	–	–	Soft mute channel 7
1	–	–	–	–	–	–	–	Soft mute channel 8
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Unmute all channels**

7.10 Automute Control Register (0x14)

For more information on how to use this register, see *Automute and Mute Channel Controls*, Section 2.8.

Table 7-10. Automute Control Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	0	0	0	0	Set input automute and output automute delay to 1 ms
–	–	–	–	0	0	0	1	Set input automute and output automute delay to 2 ms
–	–	–	–	0	0	1	0	Set input automute and output automute delay to 3 ms
–	–	–	–	0	0	1	1	Set input automute and output automute delay to 4 ms
–	–	–	–	**0**	**1**	**0**	**0**	**Set input automute and output automute delay to 5 ms**
–	–	–	–	0	1	0	1	Set input automute and output automute delay to 10 ms
–	–	–	–	0	1	1	0	Set input automute and output automute delay to 20 ms
–	–	–	–	0	1	1	1	Set input automute and output automute delay to 30 ms
–	–	–	–	1	0	0	0	Set input automute and output automute delay to 40 ms
–	–	–	–	1	0	0	1	Set input automute and output automute delay to 50 ms
–	–	–	–	1	0	1	0	Set input automute and output automute delay to 60 ms
–	–	–	–	1	0	1	1	Set input automute and output automute delay to 70ms
–	–	–	–	1	1	0	0	Set input automute and output automute delay to 80 ms
–	–	–	–	1	1	0	1	Set input automute and output automute delay to 90 ms
–	–	–	–	1	1	1	0	Set input automute and output automute delay to 100 ms
–	–	–	–	1	1	1	1	Set input automute and output automute delay to 110 ms
0	0	0	0	–	–	–		Set input automute threshold less than bit 1 (zero input signal), lowest automute threshold.
0	0	0	1	–	–	–	–	
0	0	1	0	–	–	–	–	Set input automute threshold less than bit 2
0	0	1	1	–	–	–	–	Set input automute threshold less than bit 3
0	1	0	0	–	–	–	–	Set input automute threshold less than bit 4
0	1	0	1	–	–	–	–	Set input automute threshold less than bit 5
0	1	1	0	–	–	–	–	Set input automute threshold less than bit 6
0	1	1	1	–	–	–	–	Set input automute threshold less than bit 7
1	**0**	**0**	**0**	–	–	–	–	**Set input automute threshold less than bit 8**
1	0	0	1	–	–	–	–	Set input automute threshold less than bit 9
1	0	1	0	–	–	–	–	Set input automute threshold less than bit 10
1	0	1	1	–	–	–	–	Set input automute threshold less than bit 11
1	1	0	0	–	–	–	–	Set input automute threshold less than bit 12
1	1	0	1	–	–	–	–	Set input automute threshold less than bit 13
1	1	1	0	–	–	–	–	Set input automute threshold less than bit 14
1	1	1	1	–	–	–	–	Set input automute threshold less than bit 15

Not Recommended For New Designs

7.11 Output Automute PWM Threshold and Back-End Reset Period Register (0x15)

For more information on how to use this register, see *Automute and Mute Channel Controls*, Section 2.8.

Table 7-11. Automute PWM Threshold and Back-End Reset Period Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	–	–	–	–	**Set output automute threshold equal to input automute threshold**
0	0	0	1	–	–	–	–	Set output automute threshold 1 bit more than input automute threshold
0	0	1	0	–	–	–	–	Set output automute threshold 2 bits more than input automute threshold
0	0	1	1	–	–	–	–	Set output automute threshold 3 bits more than input automute threshold
0	1	0	0	–	–	–	–	Set output automute threshold 4 bits more than input automute threshold
0	1	0	1	–	–	–	–	Set output automute threshold 5 bits more than input automute threshold
0	1	1	0	–	–	–	–	Set output automute threshold 6 bits more than input automute threshold
0	1	1	1	–	–	–	–	Set output automute threshold 7 bits more than input automute threshold
1	0	0	0	–	–	–	–	Set output automute threshold equal to input automute threshold
1	0	0	1	–	–	–	–	Set output automute threshold 1 bit less than input automute threshold
1	0	1	0	–	–	–	–	Set output automute threshold 2 bits less than input automute threshold
1	0	1	1	–	–	–	–	Set output automute threshold 3 bits less than input automute threshold
1	1	0	0	–	–	–	–	Set output automute threshold 4 bits less than input automute threshold
1	1	0	1	–	–	–	–	Set output automute threshold 5 bits less than input automute threshold
1	1	1	0	–	–	–	–	Set output automute threshold 6 bits less than input automute threshold
1	1	1	1	–	–	–	–	Set output automute threshold 7 bits less than input automute threshold
–	–	–	–	0	0	0	0	Set back-end reset period < 1 ms
–	–	–	–	0	0	0	1	Set back-end reset period 1 ms
–	–	–	–	0	0	1	0	Set back-end reset period 2 ms
–	–	–	–	0	0	1	1	Set back-end reset period 3 ms
–	–	–	–	0	1	0	0	Set back-end reset period 4 ms
–	–	–	–	**0**	**1**	**0**	**1**	**Set back-end reset period 5 ms**
–	–	–	–	0	1	1	0	Set back-end reset period 6 ms
–	–	–	–	0	1	1	1	Set back-end reset period 7 ms
–	–	–	–	1	0	0	0	Set back-end reset period 8 ms
–	–	–	–	1	0	0	1	Set back-end reset period 9 ms
–	–	–	–	1	0	1	0	Set back-end reset period 10 ms
–	–	–	–	1	0	1	1	Set back-end reset period 10 ms
–	–	–	–	1	1	X	X	Set back-end reset period 10 ms

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7.12 Modulation Index Limit Register (0x16)

Bits D7–D3 are *don't care*. Note that some power stages require a lower modulation limit than the default of 97.7%. Contact Texas Instruments for more details about the requirements for a particular power stage.

Table 7-12. Modulation Index Limit Register Format

D7	D6	D5	D4	D3	D2	D1	D0	LIMIT [DCLKs]	MIN WIDTH [DCLKs]	MODULATION INDEX
					0	0	0	1	2	99.2%
					0	0	1	2	4	98.4%
					0	**1**	**0**	**3**	**6**	**97.7%**
					0	1	1	4	8	96.9%
					1	0	0	5	10	96.1%
					1	0	1	6	12	95.3%
					1	1	0	7	14	94.5%
					1	1	1	8	16	93.8%

7.13 Bank-Switching Command Register (0x40)

Bits D31–D24, D22–D19 are *don't care*.

Table 7-13. Bank-Switching Command Register Format

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
–					**0**	**0**	**0**	**Manual selection bank 1**
–					0	0	1	Manual selection bank 2
–					0	1	0	Manual selection bank 3
–					0	1	1	Automatic bank selection
–					1	0	0	Update the values in bank 1
–					1	0	1	Update the values in bank 2
–					1	1	0	Update the values in bank 3
–					1	1	1	Update only the bank map
0					–	–	–	Update the bank map using values in D15–D0
1					–	–	–	Do not update the bank map using values in D15–D0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
1	–	–	–	–	–	–	–	**32-kHz data rate—use bank 1**
–	**1**	–	–	–	–	–	–	**38-kHz data rate—use bank 1**
–	–	**1**	–	–	–	–	–	**44.1-kHz data rate—use bank 1**
–	–	–	**1**	–	–	–	–	**48-kHz data rate—use bank 1**
–	–	–	–	**1**	–	–	–	**88.2-kHz data rate—use bank 1**
–	–	–	–	–	**1**	–	–	**96-kHz data rate—use bank 1**
–	–	–	–	–	–	**1**	–	**176.4-kHz data rate—use bank 1**
–	–	–	–	–	–	–	**1**	**192-kHz data rate—use bank 1**
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**Default**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
1	–	–	–	–	–	–	–	32-kHz data rate—use bank 2
–	1	–	–	–	–	–	–	38-kHz data rate—use bank 2
–	–	1	–	–	–	–	–	44.1-kHz data rate—use bank 2
–	–	–	1	–	–	–	–	48-kHz data rate—use bank 2

Not Recommended For New Designs

Table 7-13. Bank-Switching Command Register Format (continued)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
–	–	–	–	1	–	–	–	88.2-kHz data rate—use bank 2
–	–	–	–	–	1	–	–	96-kHz data rate—use bank 2
–	–	–	–	–	–	1	–	176.4-kHz data rate—use bank 2
–	–	–	–	–	–	–	1	192-kHz data rate—use bank 2
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default**

7.14 Input Mixer Registers, Channels 1–8 (0x41–0x48)

Input mixers 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, and 0x48, respectively.

Each gain coefficient is in 28-bit (5.23) format, so 0x80 0000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used. For eight gain coefficients, the total is 32 bytes.

Bold indicates the one channel that is passed through the mixer.

Table 7-14. Channel 1–8 Input Mixer Register Format

I^2C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x41	32	**A_to_ipmix[1]**	**SDIN1-left (Ch1) A to input mixer 1 coefficient (default = 1) u[31:28], A_1[27:24], A_1[23:16], A_1[15:8], A_1[7:0]**	**0x00, 0x80, 0x00, 0x00**
		B_to_ipmix[1]	SDIN1-right (Ch2) B to input mixer 1 coefficient (default = 0) u[31:28], B_1[27:24], B_1[23:16], B_1[15:8], B_1[7:0]	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[1]	SDIN2-left (Ch3) C to input mixer 1 coefficient (default = 0) u[31:28], C_1[27:24], C_1[23:16], C_1[15:8], C_1[7:0]	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[1]	SDIN2-right (Ch4) D to input mixer 1 coefficient (default = 0) u[31:28], D_1[27:24], D_1[23:16], D_1[15:8], D_1[7:0]	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[1]	SDIN3-left (Ch5) E to input mixer 1 coefficient (default = 0) u[31:28], E_1[27:24], E_1[23:16], E_1[15:8], E_1[7:0]	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[1]	SDIN3-right (Ch6) F to input mixer 1 coefficient (default = 0) u[31:28], F_1[27:24], F_1[23:16], F_1[15:8], F_1[7:0]	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[1]	SDIN4-left (Ch7) G to input mixer 1 coefficient (default = 0) u[31:28], G_1[27:24], G_1[23:16], G_1[15:8], G_1[7:0]	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[1]	SDIN4-right (Ch8) H to input mixer 1 coefficient (default = 0) u[31:28], H_1[27:24], H_1[23:16], H_1[15:8], H_1[7:0]	0x00, 0x00, 0x00, 0x00
0x42	32	A_to_ipmix[2]	SDIN1-left (Ch1) A to input mixer 2 coefficient (default = 0) u[31:28], A_2[27:24], A_2[23:16], A_2[15:8], A_2[7:0]	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[2]	**SDIN1-right (Ch2) B to input mixer 2 coefficient (default = 1) u[31:28], B_2[27:24], B_2[23:16], B_2[15:8], B_2[7:0]**	**0x00, 0x80, 0x00, 0x00**
		C_to_ipmix[2]	SDIN2-left (Ch3) C to input mixer 2 coefficient (default = 0) u[31:28], C_2[27:24], C_2[23:16], C_2[15:8], C_2[7:0]	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[2]	SDIN2-right (Ch4) D to input mixer 2 coefficient (default = 0) u[31:28], D_2[27:24], D_2[23:16], D_2[15:8], D_2[7:0]	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[2]	SDIN3-left (Ch5) E to input mixer 2 coefficient (default = 0) u[31:28], E_2[27:24], E_2[23:16], E_2[15:8], E_2[7:0]	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[2]	SDIN3-right (Ch6) F to input mixer 2 coefficient (default = 0) u[31:28], F_2[27:24], F_2[23:16], F_2[15:8], F_2[7:0]	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[2]	SDIN4-left (Ch7) G to input mixer 2 coefficient (default = 0) u[31:28], G_2[27:24], G_2[23:16], G_2[15:8], G_2[7:0]	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[2]	SDIN4-right (Ch8) H to input mixer 2 coefficient (default = 0) u[31:28], H_2[27:24], H_2[23:16], H_2[15:8], H_2[7:0]	0x00, 0x00, 0x00, 0x00

Not Recommended For New Designs

Table 7-14. Channel 1–8 Input Mixer Register Format (continued)

I^2C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x43	32	A_to_ipmix[3]	SDIN1-left (Ch1) A to input mixer 3 coefficient (default = 0) u[31:28], A_3[27:24], A_3[23:16], A_3[15:8], A_3[7:0]	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[3]	SDIN1-right (Ch2) B to input mixer 3 coefficient (default = 0) u[31:28], B_3[27:24], B_3[23:16], B_3[15:8], B_3[7:0]	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[3]	**SDIN2-left (Ch3) C to input mixer 3 coefficient (default = 1) u[31:28], C_3[27:24], C_3[23:16], C_3[15:8], C_3[7:0]**	**0x00, 0x80, 0x00, 0x00**
		D_to_ipmix[3]	SDIN2-right (Ch4) D to input mixer 3 coefficient (default = 0) u[31:28], D_3[27:24], D_3[23:16], D_3[15:8], D_3[7:0]	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[3]	SDIN3-left (Ch5) E to input mixer 3 coefficient (default = 0) u[31:28], E_3[27:24], E_3[23:16], E_3[15:8], E_3[7:0]	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[3]	SDIN3-right (Ch6) F to input mixer 3 coefficient (default = 0) u[31:28], F_3[27:24], F_3[23:16], F_3[15:8], F_3[7:0]	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[3]	SDIN4-left (Ch7) G to input mixer 3 coefficient (default = 0) u[31:28], G_3[27:24], G_3[23:16], G_3[15:8], G_3[7:0]	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[3]	SDIN4-right (Ch8) H to input mixer 3 coefficient (default = 0) u[31:28], H_3[27:24], H_3[23:16], H_3[15:8], H_3[7:0]	0x00, 0x00, 0x00, 0x00
0x44	32	A_to_ipmix[4]	SDIN1-left (Ch1) A to input mixer 4 coefficient (default = 0) u[31:28], A_4[27:24], A_4[23:16], A_4[15:8], A_4[7:0]	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[4]	SDIN1-right (Ch2) B to input mixer 4 coefficient (default = 0) u[31:28], B_4[27:24], B_4[23:16], B_4[15:8], B_4[7:0]	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[4]	SDIN2-left (Ch3) C to input mixer 4 coefficient (default = 0) u[31:28], C_4[27:24], C_4[23:16], C_4[15:8], C_4[7:0]	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[4]	**SDIN2-right (Ch4) D to input mixer 4 coefficient (default = 1) u[31:28], D_4[27:24], D_4[23:16], D_4[15:8], D_4[7:0]**	**0x00, 0x80, 0x00, 0x00**
		E_to_ipmix[4]	SDIN3-left (Ch5) E to input mixer 4 coefficient (default = 0) u[31:28], E_4[27:24], E_4[23:16], E_4[15:8], E_4[7:0]	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[4]	SDIN3-right (Ch6) F to input mixer 4 coefficient (default = 0) u[31:28], F_4[27:24], F_4[23:16], F_4[15:8], F_4[7:0]	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[4]	SDIN4-left (Ch7) G to input mixer 4 coefficient (default = 0) u[31:28], G_4[27:24], G_4[23:16], G_4[15:8], G_4[7:0]	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[4]	SDIN4-right (Ch8) H to input mixer 4 coefficient (default = 0) u[31:28], H_4[27:24], H_4[23:16], H_4[15:8], H_4[7:0]	0x00, 0x00, 0x00, 0x00
0x45	32	A_to_ipmix[5]	SDIN1-left (Ch1) A to input mixer 5 coefficient (default = 0) u[31:28], A_5[27:24], A_5[23:16], A_5[15:8], A_5[7:0]	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[5]	SDIN1-right (Ch2) B to input mixer 5 coefficient (default = 0) u[31:28], B_5[27:24], B_5[23:16], B_5[15:8], B_5[7:0]	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[5]	SDIN2-left (Ch3) C to input mixer 5 coefficient (default = 0) u[31:28], C_5[27:24], C_5[23:16], C_5[15:8], C_5[7:0]	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[5]	SDIN2-right (Ch4) D to input mixer 5 coefficient (default = 0) u[31:28], D_5[27:24], D_5[23:16], D_5[15:8], D_5[7:0]	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[5]	**SDIN3-left (Ch5) E to input mixer 5 coefficient (default = 1) u[31:28], E_5[27:24], E_5[23:16], E_5[15:8], E_5[7:0]**	**0x00, 0x80, 0x00, 0x00**
		F_to_ipmix[5]	SDIN3-right (Ch6) F to input mixer 5 coefficient (default = 0) u[31:28], F_5[27:24], F_5[23:16], F_5[15:8], F_5[7:0]	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[5]	SDIN4-left (Ch7) G to input mixer 5 coefficient (default = 0) u[31:28], G_5[27:24], G_5[23:16], G_5[15:8], G_5[7:0]	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[5]	SDIN4-right (Ch8) H to input mixer 5 coefficient (default = 0) u[31:28], H_5[27:24], H_5[23:16], H_5[15:8], H_5[7:0]	0x00, 0x00, 0x00, 0x00

Table 7-14. Channel 1–8 Input Mixer Register Format (continued)

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x46	32	A_to_ipmix[6]	SDIN1-left (Ch1) A to input mixer 6 coefficient (default = 0) u[31:28], A_6[27:24], A_6[23:16], A_6[15:8], A_6[7:0]	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[6]	SDIN1-right (Ch2) B to input mixer 6 coefficient (default = 0) u[31:28], B_6[27:24], B_6[23:16], B_6[15:8], B_6[7:0]	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[6]	SDIN2-left (Ch3) C to input mixer 6 coefficient (default = 0) u[31:28], C_6[27:24], C_6[23:16], C_6[15:8], C_6[7:0]	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[6]	SDIN2-right (Ch4) D to input mixer 6 coefficient (default = 0) u[31:28], D_6[27:24], D_6[23:16], D_6[15:8], D_6[7:0]	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[6]	SDIN3-left (Ch5) E to input mixer 6 coefficient (default = 0) u[31:28], E_6[27:24], E_6[23:16], E_6[15:8], E_6[7:0]	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[6]	**SDIN3-right (Ch6) F to input mixer 6 coefficient (default = 1) u[31:28], F_6[27:24], F_6[23:16], F_6[15:8], F_6[7:0]**	**0x00, 0x80, 0x00, 0x00**
		G_to_ipmix[6]	SDIN4-left (Ch7) G to input mixer 6 coefficient (default = 0) u[31:28], G_6[27:24], G_6[23:16], G_6[15:8], G_6[7:0]	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[6]	SDIN4-right (Ch8) H to input mixer 6 coefficient (default = 0) u[31:28], H_6[27:24], H_6[23:16], H_6[15:8], H_6[7:0]	0x00, 0x00, 0x00, 0x00
0x47	32	A_to_ipmix[7]	SDIN1-left (Ch1) A to input mixer 7 coefficient (default = 0) u[31:28], A_7[27:24], A_7[23:16], A_7[15:8], A_7[7:0]	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[7]	SDIN1-right (Ch2) B to input mixer 7 coefficient (default = 0) u[31:28], B_7[27:24], B_7[23:16], B_7[15:8], B_7[7:0]	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[7]	SDIN2-left (Ch3) C to input mixer 7 coefficient (default = 0) u[31:28], C_7[27:24], C_7[23:16], C_7[15:8], C_7[7:0]	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[7]	SDIN2-right (Ch4) D to input mixer 7 coefficient (default = 0) u[31:28], D_7[27:24], D_7[23:16], D_7[15:8], D_7[7:0]	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[7]	SDIN3-left (Ch5) E to input mixer 7 coefficient (default = 0) u[31:28], E_7[27:24], E_7[23:16], E_7[15:8], E_7[7:0]	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[7]	SDIN3-right (Ch6) F to input mixer 7 coefficient (default = 0) u[31:28], F_7[27:24], F_7[23:16], F_7[15:8], F_7[7:0]	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[7]	**SDIN4-left (Ch7) G to input mixer 7 coefficient (default = 1) u[31:28], G_7[27:24], G_7[23:16], G_7[15:8], G_7[7:0]**	**0x00, 0x80, 0x00, 0x00**
		H_to_ipmix[7]	SDIN4-right (Ch8) H to input mixer 7 coefficient (default = 0) u[31:28], H_7[27:24], H_7[23:16], H_7[15:8], H_7[7:0]	0x00, 0x00, 0x00, 0x00
0x48	32	A_to_ipmix[8]	SDIN1-left (Ch1) A to input mixer 8 coefficient (default = 0) u[31:28], A_8[27:24], A_8[23:16], A_8[15:8], A_8[7:0]	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[8]	SDIN1-right (Ch2) B to input mixer 8 coefficient (default = 0) u[31:28], B_8[27:24], B_8[23:16], B_8[15:8], B_8[7:0]	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[8]	SDIN2-left (Ch3) C to input mixer 8 coefficient (default = 0) u[31:28], C_8[27:24], C_8[23:16], C_8[15:8], C_8[7:0]	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[8]	SDIN2-right (Ch4) D to input mixer 8 coefficient (default = 0) u[31:28], D_8[27:24], D_8[23:16], D_8[15:8], D_8[7:0]	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[8]	SDIN3-left (Ch5) E to input mixer 8 coefficient (default = 0) u[31:28], E_8[27:24], E_8[23:16], E_8[15:8], E_8[7:0]	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[8]	SDIN3-right (Ch6) F to input mixer 8 coefficient (default = 0) u[31:28], F_8[27:24], F_8[23:16], F_8[15:8], F_8[7:0]	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[8]	SDIN4-left (Ch7) G to input mixer 8 coefficient (default = 0) u[31:28], G_8[27:24], G_8[23:16], G_8[15:8], G_8[7:0]	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[8]	**SDIN4-right (Ch8) H to input mixer 8 coefficient (default = 1) u[31:28], H_8[27:24], H_8[23:16], H_8[15:8], H_8[7:0]**	**0x00, 0x80, 0x00, 0x00**

Not Recommended For New Designs

7.15 Bass Management Registers (0x49–0x50)

Registers 0x49–0x50 provide configuration control for bass mangement.

Each gain coefficient is in 28-bit (5.23) format, so 0x80 0000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used.

Table 7-15. Bass Management Register Format

SUB-ADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x49	4	ipmix_1_to_ch8	Input mixer 1 to Ch8 mixer coefficient (default = 0) u[31:28], ipmix18[27:24], ipmix18[23:16], ipmix18[15:8], ipmix18[7:0]	0x00, 0x00, 0x00, 0x00
0x4A	4	ipmix_2_to_ch8	Input mixer 2 to Ch8 mixer coefficient (default = 0) u[31:28], ipmix28[27:24], ipmix28[23:16], ipmix28[15:8], ipmix28[7:0]	0x00, 0x00, 0x00, 0x00
0x4B	4	ipmix_7_to_ch12	Input mixer 7 to Ch1 and Ch2 mixer coefficient (default = 0) u[31:28], ipmix72[27:24], ipmix72[23:16], ipmix72[15:8], ipmix72[7:0]	0x00, 0x00, 0x00, 0x00
0x4C	4	Ch7_bp_bq2	Ch7 biquad-2 bypass coefficient (default = 0) u[31:28], ch7_bp_bq2[27:24], ch7_bp_bq2[23:16], ch7_bp_bq2[15:8], ch7_bp_bq2[7:0]	0x00, 0x00, 0x00, 0x00
0x4D	4	Ch7_bq2	Ch7 biquad-2 inline coefficient (default = 1) u[31:28], ch6_bq2[27:24], ch6_bq2[23:16], ch6_bq2[15:8], ch6_bq2[7:0]	0x00, 0x80, 0x00, 0x00
0x4E	4	ipmix_8_to_ch12	Ch8 biquad-2 output to Ch1 mixer and Ch2 mixer coefficient (default = 0) u[31:28], ipmix8_12[27:24], ipmix8_12[23:16], ipmix8_12[15:8], ipmix8_12[7:0]	0x00, 0x00, 0x00, 0x00
0x4F	4	Ch8_bp_bq2	Ch8 biquad-2 bypass coefficient (default = 0) u[31:28], ch8_bp_bq2[27:24], ch8_bp_bq2[23:16], ch8_bp_bq2[15:8], ch8_bp_bq2[7:0]	0x00, 0x00, 0x00, 0x00
0x50	4	Ch8_bq2	Ch8 biquad-2 inline coefficient (default = 1) u[31:28], ch7_bq2[27:24], ch7_bq2[23:16], ch7_bq2[15:8], ch7_bq2[7:0]	0x00, 0x80, 0x00, 0x00

7.16 Biquad Filter Register (0x51–0x88)

Table 7-16. Biquad Filter Register Format

I^2C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x51–0x57	20/reg.	Ch1_bq[1:7]	Ch1 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17
0x58–0x5E	20/reg.	Ch2_bq[1:7]	Ch2 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17
0x5F–0x65	20/reg.	Ch3_bq[1:7]	Ch3 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17
0x66–0x6C	20/reg.	Ch4_bq[1:7]	Ch4 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17
0x6D–0x73	20/reg.	Ch5_bq[1:7]	Ch5 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17
0x74–0x7A	20/reg.	Ch6_bq[1:7]	Ch6 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17
0x7B–0x81	20/reg.	Ch7_bq[1:7]	Ch7 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17
0x82–0x88	20/reg.	Ch8_bq[1:7]	Ch8 biquads 1–7. See Table 7-17 for bit definition.	See Table 7-17

Each gain coefficient is in 28-bit (5.23) format, so 0x80 0000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used.

Table 7-17. Contents of One 20-Byte Biquad Filter Register (Default = All-Pass)

DESCRIPTION	REGISTER FIELD CONTENTS	DEFAULT GAIN COEFFICIENT VALUES	
		DECIMAL	HEX
b_0 coefficient	**u[31:28], b0[27:24], b0[23:16], b0[15:8], b0[7:0]**	**1.0**	**0x00, 0x80, 0x00, 0x00**
b_1 coefficient	u[31:28], b1[27:24], b1[23:16], b1[15:8], b1[7:0]	0.0	0x00, 0x00, 0x00, 0x00
b_2 coefficient	u[31:28], b2[27:24], b2[23:16], b2[15:8], b2[7:0]	0.0	0x00, 0x00, 0x00, 0x00
a_1 coefficient	u[31:28], a1[27:24], a1[23:16], a1[15:8], a1[7:0]	0.0	0x00, 0x00, 0x00, 0x00
a_2 coefficient	u[31:28], a2[27:24], a2[23:16], a2[15:8], a2[7:0]	0.0	0x00, 0x00, 0x00, 0x00

7.17 Bass and Treble Bypass Register, Channels 1–8 (0x89–0x90)

Channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0x89, 0x8A, 0x8B, 0x8C, 0x8D, 0x8E, 0x8F, and 0x90, respectively. Eight bytes are written for each channel. Each gain coefficient is in 28-bit (5.23) format, so 0x80 0000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used.

Table 7-18. Channel 1–8 Bass and Treble Bypass Register Format

REGISTER NAME	TOTAL BYTES	CONTENTS	DEFAULT VALUE
Channel bass and treble bypass	8	u[31:28], bypass[27:24], bypass[23:16], bypass[15:8], bypass[7:0]	0x00, 0x80, 0x00, 0x00
Channel bass and treble inline		u[31:28], inline[27:24], inline[23:16], inline[15:8], inline[7:0]	0x00, 0x00, 0x00, 0x00

7.18 Loudness Registers (0x91–0x95)

Table 7-19. Loudness Register Format

I^2C SUB-ADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x91	4	Loudness Log2 gain (LG)	u[31:28], LG[27:24], LG[23:16], LG[15:8], LG[7:0]	0xFF, 0xC0, 0x00, 0x00
0x92	8	Loudness Log2 offset (LO)	u[31:24], u[23:16], LO[15:8], LO[7:0]	0x00, 0x00, 0x00, 0x00
		Loudness Log2 offset (LO)	LO[31:24], LO[23:16], LO[15:8], LO[7:0]	0x00, 0x00, 0x00, 0x00
0x93	4	Loudness gain (G)	u[31:28], G[27:24], G[23:16], G[15:8], G[7:0]	0x00, 0x00, 0x00, 0x00
0x94	8	Loudness offset upper 16 bits (O)	u[31:24], u[23:16], O[15:8], O[7:0]	0x00, 0x00, 0x00, 0x00
		Loudness offset lower 32 bits (O)	O[31:24], O[23:16], O[15:8], O[7:0]	0x00, 0x00, 0x00, 0x00
0x95	20	Loudness biquad (b_0)	u[31:28], b0[27:24], b0[23:16], b0[15:8], b0[7:0]	0x00, 0x00, 0xD5, 0x13
		Loudness biquad (b_1)	u[31:28], b1[27:24], b1[23:16], b1[15:8], b1[7:0]	0x00, 0x00, 0x00, 0x00
		Loudness biquad (b_2)	u[31:28], b2[27:24], b2[23:16], b2[15:8], b2[7:0]	0x0F, 0xFF, 0x2A, 0xED
		Loudness biquad (a_1)	u[31:28], a1[27:24], a1[23:16], a1[15:8], a1[7:0]	0x00, 0xFE, 0x50, 0x45
		Loudness biquad (a_2)	u[31:28], a2[27:24], a2[23:16], a2[15:8], a2[7:0]	0x0F, 0x81, 0xAA, 0x27

Not Recommended For New Designs

7.19 DRC1 Control Registers, Channels 1–7 (0x96)

Bits D31–D14 are *don't care*. Note that there must be a 10-ms delay between a write to register 0x96 and a write to register 0x97.

Table 7-20. Channel 1–7 DCR1 Control Register Format

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
								Unused bits
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
		0	**0**	–	–	–	–	**Channel 7 (node j): No DRC**
		0	1	–	–	–	–	Channel 7 (node j): Pre-volume DRC
		1	0	–	–	–	–	Channel 7 (node j): Post-volume DRC
		1	1	–	–	–	–	Channel 7 (node j): No DRC
		–	–	**0**	**0**	–	–	**Channel 6 (node I): No DRC**
		–	–	0	1	–	–	Channel 6 (node I): Pre-volume DRC
		–	–	1	0	–	–	Channel 6 (node I): Post-volume DRC
		–	–	1	1	–	–	Channel 6 (node i): No DRC
		–	–	–	–	**0**	**0**	**Channel 5 (node m): No DRC**
		–	–	–	–	0	1	Channel 5 (node m): Pre-volume DRC
		–	–	–	–	1	0	Channel 5 (node m): Post-volume DRC
		–	–	–	–	1	1	Channel 5 (node m): No DRC
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	–	–	–	–	–	–	**Channel 4 (node n): No DRC**
0	1	–	–	–	–	–	–	Channel 4 (node n): Pre-volume DRC
1	0	–	–	–	–	–	–	Channel 4 (node n): Post-volume DRC
1	1	–	–	–	–	–	–	Channel 4 (node n): No DRC
–	–	**0**	**0**	–	–	–	–	**Channel 3 (node o): No DRC**
–	–	0	1	–	–	–	–	Channel 3 (node o): Pre-volume DRC
–	–	1	0	–	–	–	–	Channel 3 (node o): Post-volume DRC
–	–	1	1	–	–	–	–	Channel 3 (node o): No DRC
–	–	–	–	**0**	**0**	–	–	**Channel 2 (node p): No DRC**
–	–	–	–	0	1	–	–	Channel 2 (node p): Pre-volume DRC
–	–	–	–	1	0	–	–	Channel 2 (node p): Post-volume DRC
–	–	–	–	1	1	–	–	Channel 2 (node p): No DRC
–	–	–	–	–	–	**0**	**0**	**Channel 1 (node q): No DRC**
–	–	–	–	–	–	0	1	Channel 1 (node q): Pre-volume DRC
–	–	–	–	–	–	1	0	Channel 1 (node q): Post-volume DRC
–	–	–	–	–	–	1	1	Channel 1 (node q): No DRC

Not Recommended For New Designs

7.20 DRC2 Control Register, Channel 8 (0x97)

Note that there must be a 10-ms delay between a write to register 0x96 and a write to register 0x97.

Table 7-21. Channel-8 DRC2 Control Register Format

D31–D2		D1	D0	FUNCTION
0	**0**	**0**	**0**	**Channel 8 (node r): no DRC**
0	0	0	1	Channel 8 (node r): pre-volume DRC
0	0	1	0	Channel 8 (node r): post-volume DRC
0	0	1	1	Channel 8 (node r): no DRC

7.21 DRC1 Data Registers (0x98–0x9C)

DRC1 applies to channels 1, 2, 3, 4, 5, 6, and 7.

Table 7-22. DRC1 Data Register Format

I^2C SUB-ADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x98	8	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 energy	u[31:28], E[27:24], E[23:16], E[15:8], E[7:0]	0x00, 0x00, 0x88, 0x3F
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 (1 – energy)	u[31:28], 1–E[27:24], 1–E[23:16], 1–E[15:8], 1–E[7:0]	0x00, 0x7F, 0x77, 0xC0
0x99	16	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 threshold upper 16 bits (T1)	u[31:24], u[23:16], T1[15:8], T1[7:0]	0x00, 0x00, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 threshold lower 32 bits (T1)	T1[31:24], T1[23:16], T1[15:8], T1[7:0]	0x0B, 0x20, 0xE2, 0xB2
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 threshold upper 16 bits (T2)	u[31:24], u[23:16], T2[15:8], T2[7:0]	0x00, 0x00, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 threshold lower 32 bits (T2)	T2[31:24], T2[23:16], T2[15:8], T2[7:0]	0x06, 0xF9, 0xDE, 0x58
0x9A	12	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 slope (k0)	u[31:28], k0[27:24], k0[23:16], k0[15:8], k0[7:0]	0x00, 0x40, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 slope (k1)	u[31:28], k1[27:24], k1[23:16], k1[15:8], k1[7:0]	0x0F, 0xC0, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 slope (k2)	u[31:28], k2[27:24], k2[23:16], k2[15:8], k2[7:0]	0x0F, 0x90, 0x00, 0x00
0x9B	16	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 offset-1 upper 16 bits (O1)	u[31:24], u[23:16], O1[15:8], O1[7:0]	0x00, 0x00, 0xFF, 0xFF
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 offset-1 lower 32 bits (O1)	O1[31:24], O1[23:16], O1[15:8], O1[7:0]	0xFF, 0x82, 0x30, 0x98
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 offset-2 upper 16 bits (O2)	u[31:24], u[23:16], O2[15:8], O2[7:0]	0x00, 0x00, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 offset-2 lower 32 bits (O2)	O2[31:24], O2[23:16], O2[15:8], O2[7:0]	0x01, 0x95, 0xB2, 0xC0
0x9C	16	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 attack	u[31:28], A[27:24], A[23:16], A[15:8], A[7:0]	0x00, 0x00, 0x88, 0x3F
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 (1 – attack)	u[31:28], 1–A[27:24], 1–A[23:16], 1–A[15:8], 1–A[7:0]	0x00, 0x7F, 0x77, 0xC0
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 decay	u[31:28], D[27:24], D[23:16], D[15:8], D[7:0]	0x00, 0x00, 0x00, 0x56
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 (1 – decay)	u[31:28], 1–D[27:24], 1–D[23:16], 1–D[15:8], 1–D[7:0]	0x00, 0x3F, 0xFF, 0xA8

7.22 DRC2 Data Registers (0x9D–0xA1)

DRC2 applies to channel 8.

Table 7-23. DRC2 Data Register Format

I²C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x9D	8	Channel 8 DRC2 energy	u[31:28], E[27:24], E[23:16], E[15:8], E[7:0]	0x00, 0x00, 0x88, 0x3F
		Channel 8 DRC2 (1 – energy)	u[31:28], 1–E[27:24], 1–E[23:16], 1–E[15:8], 1–E[7:0]	0x00, 0x7F, 0x77, 0xC0
0x9E	16	Channel 8 DRC2 threshold upper 16 bits (T1)	u[31:24], u[23:16], T1[15:8], T1[7:0]	0x00, 0x00, 0x00, 0x00
		Channel 8 DRC2 threshold lower 32 bits (T1)	T1[31:24], T1[23:16], T1[15:8], T1[7:0]	0x0B, 0x20, 0xE2, 0xB2
		Channel 8 DRC2 threshold upper 16 bits (T2)	u[31:24], u[23:16], T2[15:8], T2[7:0]	0x00, 0x00, 0x00, 0x00
		Channel 8 DRC2 threshold lower 32 bits (T2)	T2[31:24], T2[23:16], T2[15:8], T2[7:0]	0x06, 0xF9, 0xDE, 0x58
0x9F	12	Channel 8 DRC2 slope (k0)	u[31:28], k0[27:24], k0[23:16], k0[15:8], k0[7:0]	0x00, 0x40, 0x00, 0x00
		Channel 8 DRC2 slope (k1)	u[31:28], k1[27:24], k1[23:16], k1[15:8], k1[7:0]	0x0F, 0xC0, 0x00, 0x00
		Channel 8 DRC2 slope (k2)	u[31:28], k2[27:24], k2[23:16], k2[15:8], k2[7:0]	0x0F, 0x90, 0x00, 0x00
0xA0	16	Channel 8 DRC2 offset 1 upper 16 bits (O1)	u[31:24], u[23:16], O1[15:8], O1[7:0]	0x00, 0x00, 0xFF, 0xFF
		Channel 8 DRC2 offset 1 lower 32 bits (O1)	O1[31:24], O1[23:16], O1[15:8], O1[7:0]	0xFF, 0x82, 0x30, 0x98
		Channel 8 DRC2 offset 2 upper 16 bits (O2)	u[31:24], u[23:16], O2[15:8], O2[7:0]	0x00, 0x00, 0x00, 0x00
		Channel 8 DRC2 offset 2 lower 32 bits (O2)	O2[31:24], O2[23:16], O2[15:8], O2[7:0]	0x01, 0x95, 0xB2, 0xC0
0xA1	16	Channel 8 DRC2 attack	u[31:28], A[27:24], A[23:16], A[15:8], A[7:0]	0x00, 0x00, 0x88, 0x3F
		Channel 8 DRC2 (1 – attack)	u[31:28], 1–A[27:24], 1–A[23:16], 1–A[15:8], 1–A[7:0]	0x00, 0x7F, 0x77, 0xC0
		Channel 8 DRC2 decay	u[31:28], D[27:24], D[23:16], D[15:8], D[7:0]	0x00, 0x00, 0x00, 0x56
		Channel 8 DRC2 (1 – decay)	u[31:28], 1–D[27:24], 1–D[23:16], 1–D[15:8], 1–D[7:0]	0x00, 0x3F, 0xFF, 0xA8

7.23 DRC Bypass Registers (0xA2–0xA9)

DRC bypass/inline for channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0xA2, 0xA3, 0xA4, 0xA5, 0xA6, 0xA7, 0xA8, and 0xA9, respectively. Eight bytes are written for each channel. Each gain coefficient is in 28-bit (5.23) format, so 0x0080 0000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper 4 bits not used.

To enable DRC for a given channel (with unity gain), bypass = 0x0000 0000 and inline = 0x0080 0000.

To disable DRC for a given channel, bypass = 0x0080 0000 and inline = 0x0000 0000.

Table 7-24. DRC Bypass Register Format

REGISTER NAME	TOTAL BYTES	CONTENTS	DEFAULT VALUE
Channel bass DRC bypass	8	u[31:28], bypass[27:24], bypass[23:16], bypass[15:8], bypass[7:0]	0x00, 0x80, 0x00, 0x00
Channel DRC inline		u[31:28], inline[27:24], inline[23:16], inline[15:8], inline[7:0]	0x00, 0x00, 0x00, 0x00

7.24 8×2 Output Mixer Registers (0xAA–0xAF)

The pass-through output mixer setting is:

- DAP channel 1 is mapped though the 8×2 crossbar mixer (0xAA) to PWM channel 1
- DAP channel 2 is mapped though the 8×2 crossbar mixer (0xAB) to PWM channel 2
- DAP channel 3 is mapped though the 8×2 crossbar mixer (0xAC) to PWM channel 3
- DAP channel 4 is mapped though the 8×2 crossbar mixer (0xAD) to PWM channel 4
- DAP channel 5 is mapped though the 8×2 crossbar mixer (0xAE) to PWM channel 5

- DAP channel 6 is mapped though the 8×2 crossbar mixer (0xAF) to PWM channel 6

Note that the pass-through output mixer configuration (0xD0 bit 30 = 1) is recommended. Using the remapped output mixer configuration (0xD0 bit 30 = 0) increases the complexity of using some features such as volume and mute. See *TAS5518C Errata* (SLEZ006).

Total data per register is 8 bytes. The default gain for each selected channel is 1 (0x0 80 00 00).

Table 7-25. Output Mixer Register Format (Upper 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

Table 7-26. Output Mixer Register Format (Lower 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

7.25 8×3 Output Mixer Registers (0xB0–0xB1)

The pass-through output mixer setting is:

- DAP channel 7 is mapped though the 8×3 crossbar mixer (0xB0) to PWM channel 7
- DAP channel 8 is mapped though the 8×3 crossbar mixer (0xB1) to PWM channel 8

Note that the default setting is recommended for most systems. Any variation from this setting increases the complexity of using some features such as volume and mute. See *TAS5518C Errata* (SLEZ006).

Total data per register is 12 bytes. The default gain for each selected channel is 1 (0x0080 0000).

Table 7-27. Output Mixer Register Format (Upper 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

Table 7-28. Output Mixer Register Format (Middle 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

Table 7-29. Output Mixer Register Format (Lower 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer

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Table 7-29. Output Mixer Register Format (Lower 4 Bytes) (continued)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

7.26 PSVC Volume Biquad Register (0xCF)

Each gain coefficient is in 28-bit (5.23) format, so 0x80 0000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used. Note that this register should be used only with the PSVC feature its use is not required. For systems not using this feature, it is recommended that this biquad be set to all-pass (default).

Table 7-30. Volume Biquad Register Format (Default = All-Pass)

DESCRIPTION	REGISTER FIELD CONTENTS	DEFAULT GAIN COEFFICIENT VALUES	
		DECIMAL	HEX
b_0 coefficient	u[31:28], b0[27:24], b0[23:16], b0[15:8], b0[7:0]	1.0	0x00, 0x80, 0x00, 0x00
b_1 coefficient	u[31:28], b1[27:24], b1[23:16], b1[15:8], b1[7:0]	0.0	0x00, 0x00, 0x00, 0x00
b_2 coefficient	u[31:28], b2[27:24], b2[23:16], b2[15:8], b2[7:0]	0.0	0x00, 0x00, 0x00, 0x00
a_1 coefficient	u[31:28], a1[27:24], a1[23:16], a1[15:8], a1[7:0]	0.0	0x00, 0x00, 0x00, 0x00
a_2 coefficient	u[31:28], a2[27:24], a2[23:16], a2[15:8], a2[7:0]	0.0	0x00, 0x00, 0x00, 0x00

7.27 Volume, Treble, and Bass Slew Rates Register (0xD0)

Table 7-31. Volume Gain Update Rate (Slew Rate)

D31–D10	D9	D8	FUNCTION
0	0	0	512 step update at 4 Fs, 42.6 ms at 48 kHz
0	**0**	**1**	**1024 step update at 4 Fs, 85.3 ms at 48 kHz**
0	1	0	2048 step update at 4 Fs, 170 ms at 48 kHz
0	1	1	2048 step update at 4 Fs, 170 ms at 48 kHz

Table 7-32. Treble and Bass Gain Step Size (Slew Rate)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No operation
0	0	0	0	0	1	0	0	Minimum rate – Updates every 0.083 ms (every LRCLK at 48 kHz)
0	0	1	0	0	0	0	0	Updates every 0.67 ms (32 LRCLKs at 48 kHz)
0	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**Default rate - Updates every 1.31 ms (63 LRCLKs at 48 kHz). This is the maximum constant time that can be set for all sample rates.**
1	1	1	1	1	1	1	1	Maximum rate – Updates every 5.08 ms (every 255 LRCLKs at 48 kHz)

7.28 Volume Registers (0xD1–0xD9)

Channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0xD1, 0xD2, 0xD3, 0xD4, 0xD5, 0xD6, 0xD7, and 0xD8, respectively. The default volume for all channels is 0 dB.

Master volume is mapped into register 0xD9. The default for the master volume is mute.

Bits D31–D12 are *don't care*.

Table 7-33. Volume Register Format

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
								Unused bits
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
				V11	V10	V9	V8	Volume
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
V7	V6	V5	V4	V3	V2	V1	V0	Volume

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Table 7-34. Master and Individual Volume Controls

VOLUME INDEX (H)	GAIN/INDEX(dB)
001	17.75
002	17.5
003	17.25
004	17
005	16.75
006	16.5
007	16.25
008	16
009	15.75
00A	15.5
00B	15.25
00C	15
00D	14.75
00E	14.5
00F	14.25
010	14
. . .	. . .
044	1
045	0.75
046	0.5
047	0.25
048	0
049	–0.25
04A	–0.5
04B	–0.75
04C	–1
. . .	. . .
240	–126
241	–126.25
242	–126.5
243	–126.75
244	–127
245	**Mute**
TO	
3FF	**Mute**

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7.29 Bass Filter Set Register (0xDA)

To use the bass and treble function, the bass and treble bypass registers (0x89–0x90) must be configured as inline (default is bypass).

Table 7-35. Channel 8 (Subwoofer)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Reserved
0	0	0	0	0	1	1	1	Reserved

Table 7-36. Channels 6 and 5 (Right and Left Lineout in 6-Channel Configuration; Right and Left Surround in 8-Channel Configuration)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Reserved
0	0	0	0	0	1	1	1	Reserved

Table 7-37. Channels 4 and 3 (Right and Left Rear)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

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Table 7-38. Channels 7, 2, and 1 (Center, Right Front, and Left Front)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

7.30 Bass Filter Index Register (0xDB)

Index values above 0x24 are invalid. To use the bass and treble function, the bass and treble bypass registers (0x89–0x90) must be configured as inline (default is bypass).

Table 7-39. Bass Filter Index Register Format

I^2C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0xDB	4	Bass filter index (BFI)	Ch8_BFI[31:24], Ch65_BFI[23:16], Ch43_BFI[15:8], Ch721_BFI[7:0]	0x12, 0x12, 0x12, 0x12

Table 7-40. Bass Filter Indexes

BASS INDEX VALUE	ADJUSTMENT (dB)	BASS INDEX VALUE	ADJUSTMENT (dB)
0x00	18	0x13	–1
0x01	17	0x14	–2
0x02	16	0x15	–3
0x03	15	0x16	–4
0x04	14	0x17	–5
0x05	13	0x18	–6
0x06	12	0x19	–7
0x07	11	0x1A	–8
0x08	10	0x1B	–9
0x09	9	0x1C	–10
0x0A	8	0x1D	–11
0x0B	7	0x1E	–12
0x0C	6	0x1F	–13
0x0D	5	0x20	–14
0x0E	4	0x21	–15
0x0F	3	0x22	–16
0x10	2	0x23	–17
0x11	1	0x24	–18
0x12	**0**		

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7.31 Treble Filter Set Register (0xDC)

Bits D31–D27 are *don't care*. To use the bass and treble function, the bass and treble bypass registers (0x89 - 0x90) must be configured as inline (enabled).

Table 7-41. Channel 8 (Subwoofer)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Bits D23–D19 are *don't care*.

Table 7-42. Channels 6 and 5 (Right and Left Lineout in 6-Channel Configuration; Right and Left Surround in 8-Channel Configuration)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Bits D15–D11 are *don't care*.

Table 7-43. Channels 4 and 3 (Right and Left Rear)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Bits D7–D3 are *don't care*.

Table 7-44. Channels 7, 2, and 1 (Center, Right Front, and Left Front)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

7.32 Treble Filter Index (0xDD)

Index values above 0x24 are invalid. To use the bass and treble function, the bass and treble bypass registers (0x89 - 0x90) must be configured as inline (enabled).

Table 7-45. Treble Filter Index Register Format

I^2C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0xDD	4	Treble filter index (TFI)	Ch8_TFI[31:24], Ch65_TFI[23:16], Ch43_TFI[15:8], Ch721_TFI[7:0]	0x12, 0x12, 0x12, 0x12

Table 7-46. Treble Filter Indexes

TREBLE INDEX VALUE	ADJUSTMENT (dB)	TREBLE INDEX VALUE	ADJUSTMENT (dB)
0x00	18	0x13	–1
0x01	17	0x14	–2
0x02	16	0x15	–3
0x03	15	0x16	–4
0x04	14	0x17	–5
0x05	13	0x18	–6
0x\06	12	0x19	–7
0x07	11	0x1A	–8
0x08	10	0x1B	–9
0x09	9	0x1C	–10
0x0A	8	0x1D	–11
0x0B	7	0x1E	–12
0x0C	6	0x1F	–13
0x0D	5	0x20	–14
0x0E	4	0x21	–15
0x0F	3	0x22	–16
0x10	2	0x23	–17
0x11	1	0x24	–18
0x12	**0**		

7.33 AM Mode Register (0xDE)

Bits D31–D21 are *don't care*.

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Table 7-47. AM Mode Register Format

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
			0	–	–	–	–	**AM mode disabled**
			1	–	–	–	–	AM mode enabled
			–	**0**	**0**	–	–	**Select sequence 1**
			–	0	1	–	–	Select sequence 2
			–	1	0	–	–	Select sequence 3
			–	1	1	–	–	Select sequence 4
			–	–	–	**0**	–	**IF frequency = 455 kHz**
			–	–	–	1	–	IF frequency = 262.5 kHz
			–	–	–	–	**0**	**Use BCD-tuned frequency**
			–	–	–	–	1	Use binary-tuned frequency

Table 7-48. AM Tuned Frequency Register in BCD Mode (Lower 2 Bytes of 0xDE)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	B0	–	–	–	–	BCD frequency (1000s kHz)
–	–	–	–	B3	B2	B1	B0	BCD frequency (100s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
B3	B2	B1	B0	–	–	–	–	BCD frequency (10s kHz)
–	–	–	–	B3	B2	B1	B0	BCD frequency (1s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**

Table 7-49. AM Tuned Frequency Register in Binary Mode (Lower 2 Bytes of 0xDE)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	B10	B9	B8	Binary frequency (upper 3 bits)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
B7	B6	B5	B4	B3	B2	B1	B0	Binary frequency (lower 8 bits)
0	0	0	0	0	0	0	0	Default value

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7.34 PSVC Range Register (0xDF)

Bits D31–D2 are zero.

Table 7-50. PSVC Range Register Format

D31–D2	D1	D0	FUNCTION
0	0	0	12.04-dB control range for PSVC
0	0	1	18.06-dB control range for PSVC
0	**1**	**0**	**24.08-dB control range for PSVC**
0	1	1	Ignore – retain last value

7.35 General Control Register (0xE0)

Bits D31–D4 are zero. Bit D0 is *don't care*.

Table 7-51. General Control Register Format

D31–D4	D3	D2	D1	D0	FUNCTION
0	–	–	**0**		**8-channel configuration**
0	–	–	1		6-channel configuration
0	–	**0**	–		**Power-supply volume control disabled**
0	–	1	–		Power-supply volume control enabled
0	**0**	–	–		**Subwoofer part of PSVC. This bit must always be 0. (D3 is a write-only bit)**

7.36 Incremental Multiple-Byte Write Append Register (0xFE)

This is a special register used to append data to a previously opened register. See *Multiple-Byte Write*, Section 5.4, for programming details.

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8 TAS5518C Example Application Schematic

Figure 8-1 shows an example application schematic for the TAS5518C.

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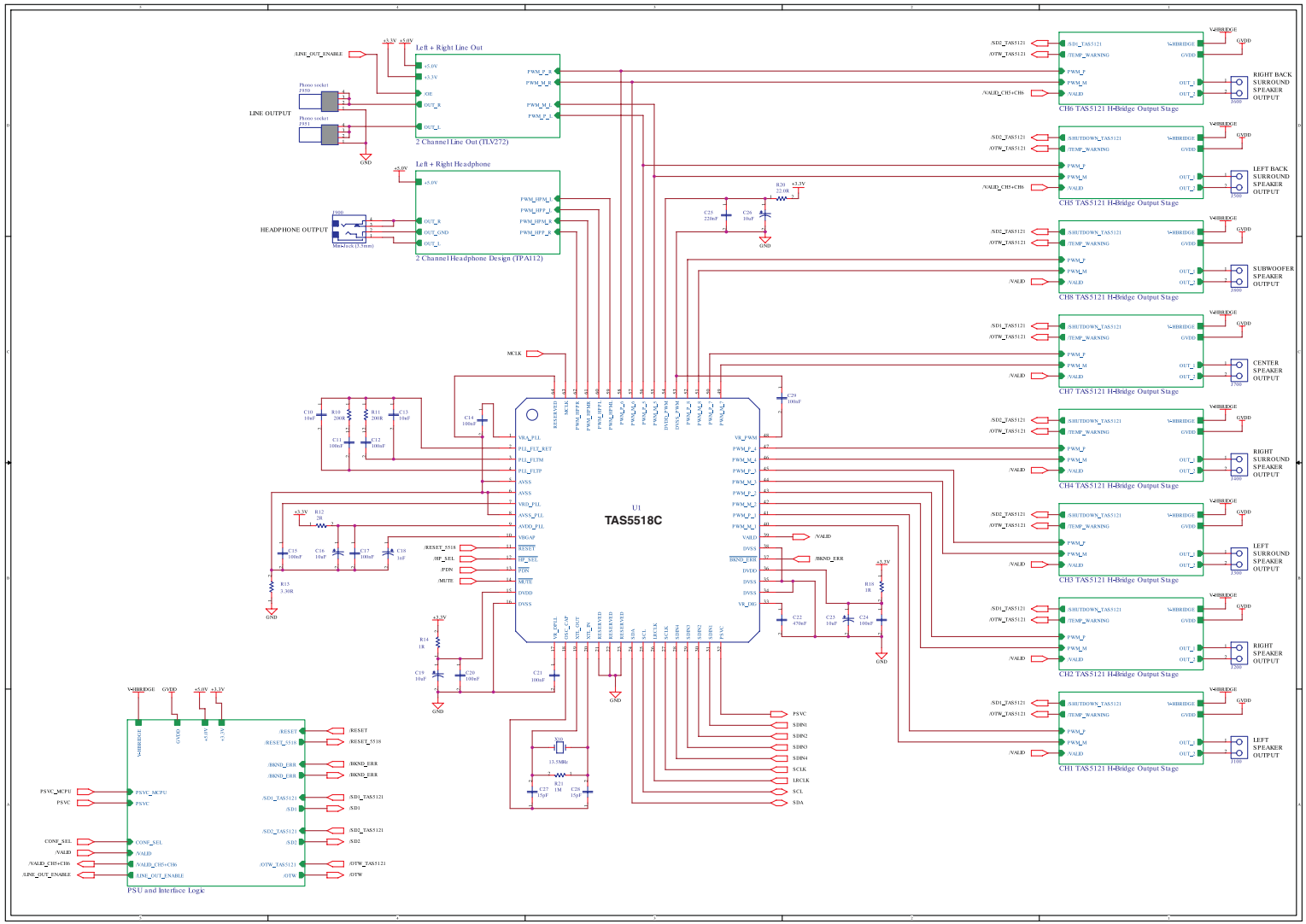

Circuit is subject to change without notice.

Figure 8-1. Example Application Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TAS5518CPAG	NRND	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
TAS5518CPAGR	NRND	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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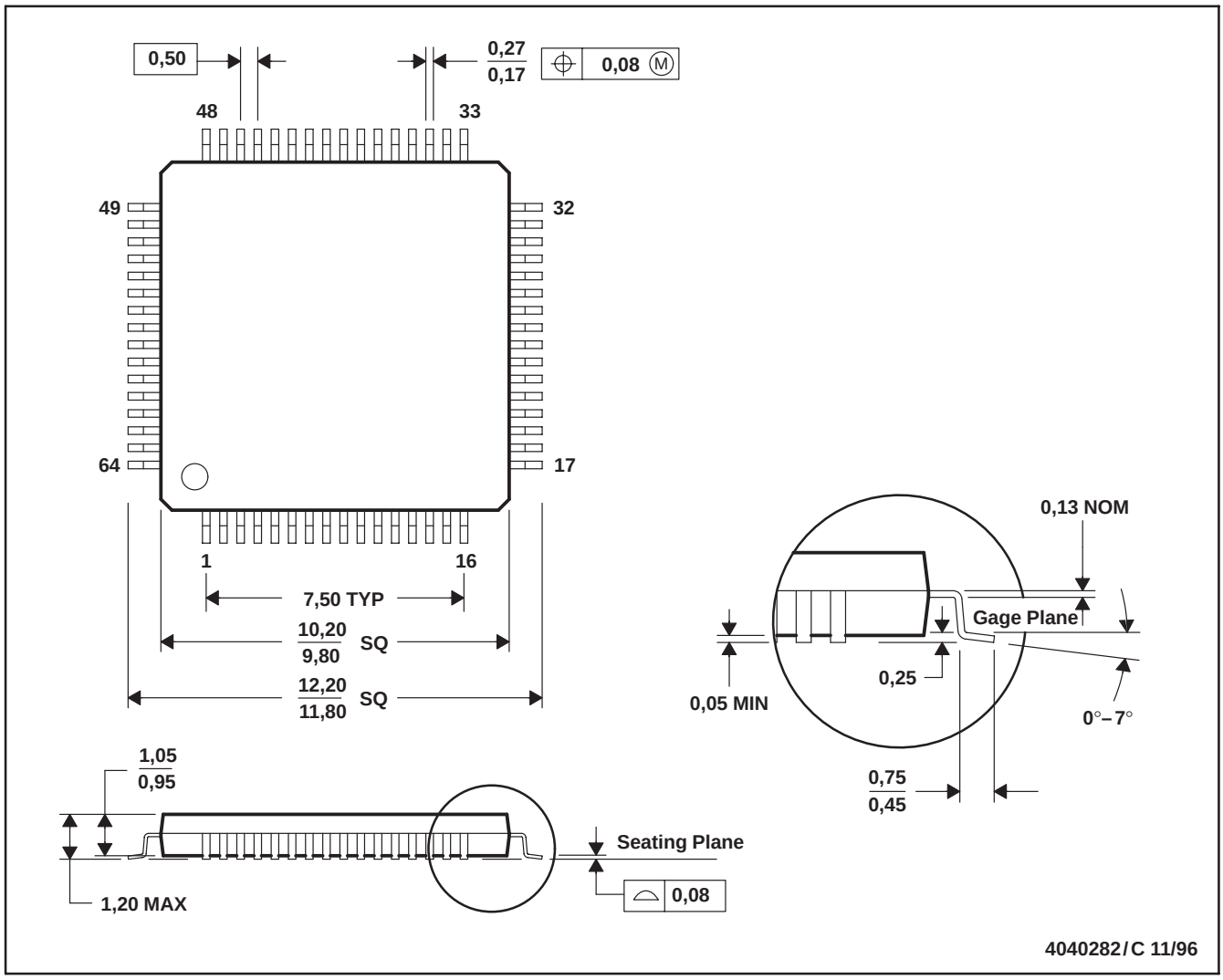
PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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