

## FEATURES

Integrated baluns for single-ended receiver (Rx) inputs and local oscillator (LO) input

Rx channel gain: 22 dB

Noise figure (NF): 10 dB

P1dB: -10 dBm

LO input range: -8 dBm to +5 dBm

Rx to IF isolation: 30 dB

RF signal bandwidth: 250 MHz

Rx output impedance: 900  $\Omega$  differential

LO input buffer: 24 GHz

RF and LO S11 at 50  $\Omega$ : -5 dB

Temperature sensor with analog output:  $\pm 5^\circ$

Electrostatic discharge (ESD) performance

Human body model (HBM): 2000 V

Charged device model (CDM): 500 V

Qualified for automotive applications

## APPLICATIONS

Automotive radars

Industrial radars

Microwave ( $\mu$ W) radar sensors

## GENERAL DESCRIPTION

The ADF5904 is a 4-channel, 24 GHz, receiver downconverter.

Each channel contains a single-ended RF input with an on-chip balun followed by a differential low noise amplifier (LNA) and a downconverter mixer with differential output buffers. The RF LO path also has an on-chip balun.

Control of the on-chip registers is through a simple 3-wire interface.

The ADF5904 comes in a compact 32-lead, 5 mm  $\times$  5 mm LFCSP package.

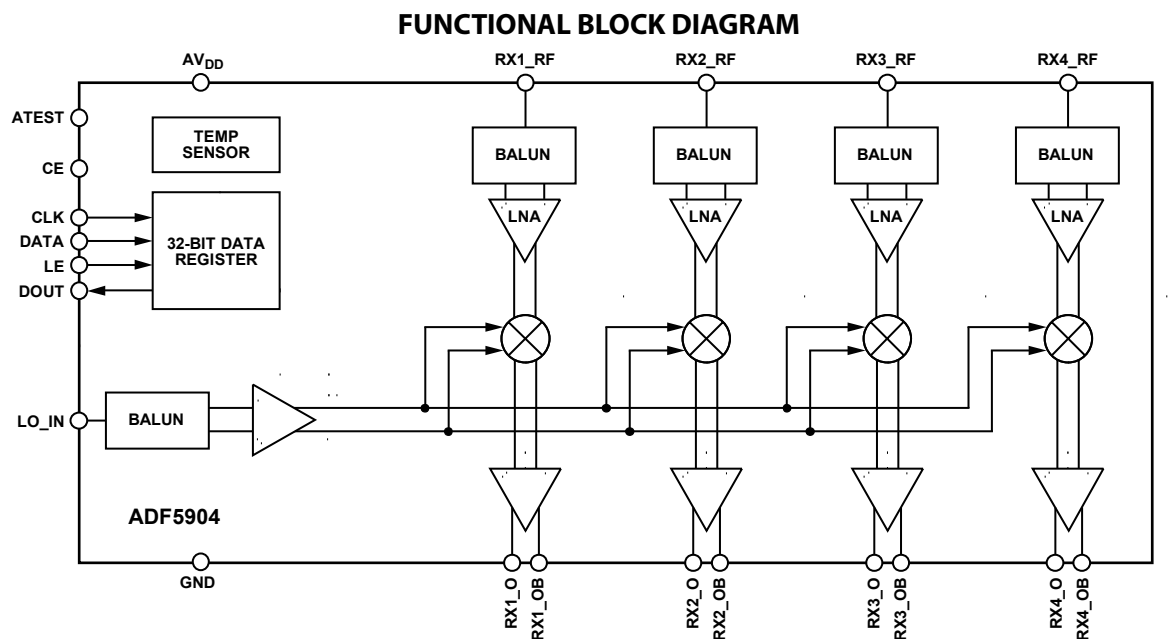


Figure 1.

12885-001

Rev. A

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## REVISION HISTORY

### 2/16—Rev. 0 to Rev. A

|                                            |    |
|--------------------------------------------|----|
| Changes to Features Section .....          | 1  |
| Change to Parameter HBM, Table 3 .....     | 5  |
| Change to Temperature Sensor Section ..... | 13 |
| Changes to Ordering Guide .....            | 15 |

### 3/15—Revision 0: Initial Version

## SPECIFICATIONS

$AV_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $GND = 0 \text{ V}$ , dBm referred to  $50 \Omega$ ,  $T_A = T_{MAX}$  to  $T_{MIN}$ , unless otherwise noted. Operating temperature range is  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ .

Table 1.

| Parameter                                          | Symbol                              | Min                   | Typ                    | Max   | Unit    | Test Conditions/Comments                                                                               |
|----------------------------------------------------|-------------------------------------|-----------------------|------------------------|-------|---------|--------------------------------------------------------------------------------------------------------|
| OPERATING CONDITIONS                               |                                     |                       |                        |       |         |                                                                                                        |
| LO and RF Frequency Range                          |                                     | 24                    |                        | 24.25 | GHz     |                                                                                                        |
| LO INPUT                                           |                                     |                       |                        |       |         |                                                                                                        |
| Input Return Loss (S11)                            |                                     |                       | −5                     |       | dB      |                                                                                                        |
| LO Input Level                                     |                                     | −8                    | −5                     | +5    | dBm     |                                                                                                        |
| BASEBAND OUTPUTS                                   |                                     |                       |                        |       |         |                                                                                                        |
| Voltage Conversion Gain                            |                                     |                       | 22                     |       | dB      | Measured differentially<br>Maximum capacitance = 10 pF                                                 |
| Demodulation Bandwidth                             |                                     |                       | 10                     |       | MHz     |                                                                                                        |
| Output DC Offset (Differential)                    |                                     |                       | ±20                    |       | mV      | Differential 900 Ω load                                                                                |
| Output Common Mode                                 |                                     |                       | AV <sub>DD</sub> − 1.0 |       | V       |                                                                                                        |
| Output Swing                                       |                                     |                       | 2                      |       | V peak  |                                                                                                        |
| Channel to Channel Phase Mismatch over Temperature |                                     |                       | ±5                     |       | Degrees |                                                                                                        |
| DYNAMIC PERFORMANCE, RF = 24.125 GHz               |                                     |                       |                        |       |         |                                                                                                        |
| Conversion Gain                                    |                                     |                       | 22                     |       | dB      | Terminated in 50 Ω                                                                                     |
| Input P1dB                                         |                                     |                       | −10                    |       | dBm     |                                                                                                        |
| RF Input Return Loss                               |                                     |                       | −5                     |       | dB      |                                                                                                        |
| Second-Order Input Intercept                       | IIP2                                |                       | 20                     |       | dBm     |                                                                                                        |
| Third-Order Input Intercept                        | IIP3                                |                       | 0                      |       | dBm     |                                                                                                        |
| LO to RF Isolation                                 |                                     |                       | 30                     |       | dB      |                                                                                                        |
| RF to IF Isolation                                 |                                     |                       | 30                     |       | dB      |                                                                                                        |
| Noise Figure                                       |                                     |                       | 10                     |       | dB      |                                                                                                        |
| Noise Figure Under Blocking Conditions             |                                     |                       | 15                     |       | dB      | Double sideband (DSB) at 100 kHz<br>With a −30 dBm input interferer at 5 MHz offset from carrier (DSB) |
| LOGIC INPUTS                                       |                                     |                       |                        |       |         |                                                                                                        |
| Input Voltage                                      |                                     |                       |                        |       |         |                                                                                                        |
| High                                               | V <sub>IH</sub>                     | 1.4                   |                        |       | V       |                                                                                                        |
| Low                                                | V <sub>IL</sub>                     |                       |                        | 0.6   | V       |                                                                                                        |
| Input Current                                      | I <sub>INH</sub> , I <sub>INL</sub> |                       |                        | ±1    | μA      |                                                                                                        |
| Input Capacitance                                  | C <sub>IN</sub>                     |                       |                        | 10    | pF      |                                                                                                        |
| LOGIC OUTPUTS                                      |                                     |                       |                        |       |         |                                                                                                        |
| Output Voltage                                     |                                     |                       |                        |       |         |                                                                                                        |
| High                                               | V <sub>OH</sub>                     | V <sub>DD</sub> − 0.4 |                        |       | V       | V <sub>DD</sub> selected from the DOUT VSEL bit (Bit DB8, Register 0)                                  |
| Low                                                | V <sub>OL</sub>                     |                       |                        | 0.4   | V       |                                                                                                        |
| Output Current                                     |                                     |                       |                        |       |         |                                                                                                        |
| High                                               | I <sub>OH</sub>                     |                       |                        | 500   | μA      |                                                                                                        |
| Low                                                | I <sub>OL</sub>                     |                       |                        | 500   | μA      |                                                                                                        |
| TEMPERATURE SENSOR                                 |                                     |                       |                        |       |         |                                                                                                        |
| Analog Accuracy                                    |                                     |                       | ±5                     |       | °C      | Following one-point calibration                                                                        |
| Sensitivity                                        |                                     |                       | 4.243                  |       | mV/°C   |                                                                                                        |
| POWER SUPPLIES                                     |                                     |                       |                        |       |         |                                                                                                        |
| AV <sub>DD</sub>                                   |                                     |                       | 170                    |       | mA      |                                                                                                        |
| Power-Down Current                                 |                                     |                       | 100                    |       | μA      |                                                                                                        |

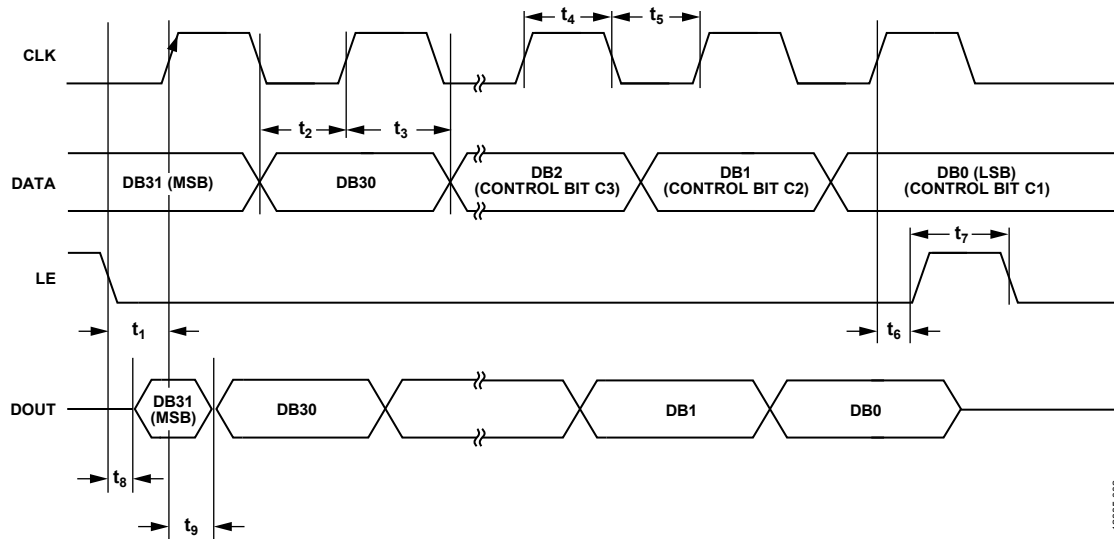
## TIMING CHARACTERISTICS

$AV_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $GND = 0 \text{ V}$ , dBm referred to  $50 \Omega$ ,  $T_A = T_{MAX}$  to  $T_{MIN}$ , unless otherwise noted. Operating temperature range is  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ .

Table 2.

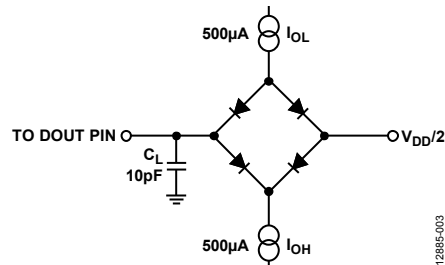
| Parameter | Limit at $T_{MIN}$ to $T_{MAX}$ | Unit   | Description            |
|-----------|---------------------------------|--------|------------------------|
| $t_1$     | 20                              | ns min | LE setup time          |
| $t_2$     | 10                              | ns min | DATA to CLK setup time |
| $t_3$     | 10                              | ns min | DATA to CLK hold time  |
| $t_4$     | 25                              | ns min | CLK high duration      |
| $t_5$     | 25                              | ns min | CLK low duration       |
| $t_6$     | 10                              | ns min | CLK to LE setup time   |
| $t_7$     | 20                              | ns min | LE pulse width         |
| $t_8$     | 10                              | ns max | LE setup time to DOUT  |
| $t_9$     | 15                              | ns max | CLK setup time to DOUT |

## Timing Diagrams



12885-002

Figure 2. Timing Diagram



12885-003

Figure 3. Load Circuit for DOUT Timing,  $C_L = 10 \text{ pF}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

| Parameter                                                   | Rating                      |
|-------------------------------------------------------------|-----------------------------|
| $AV_{DD}$ to GND                                            | –0.3 V to +3.9 V            |
| Digital Input/Output Voltage to GND                         | –0.3 V to $AV_{DD} + 0.3$ V |
| Analog Input/Output Voltage to GND                          | –0.3 V to $AV_{DD} + 0.3$ V |
| $RXx\_RF$ , $LO\_IN$ to GND                                 | –0.3 V to $AV_{DD} + 0.3$ V |
| Operating Temperature Range                                 | –40°C to +105°C             |
| Storage Temperature Range                                   | –65°C to +125°C             |
| Maximum Junction Temperature                                | 150°C                       |
| $\theta_{JA}$ Thermal Impedance <sup>1</sup> (Pad Soldered) | 40.83°C/W                   |
| Reflow Soldering                                            |                             |
| Peak Temperature                                            | 260°C                       |
| Time at Peak Temperature                                    | 40 sec                      |
| Transistor Count                                            |                             |
| CMOS                                                        | 65,100                      |
| Bipolar                                                     | 2280                        |
| ESD                                                         |                             |
| CDM                                                         | 500 V                       |
| HBM                                                         | 2000 V                      |

<sup>1</sup> Two signal planes (that is, on the top and the bottom surfaces of the board), two buried planes, and nine vias.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

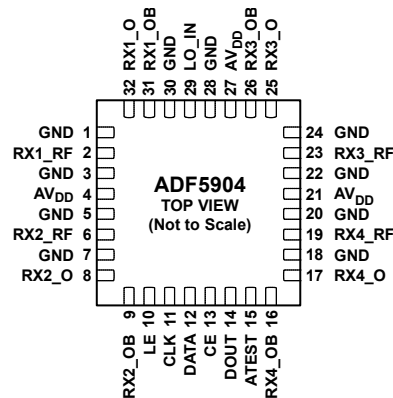
### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE CONNECTED TO GND.

12885-004

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No.                            | Mnemonic         | Description                                                                                                                                                                                      |
|------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 3, 5, 7, 18, 20, 22, 24, 28, 30 | GND              | Ground Pins.                                                                                                                                                                                     |
| 2                                  | RX1_RF           | Channel 1 RF Input.                                                                                                                                                                              |
| 4, 21, 27                          | AV <sub>DD</sub> | Analog Power Supply. The supply range is 3.3 V $\pm$ 5%. Place decoupling capacitors (0.1 $\mu$ F, 1 nF, and 10 pF) to the ground plane as close as possible to this pin.                        |
| 6                                  | RX2_RF           | Channel 2 RF Input.                                                                                                                                                                              |
| 8                                  | RX2_O            | Channel 2 Baseband Output.                                                                                                                                                                       |
| 9                                  | RX2_OB           | Channel 2 Complementary Baseband Output.                                                                                                                                                         |
| 10                                 | LE               | Load Enable, CMOS Input. When LE goes high, data stored in the shift registers is loaded into one of the four latches; the control bits select the latch.                                        |
| 11                                 | CLK              | Serial Clock Input. This serial clock clocks in the serial data to the registers. Data latches into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input. |
| 12                                 | DATA             | Serial Data Input. The serial data loads MSB first and the two LSBs are the control bits. This input is a high impedance CMOS input.                                                             |
| 13                                 | CE               | Chip Enable. A logic low on this pin powers down the device.                                                                                                                                     |
| 14                                 | DOUT             | Serial Data Output.                                                                                                                                                                              |
| 15                                 | ATEST            | Analog Test Output                                                                                                                                                                               |
| 16                                 | RX4_OB           | Channel 4 Complementary Baseband Output.                                                                                                                                                         |
| 17                                 | RX4_O            | Channel 4 Baseband Output.                                                                                                                                                                       |
| 19                                 | RX4_RF           | Channel 4 RF Input.                                                                                                                                                                              |
| 23                                 | RX3_RF           | Channel 3 RF Input.                                                                                                                                                                              |
| 25                                 | RX3_O            | Channel 3 Baseband Output.                                                                                                                                                                       |
| 26                                 | RX3_OB           | Channel 3 Complementary Baseband Output.                                                                                                                                                         |
| 29                                 | LO_IN            | Local Oscillator Input.                                                                                                                                                                          |
| 31                                 | RX1_OB           | Channel 1 Complementary Baseband Output.                                                                                                                                                         |
| 32                                 | RX1_O            | Channel 1 Baseband Output.                                                                                                                                                                       |
|                                    | EPAD             | Exposed Pad. The LFCSP has an exposed pad that must connect to GND.                                                                                                                              |

## TYPICAL PERFORMANCE CHARACTERISTICS

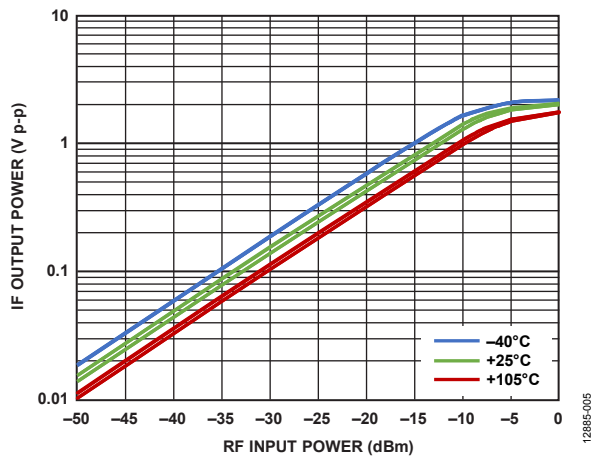


Figure 5. IF Output Power vs. RF Input Power,  
LO Frequency = 24 GHz at -5 dBm and IF Frequency = 100 kHz

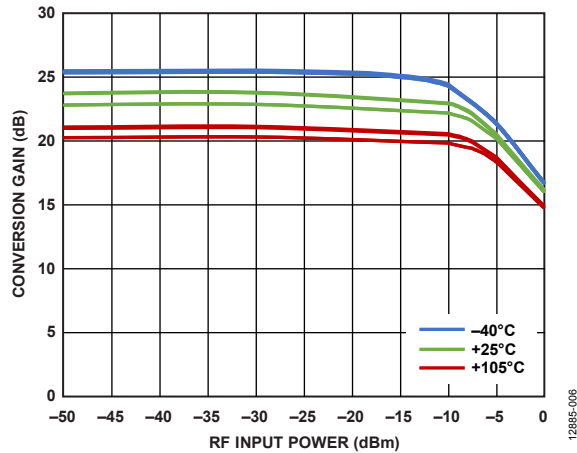


Figure 6. Conversion Gain vs. RF Input Power,  
LO Frequency = 24 GHz at -5 dBm, and IF Frequency = 100 kHz

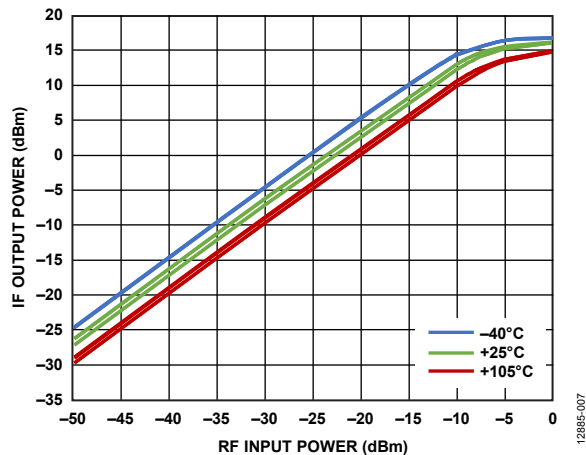


Figure 7. IF Output Power vs. RF Input Power,  
LO Frequency = 24 GHz at -5 dBm, and IF Frequency = 100 kHz

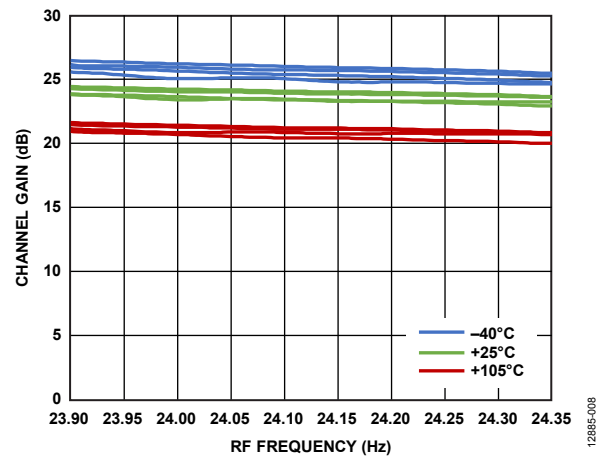


Figure 8. Channel Gain vs. RF Frequency,  
Rx Input = -50 dBm, LO Power = -5 dBm, and IF Frequency = 100 kHz

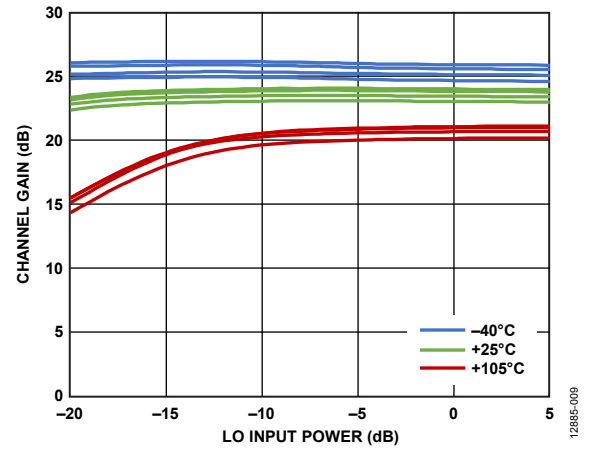


Figure 9. Channel Gain vs. LO Input Power, Rx Input = -50 dBm,  
LO Frequency = 24 GHz, and IF Frequency = 100 kHz

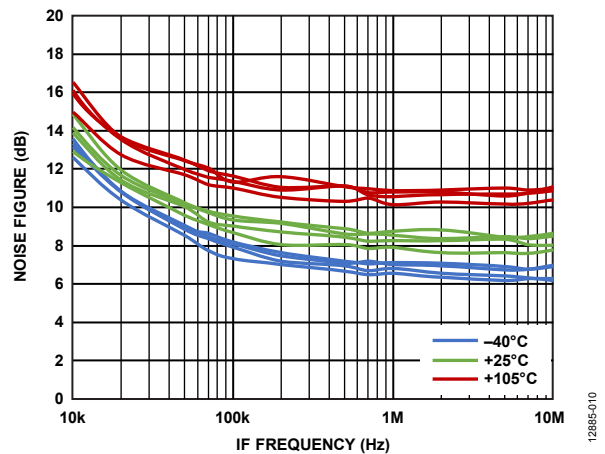


Figure 10. Noise Figure vs. IF Frequency, LO Frequency = 24.125 GHz at -5 dBm

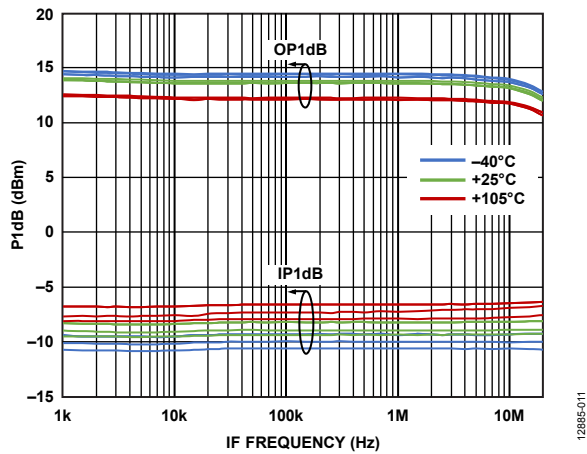


Figure 11. P1dB vs. IF Frequency, LO Frequency = 24 GHz at -5 dBm

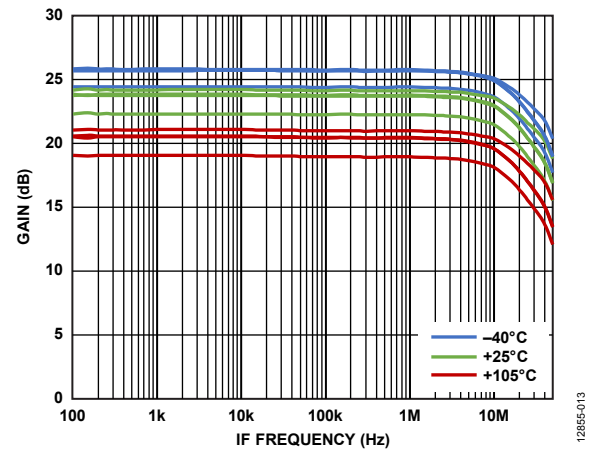


Figure 13. Gain vs. IF Frequency, Rx Power = -50 dBm and LO Frequency = 24 GHz at -5 dBm

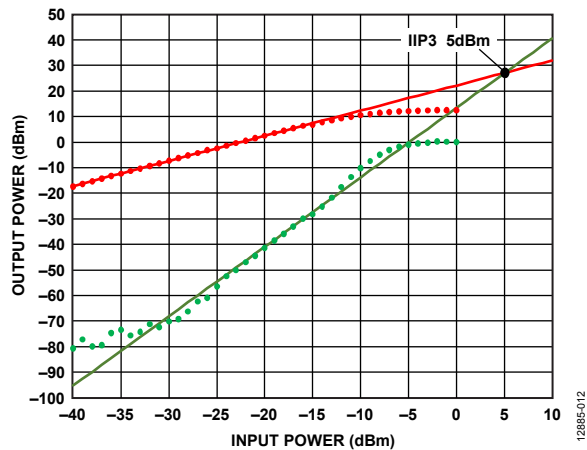


Figure 12. Output Power vs. Input Power, IIP3 LO Frequency = 24.125 GHz at -5 dBm, Rx Frequency = LO + 100 kHz and LO + 200 kHz

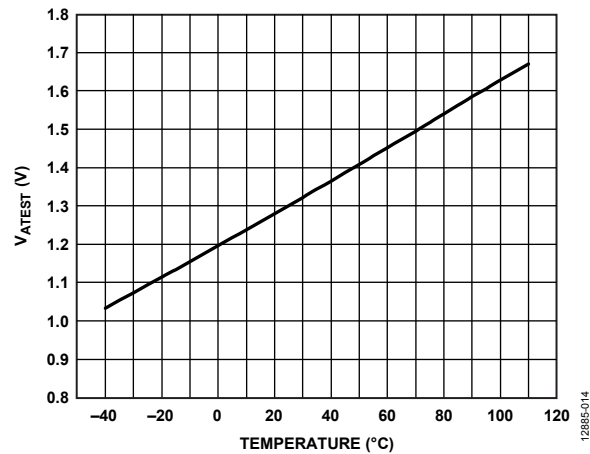


Figure 14. Temperature Sensor Voltage on ATEST

## THEORY OF OPERATION

### RF PATH

The ADF5904 contains four identical 24 GHz downconverter channels. Each channel contains a balun that converts the single-ended input into a differential signal for the rest of the downconverter path (see Figure 15). This balun is followed by a LNA that feeds the downconverter mixer.

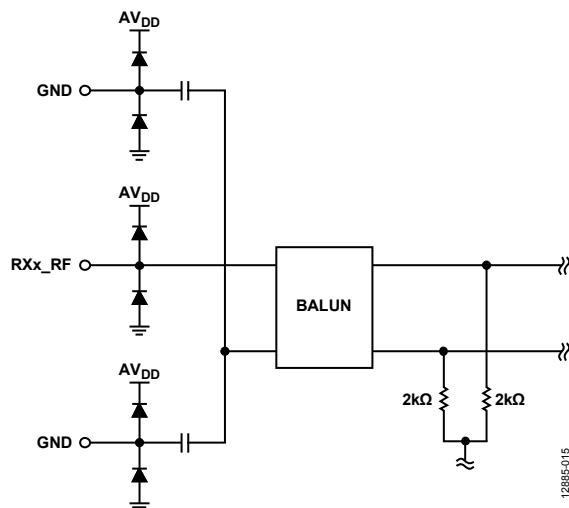


Figure 15. RF Input Stage

### LO PATH

The four downconverter channels share the same LO path. The LO path contains a balun that converts the single-ended input to a differential signal to drive the mixer (see Figure 16).

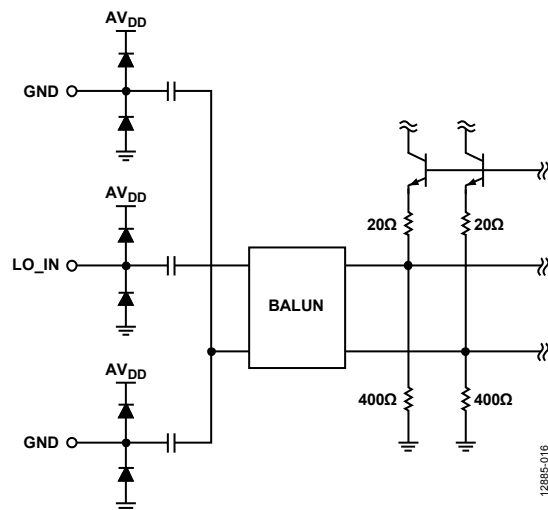


Figure 16. LO Input Stage

### INPUT SHIFT REGISTER

The ADF5904 digital section includes power-down bits and test modes to read back registers. Data is clocked into the 32-bit input shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2 and C1) in the input shift register. These are the two LSBs (DB1 and DB0, respectively), as shown in Table 5. The truth table for these bits is shown in Table 5. Figure 18 to Figure 20 show a summary of how the latches are programmed.

### PROGRAM MODES

Table 5 and Figure 18 through Figure 20 show how to set up the program modes in the ADF5904.

Table 5. C2 and C1 Truth Table

| Control Bits |          | Register |
|--------------|----------|----------|
| C2 (DB1)     | C1 (DB0) |          |
| 0            | 0        | R0       |
| 0            | 1        | R1       |
| 1            | 0        | R2       |
| 1            | 1        | R3       |

## REGISTER MAP

REGISTER 0 (R0)

| RESERVED |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      | PUP CH4 | PUP CH3 | PUP CH2 | PUP CH1 | PUP LO | LO PIN BIAS | DOUT VSEL | RESERVED |     |     |     |     |     | CONTROL BITS |       |       |
|----------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|---------|---------|---------|---------|--------|-------------|-----------|----------|-----|-----|-----|-----|-----|--------------|-------|-------|
| DB31     | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15    | DB14    | DB13    | DB12    | DB11   | DB10        | DB9       | DB8      | DB7 | DB6 | DB5 | DB4 | DB3 | DB2          | DB1   | DB0   |
| 1        | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0       | PC4     | PC3     | PC2     | PC1    | PLO         | LPB       | DIO      | 1   | 0   | 1   | 0   | 0   | 0            | C2(0) | C1(0) |

REGISTER 1 (R1)

| CHANNEL SELECT |      | RESERVED |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |     |     |     |     |     |     |     |     | CONTROL BITS |       |
|----------------|------|----------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|--------------|-------|
| DB31           | DB30 | DB29     | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1          | DB0   |
| CS2            | CS1  | CS0      | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 1    | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 0   | C2(0)        | C1(1) |

REGISTER 2 (R2)

| RESERVED |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      | 5-BIT<br>CHANNEL TEST SELECT |      |      |      |      | RESERVED |     |     |     |     |     |     |     | CONTROL<br>BITS |       |       |
|----------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------------------------------|------|------|------|------|----------|-----|-----|-----|-----|-----|-----|-----|-----------------|-------|-------|
| DB31     | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15                         | DB14 | DB13 | DB12 | DB11 | DB10     | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2             | DB1   | DB0   |
| 0        | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0                            | TC4  | TC3  | TC2  | TC1  | TC0      | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1               | C2(1) | C1(0) |

REGISTER 3 (R3)

| RESERVED |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |     |     |     |     |     |     |     |     | CONTROL BITS |       |
|----------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|--------------|-------|
| DB31     | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1          | DB0   |
| 0        | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | C2(1)        | C1(1) |

Figure 17. Latch Summary

12895-017

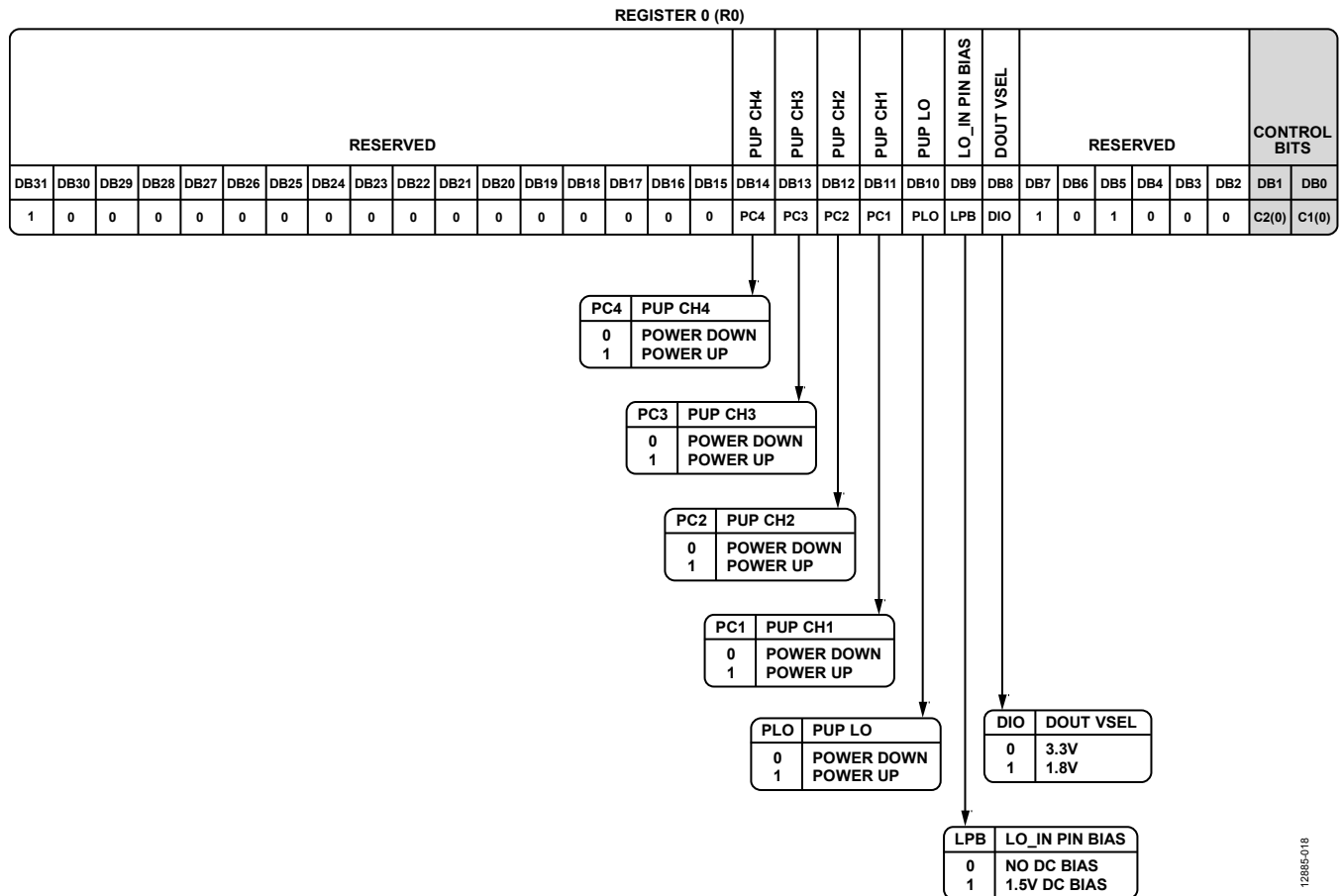


Figure 18. Register 0

**REGISTER 0****Register 0 Control Bits**

With Bits[C2:C1] set to 00, Register R0 is programmed. Figure 18 shows the input data format for programming this register.

**DOUT VSEL**

DB8 controls the DOUT logic levels. Set this bit to 0 to set the DOUT logic level to 3.3 V, and set this bit to 1 to sets the DOUT logic level to 1.8 V.

**LO\_IN Pin Bias**

DB9 controls the dc bias voltage on the LO\_IN pin (Pin 29). Set this bit to 0 to set no dc bias on the LO\_IN pin, and set this bit to 1 to set the dc bias to 1.5 V. AC couple the LO signal to the LO\_IN pin.

**PUP LO**

DB10 provides the power-up bit for the LO block. Set this bit to 0 to power down the LO block, and set this bit to 1 to return the LO block to normal operation.

**PUP CH1**

DB11 provides the power-up bit for RF Receiver Channel 1. Setting this bit to 0 performs a power-down of Channel 1 blocks. Setting this bit to 1 returns Channel 1 blocks to normal operation.

**PUP CH2**

DB12 provides the power-up bit for RF Receiver Channel 2. Set this bit to 0 to power down the Channel 2 blocks, and set this bit to 1 to return the Channel 2 blocks to normal operation.

**PUP CH3**

DB13 provides the power-up bit for RF Receiver Channel 3. Set this bit to 0 to power down the Channel 3 blocks, and set this bit to 1 to return the Channel 3 blocks to normal operation.

**PUP CH4**

DB14 provides the power-up bit for RF Receiver Channel 4. Set this bit to 0 to power down the Channel 4 blocks, and set this bit to 1 to return the Channel 4 blocks to normal operation.

REGISTER 1 (R1)

| CHANNEL SELECT |      |      | RESERVED |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |     |     |     |     |     | CONTROL BITS |     |     |       |       |
|----------------|------|------|----------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|--------------|-----|-----|-------|-------|
| DB31           | DB30 | DB29 | DB28     | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4          | DB3 | DB2 | DB1   | DB0   |
| CS2            | CS1  | CS0  | 0        | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 1    | 0   | 0   | 1   | 0   | 0   | 1            | 1   | 0   | C2(0) | C1(1) |



| CS2 | CS1 | CS0 | CHANNEL SELECT |
|-----|-----|-----|----------------|
| 0   | 0   | 0   | NONE           |
| 0   | 0   | 1   | CHANNEL 1      |
| 0   | 1   | 0   | CHANNEL 2      |
| 0   | 1   | 1   | CHANNEL 3      |
| 1   | 0   | 0   | CHANNEL 4      |
| 1   | 0   | 1   | LO             |
| 1   | 1   | 0   | RESERVED       |
| 1   | 1   | 1   | RESERVED       |

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Figure 19. Register 1

REGISTER 2 (R2)

|          |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |                              |      |      |      |      |          |     |     |     |     |     |     |     |                 |       |       |
|----------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------------------------------|------|------|------|------|----------|-----|-----|-----|-----|-----|-----|-----|-----------------|-------|-------|
| RESERVED |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      | 5-BIT<br>CHANNEL TEST SELECT |      |      |      |      | RESERVED |     |     |     |     |     |     |     | CONTROL<br>BITS |       |       |
| DB31     | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15                         | DB14 | DB13 | DB12 | DB11 | DB10     | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2             | DB1   | DB0   |
| 0        | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0                            | TC4  | TC3  | TC2  | TC1  | TC0      | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1               | C2(1) | C1(0) |

|     |     |     |     |     |                               |
|-----|-----|-----|-----|-----|-------------------------------|
| TC4 | TC3 | TC2 | TC1 | TC0 | CHANNEL TEST SELECT           |
| 0   | 0   | 0   | 0   | 0   | NONE SELECTED                 |
| 0   | 0   | 0   | 0   | 1   | TEMPERATURE SENSOR TO ATEST   |
| 0   | 0   | 0   | 1   | 0   | RESERVED                      |
| 0   | -   | -   | -   | -   | RESERVED                      |
| 0   | 1   | 1   | 1   | 1   | RESERVED                      |
| 1   | 0   | 0   | 0   | 0   | REGISTER 0 READBACK           |
| 1   | 0   | 0   | 0   | 1   | REGISTER 1 CHANNEL 1 READBACK |
| 1   | 0   | 0   | 1   | 0   | REGISTER 1 CHANNEL 2 READBACK |
| 1   | 0   | 0   | 1   | 1   | REGISTER 1 CHANNEL 3 READBACK |
| 1   | 0   | 1   | 0   | 0   | REGISTER 1 CHANNEL 4 READBACK |
| 1   | 0   | 1   | 0   | 1   | REGISTER 1 LO READBACK        |
| 1   | 0   | 1   | 1   | 0   | REGISTER 2 READBACK           |
| 1   | 0   | 1   | 1   | 1   | RESERVED                      |
| 1   | 1   | x   | x   | x   | RESERVED                      |

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Figure 20. Register 2

## REGISTER 1

### Register 1 Control Bits

With Bits[C2:C1] set to 01, Register R1 is programmed. Register 1 contains the internal controls for the four RF channels and the LO path. During the initialization sequence, the default conditions are loaded. See Step 3 to Step 7 in Table 6.

## REGISTER 2

### Register 2 Control Bits

With Bits[C2:C1] set to 10, Register R2 is programmed. Figure 20 shows the input data format for programming this register.

### 5-Bit Channel Test Select

Bits[DB14:DB10] control the [ADF5904](#) test modes. These bits allow access to the temperature sensor on the ATEST pin and the register readback on the DOUT pin. See Figure 20 for the truth table.

## INITIALIZATION SEQUENCE

After powering up the device, administer the initialization sequence in Table 6 to set the register with the code to configure the device.

**Table 6. Initialization Sequence**

| Step | Register | Hex Code   | Description                 |
|------|----------|------------|-----------------------------|
| 1    | R3       | 0x00000003 | Reserved                    |
| 2    | R2       | 0x00020406 | Temperature sensor to ATEST |
| 3    | R1       | 0x20001499 | Configure Channel 1         |
| 4    | R1       | 0x40001499 | Configure Channel 2         |
| 5    | R1       | 0x60001499 | Configure Channel 3         |
| 6    | R1       | 0x80001499 | Configure Channel 4         |
| 7    | R1       | 0xA0000019 | Configure LO                |
| 8    | R0       | 0x80007CA0 | Power up                    |

## TEMPERATURE SENSOR

The on-chip temperature sensor of the ADF5904 is accessed on the ATEST pin. The temperature sensor operates over the full operating temperature range of  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . To improve accuracy, conduct a one-point calibration at room temperature and store the result in the external memory. Convert the ATEST voltage to temperature by using the following equation:

$$\text{Temperature } (^{\circ}\text{C}) = (V_{\text{ATEST}} - V_{\text{OFF}})/V_{\text{GAIN}}$$

where:

$V_{\text{ATEST}}$  is the voltage on the ATEST pin.

$V_{\text{OFF}}$  is the offset voltage and it is 1.212 V.

$V_{\text{GAIN}}$  is the voltage gain and it is  $4.072\text{e}^{-3}$ .

## APPLICATION INFORMATION

### APPLICATION OF THE ADF5904 IN FMCW RADAR

Figure 21 shows the application of the ADF5904 in a frequency modulated continuous wave (FMCW) radar system.

In the FMCW radar system, the ADF4159 generates the sawtooth or triangle ramps necessary for this type of radar to operate.

The ADF4159 controls the VTUNE pin on the transceiver (Tx) monolithic microwave integrated circuit (MMIC) and thus the frequency of the voltage controlled oscillator (VCO) and the Tx output signal on TXOUT1 or TXOUT2. The LO signal from the Tx MMIC is fed to the LO input on the ADF5904.

The ADF5904 downconverts the signal from the four receiver antennas to baseband with the LO signal from the Tx MMIC.

The downconverted baseband signals from the four receiver channels on the ADF5904 are fed to the ADAR7251 4-channel, continuous time (CT), sigma-delta ( $\Sigma$ - $\Delta$ ) analog-to-digital converter (ADC).

A digital signal processor (DSP) follows the ADC to handle the target information processing.

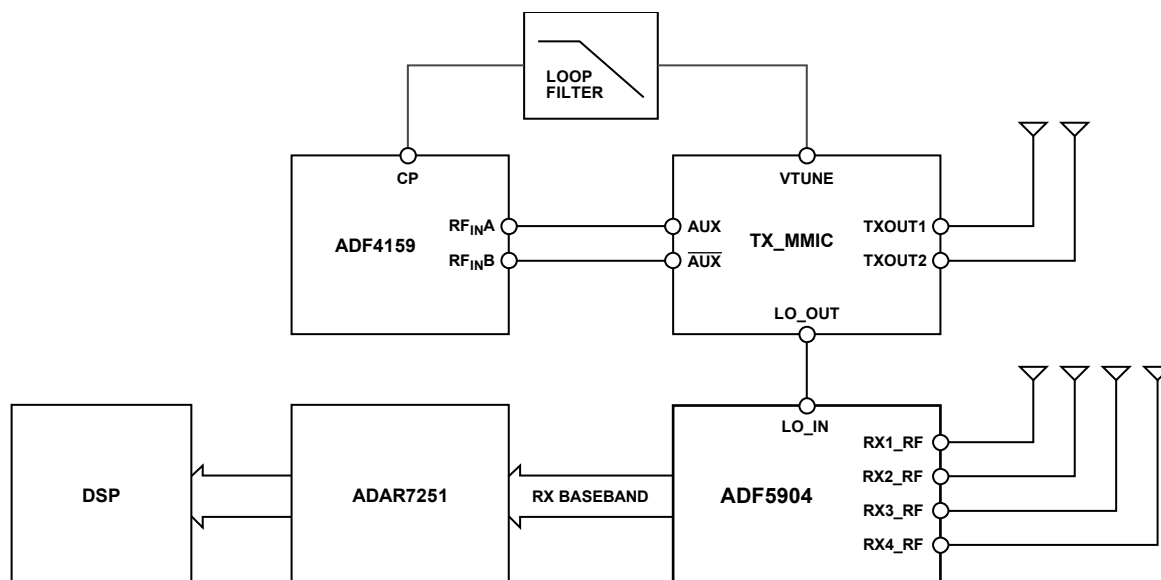
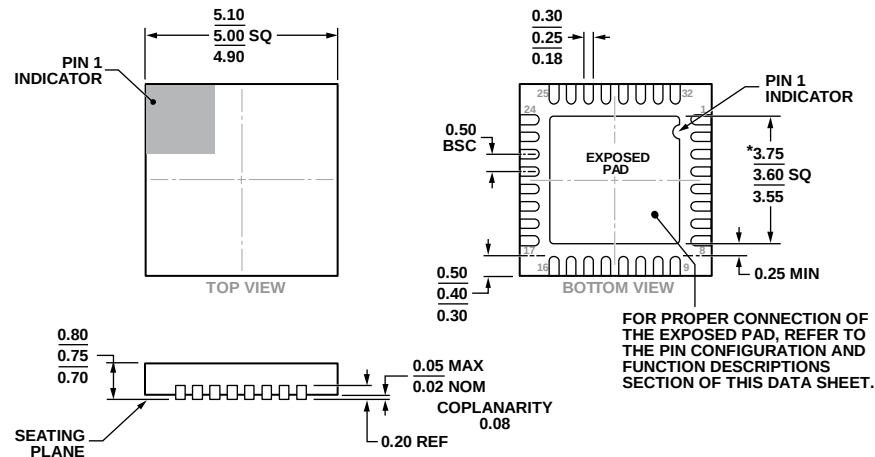


Figure 21. FMCW Radar with ADF5904

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## OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5  
WITH THE EXCEPTION OF THE EXPOSED PAD DIMENSION.

Figure 22. 32-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
5 mm × 5 mm Body, Very Very Thin Quad  
(CP-32-12)  
Dimensions shown in millimeters

08-16-2010-B

## ORDERING GUIDE

| Model <sup>1,2</sup> | Temperature Range | Package Description                              | Package Option |
|----------------------|-------------------|--------------------------------------------------|----------------|
| ADF5904WCCPZ         | −40°C to +105°C   | 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-32-12       |
| ADF5904WCCPZ-RL7     | −40°C to +105°C   | 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-32-12       |
| ADF5904ACPZ          | −40°C to +105°C   | 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-32-12       |
| ADF5904ACPZ-RL7      | −40°C to +105°C   | 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-32-12       |
| EV-ADF5904SD2Z       |                   | Evaluation Board                                 |                |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The [ADF5904W](#) models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.