

## FEATURES

**Low input offset voltage:** 75  $\mu\text{V}$  maximum  
**Low offset voltage drift, over  $-55^\circ\text{C} < T_A < +125^\circ\text{C}$**   
     0.5  $\mu\text{V}/^\circ\text{C}$  maximum  
**Low supply current (per amplifier):** 725  $\mu\text{A}$  maximum  
**High open-loop gain:** 5000 V/mV minimum  
**Low input bias current:** 2 nA maximum  
**Low noise voltage density:** 11 nV/ $\sqrt{\text{Hz}}$  at 1 kHz  
**Stable with large capacitive loads:** 10 nF typical

## PIN CONNECTIONS

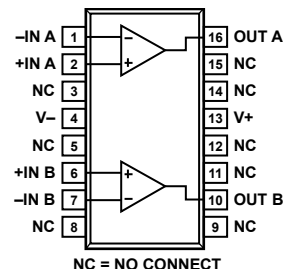


Figure 1. 16-Lead SOIC (S-Suffix)

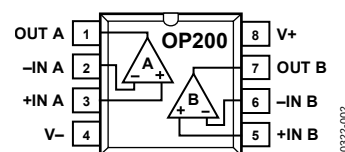


Figure 2. 8-Lead PDIP (P-Suffix)  
8-Lead CERDIP (Z-Suffix)

## GENERAL DESCRIPTION

The **OP200** is the first monolithic dual operational amplifier to offer **OP77** type precision performance. Available in the industry standard 8-lead pinout, the **OP200** combines precision performance with the space and cost savings offered by a dual amplifier.

The **OP200** features an extremely low input offset voltage of less than 75  $\mu\text{V}$  with a drift below 0.5  $\mu\text{V}/^\circ\text{C}$ , guaranteed over the full military temperature range. Open-loop gain of the **OP200** exceeds 5,000,000 into a 10 k $\Omega$  load; input bias current is under 2 nA; CMRR is over 120 dB; and PSRR is below 1.8  $\mu\text{V}/\text{V}$ . On-chip Zener zap trimming is used to achieve the extremely low input offset voltage of the **OP200** and eliminates the need for offset pulling.

Power consumption of the **OP200** is low, with each amplifier drawing less than 725  $\mu\text{A}$  of supply current. The total current drawn by the dual **OP200** is less than one-half that of a single **OP07**, yet the **OP200** offers significant improvements over this industry-standard op amp. The voltage noise density of the **OP200**, 11 nV/ $\sqrt{\text{Hz}}$  at 1 kHz, is half that of most competitive devices.

The **OP200** is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the **OP400**.

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## REVISION HISTORY

### 3/2017—Rev. F to Rev. G

|                            |    |
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| Changes to Figure 21 ..... | 10 |
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### 10/2015—Rev. E to Rev. F

|                                      |    |
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### 9/2012—Rev. D to Rev. E

|                                                                                      |    |
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| Changed Table 2 Conditions from $V_S = 15\text{ V}$ to $V_S = \pm 15\text{ V}$ ..... | 4  |
| Updated Outline Dimensions .....                                                     | 15 |
| Changes to Ordering Guide .....                                                      | 16 |

### 2/2009—Rev. C to Rev. D

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| Change to Large Signal Voltage Gain, Table 2 ..... | 4  |
| Changes to Ordering Guide .....                    | 16 |

### 8/2008—Rev. B to Rev. C

|                                               |           |
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| Updated Format .....                          | Universal |
| Changes to Features Section.....              | 1         |
| Changes to Table 1 and Table 2.....           | 4         |
| Changes to Table 3 and Table 4.....           | 5         |
| Deleted Table 7; Renumbered Sequentially..... | 5         |

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### 2/2004—Rev. A to Rev. B.

|                                 |           |
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| OP200F Deleted.....             | Universal |
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| Changes to Figure 4.....        | 8         |
| Updated Outline Dimension ..... | 11        |

### 4/2002—Rev. 0 to Rev. A.

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| Edits to Features.....                  | 1 |
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| Edits to Pin Connections.....           | 1 |
| Edits to Absolute Maximum Ratings ..... | 2 |
| Edits to Package Type .....             | 2 |

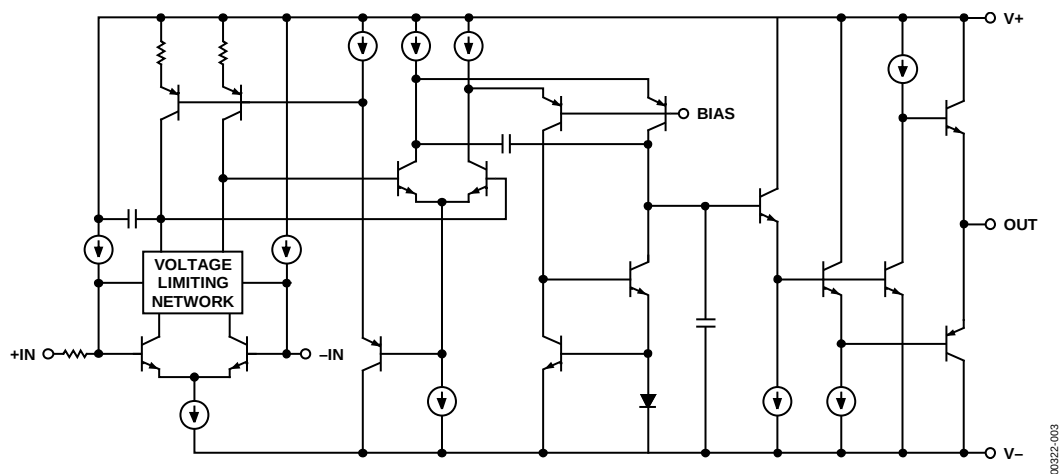


Figure 3. Simplified Schematic (One of Two Amplifiers Shown)

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

| Parameter                                | Symbol             | Conditions               | OP200A/OP200E |        |     | OP200G |      |     | Unit   |
|------------------------------------------|--------------------|--------------------------|---------------|--------|-----|--------|------|-----|--------|
|                                          |                    |                          | Min           | Typ    | Max | Min    | Typ  | Max |        |
| INPUT CHARACTERISTICS                    |                    |                          |               |        |     |        |      |     |        |
| Input Offset Voltage                     | V <sub>OS</sub>    |                          |               | 25     | 75  |        | 80   | 200 | μV     |
| Long-Term Input Voltage Stability        |                    |                          |               | 0.1    |     |        | 0.1  |     | μV/mo  |
| Input Offset Current                     | I <sub>OS</sub>    | V <sub>CM</sub> = 0 V    |               | 0.05   | 1.0 |        | 0.05 | 3.5 | nA     |
| Input Bias Current                       | I <sub>B</sub>     | V <sub>CM</sub> = 0 V    |               | 0.1    | 2.0 |        | 0.1  | 5.0 | nA     |
| Input Noise Voltage                      | e <sub>n</sub> p-p | 0.1 Hz to 10 Hz          |               | 0.5    |     |        | 0.5  |     | μV p-p |
| Input Noise Voltage Density <sup>1</sup> | e <sub>n</sub>     | f <sub>0</sub> = 10 Hz   |               | 22     | 36  |        | 22   |     | nV/√Hz |
|                                          |                    | f <sub>0</sub> = 1000 Hz |               | 11     | 18  |        | 11   |     | nV/√Hz |
| Input Noise Current                      | i <sub>n</sub> p-p | 0.1 Hz to 10 Hz          |               | 15     |     |        | 15   |     | pA p-p |
| Input Noise Current Density              | i <sub>n</sub>     | f <sub>0</sub> = 10 Hz   |               | 0.4    |     |        | 0.4  |     | pA/√Hz |
| Input Resistance Differential Mode       | R <sub>IN</sub>    |                          |               | 10     |     |        | 10   |     | MΩ     |
| Input Resistance Common Mode             | R <sub>INCM</sub>  |                          |               | 125    |     |        | 125  |     | GΩ     |
| Large Signal Voltage Gain                | A <sub>VO</sub>    | V <sub>O</sub> = ±10 V   |               |        |     |        |      |     |        |
|                                          |                    | R <sub>L</sub> = 10 kΩ   | 5000          | 12,000 |     | 3000   | 7000 |     | M/mV   |
|                                          |                    | R <sub>L</sub> = 2 kΩ    | 2000          | 3700   |     | 1500   | 3200 |     | M/mV   |

<sup>1</sup> Sample tested.

$V_S = \pm 15\text{ V}$ ,  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  for OP200A, unless otherwise noted.

Table 2.

| Parameter                          | Symbol            | Conditions                   | OP200A |       |     | Unit  |
|------------------------------------|-------------------|------------------------------|--------|-------|-----|-------|
|                                    |                   |                              | Min    | Typ   | Max |       |
| INPUT CHARACTERISTICS              |                   |                              |        |       |     |       |
| Input Offset Voltage               | V <sub>OS</sub>   |                              |        | 45    | 125 | μV    |
| Average Input Offset Voltage Drift | TCV <sub>OS</sub> |                              |        | 0.2   | 0.5 | μV/°C |
| Input Offset Current               | I <sub>OS</sub>   | V <sub>CM</sub> = 0 V        |        | 0.15  | 2.5 | nA    |
| Input Bias Current                 | I <sub>B</sub>    | V <sub>CM</sub> = 0 V        |        | 0.9   | 5.0 | nA    |
| Large Signal Voltage Gain          | A <sub>VO</sub>   | V <sub>O</sub> = 10 V        |        |       |     |       |
|                                    |                   | R <sub>L</sub> = 10 kΩ       | 3000   | 9000  |     | V/mV  |
|                                    |                   | R <sub>L</sub> = 2 kΩ        | 1000   | 2700  |     | V/mV  |
| Input Voltage Range <sup>1</sup>   | IVR               |                              | ±12    | ±12.5 |     | V     |
| Common-Mode Rejection Ratio        | CMRR              | V <sub>CM</sub> = ±12 V      | 115    | 130   |     | dB    |
| Capacitive Load Stability          |                   | A <sub>v</sub> = 1           |        | 8     |     | nF    |
| POWER SUPPLY                       |                   |                              |        |       |     |       |
| Power Supply Rejection Ratio       | PSRR              | V <sub>S</sub> = 3 V to 18 V |        | 0.2   | 3.2 | μV/V  |
| Supply Current Per Amplifier       | I <sub>SY</sub>   | No load                      |        | 600   | 775 | μA    |
| OUTPUT CHARACTERISTICS             |                   |                              |        |       |     |       |
| Output Voltage Swing               | V <sub>O</sub>    | R <sub>L</sub> = 10 kΩ       | ±12    | ±12.4 |     | V     |
|                                    |                   | R <sub>L</sub> = 2 kΩ        | ±11    | ±12   |     | V     |

<sup>1</sup> Guaranteed by CMRR test.

$V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

| Parameter                        | Symbol   | Conditions                                                                   | OP200A/OP200E |            |     | OP200G   |            |     | Unit             |
|----------------------------------|----------|------------------------------------------------------------------------------|---------------|------------|-----|----------|------------|-----|------------------|
|                                  |          |                                                                              | Min           | Typ        | Max | Min      | Typ        | Max |                  |
| INPUT CHARACTERISTICS            |          |                                                                              |               |            |     |          |            |     |                  |
| Input Voltage Range <sup>1</sup> | IVR      | $V_{CM} = \pm 12\text{ V}$<br>$V_O = 20\text{ V p-p}$ , $f_o = 10\text{ Hz}$ | $\pm 12$      | $\pm 13$   |     | $\pm 12$ | $\pm 13$   |     | V                |
| Common-Mode Rejection Ratio      | CMRR     |                                                                              | 120           | 135        |     | 110      | 130        |     | dB               |
| Channel Separation <sup>2</sup>  | CS       |                                                                              | 123           | 145        |     | 123      | 145        |     | dB               |
| Input Capacitance                | $C_{IN}$ | $A_V = 1$ , no oscillations                                                  |               | 3.2        |     |          | 3.2        |     | pF               |
| Capacitive Load Stability        |          |                                                                              |               | 10         |     |          | 10         |     | nF               |
| POWER SUPPLY                     |          |                                                                              |               |            |     |          |            |     |                  |
| Power Supply Rejection Ratio     | PSRR     | $V_S = \pm 3\text{ V to } \pm 18\text{ V}$                                   |               | 0.4        | 1.8 |          | 0.6        | 5.6 | $\mu\text{V/V}$  |
| Supply Current Per Amplifier     | $I_{SY}$ | No load                                                                      |               | 570        | 725 |          | 570        | 725 | $\mu\text{A}$    |
| OUTPUT CHARACTERISTICS           |          |                                                                              |               |            |     |          |            |     |                  |
| Output Voltage Swing             | $V_O$    | $R_L = 10\text{ k}\Omega$                                                    | $\pm 12$      | $\pm 12.6$ |     | $\pm 12$ | $\pm 12.6$ |     | V                |
|                                  |          | $R_L = 2\text{ k}\Omega$                                                     | $\pm 11$      | $\pm 12.2$ |     | $\pm 11$ | $\pm 12.2$ |     | V                |
| DYNAMIC PERFORMANCE              |          |                                                                              |               |            |     |          |            |     |                  |
| Slew Rate                        | SR       | $A_V = 1$                                                                    | 0.1           | 0.15       |     | 0.1      | 0.15       |     | V/ $\mu\text{s}$ |
| Gain Bandwidth Product           | GBP      |                                                                              |               | 500        |     |          | 500        |     | kHz              |

<sup>1</sup> Guaranteed by CMRR test.

<sup>2</sup> Guaranteed but not 100% tested.

$V_S = \pm 15\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise noted.

Table 4.

| Parameter                          | Symbol            | Conditions                          | OP200E |        |     | OP200G |       |      | Unit  |
|------------------------------------|-------------------|-------------------------------------|--------|--------|-----|--------|-------|------|-------|
|                                    |                   |                                     | Min    | Typ    | Max | Min    | Typ   | Max  |       |
| INPUT CHARACTERISTICS              |                   |                                     |        |        |     |        |       |      |       |
| Input Offset Voltage               | V <sub>OS</sub>   |                                     |        | 35     | 100 |        | 110   | 300  | μV    |
| Average Input Offset Voltage Drift | TCV <sub>OS</sub> |                                     |        | 0.2    | 0.5 |        | 0.6   | 2.0  | μV/°C |
| Input Offset Current               | I <sub>OS</sub>   | V <sub>CM</sub> = 0 V               |        | 0.08   | 2.5 |        | 0.1   | 6.0  | nA    |
| Input Bias Current                 | I <sub>B</sub>    | V <sub>CM</sub> = 0 V               |        | 0.3    | 5.0 |        | 0.5   | 10.0 | nA    |
| Large-Signal Voltage Gain          | A <sub>VO</sub>   | V <sub>O</sub> = ±10 V              |        |        |     |        |       |      |       |
|                                    |                   | R <sub>L</sub> = 10 kΩ              | 3000   | 10,000 |     | 2000   | 5000  |      | V/mV  |
|                                    |                   | R <sub>L</sub> = 2 kΩ               | 1500   | 3200   |     | 1000   | 2500  |      | V/mV  |
| Input Voltage Range <sup>1</sup>   | IVR               |                                     | ±12    | ±12.5  |     | ±12    | ±12.5 |      | V     |
| Common-Mode Rejection Ratio        | CMRR              | V <sub>CM</sub> = ±12 V             | 115    | 130    |     | 105    | 130   |      | dB    |
| Capacitive Load Stability          |                   | A <sub>V</sub> = 1, no oscillations |        | 10     |     |        | 10    |      | nF    |
| POWER SUPPLY                       |                   |                                     |        |        |     |        |       |      |       |
| Power Supply Rejection Ratio       | PSRR              | V <sub>S</sub> = ±3 V to ±18 V      |        | 0.15   | 3.2 |        | 0.3   | 10.0 | μV/V  |
| Supply Current Per Amplifier       | I <sub>SY</sub>   | No load                             |        | 600    | 775 |        | 600   | 775  | μA    |
| OUTPUT CHARACTERISTICS             |                   |                                     |        |        |     |        |       |      |       |
| Output Voltage Swing               | V <sub>O</sub>    | R <sub>L</sub> = 10 kΩ              | ±12    | ±12.4  |     | ±12    | ±12.4 |      | V     |
|                                    |                   | R <sub>L</sub> = 2 kΩ               | ±11    | ±12    |     | ±11    | ±12.2 |      | V     |

<sup>1</sup> Guaranteed by CMRR test.

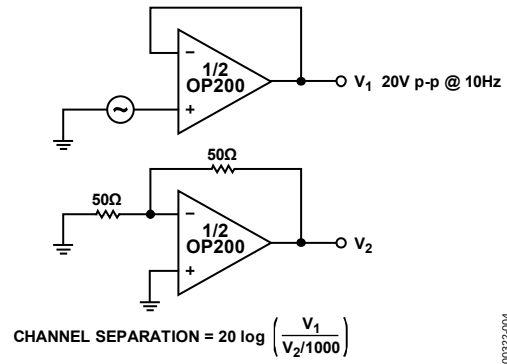


Figure 4. Channel Separation Test Circuit

00322-004

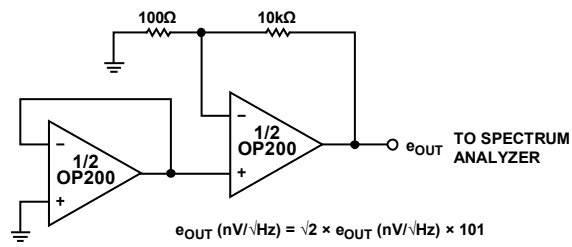


Figure 5. Noise Test Schematic

00322-005

## ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter                            | Rating                                          |
|--------------------------------------|-------------------------------------------------|
| Supply Voltage                       | $\pm 20$ V                                      |
| Differential Input Voltage           | $\pm 30$ V                                      |
| Input Voltage                        | Supply voltage                                  |
| Output Short-Circuit Duration        | Continuous                                      |
| Storage Temperature Range            | $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ |
| Lead Temperature (Soldering, 60 sec) | $300^{\circ}\text{C}$                           |
| Junction Temperature Range ( $T_J$ ) | $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ |
| Operating Temperature Range          |                                                 |
| OP200A                               | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| OP200E, OP200G                       | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Table 6.

| Package Type                  | $\theta_{JA}^1$ | $\theta_{JC}$ | Unit                        |
|-------------------------------|-----------------|---------------|-----------------------------|
| 8-Lead Cerdip (Z Suffix)      | 148             | 16            | $^{\circ}\text{C}/\text{W}$ |
| 8-Lead Plastic DIP (P Suffix) | 96              | 37            | $^{\circ}\text{C}/\text{W}$ |
| 16-Lead SOIC (S Suffix)       | 92              | 27            | $^{\circ}\text{C}/\text{W}$ |

<sup>1</sup>  $\theta_{JA}$  is specified for worst-case mounting conditions, that is,  $\theta_{JA}$  is specified for device in socket for Cerdip and PDIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SOIC package.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

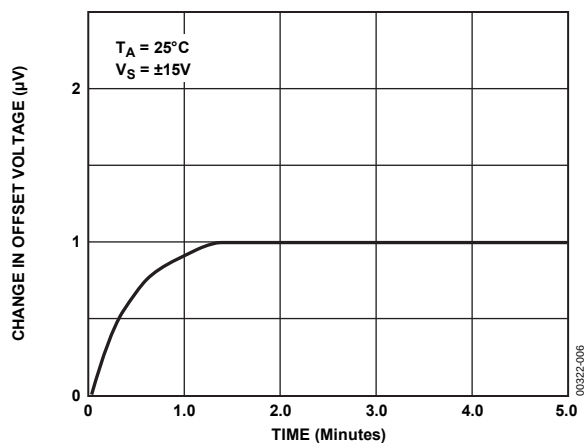


Figure 6. Warm-Up Drift

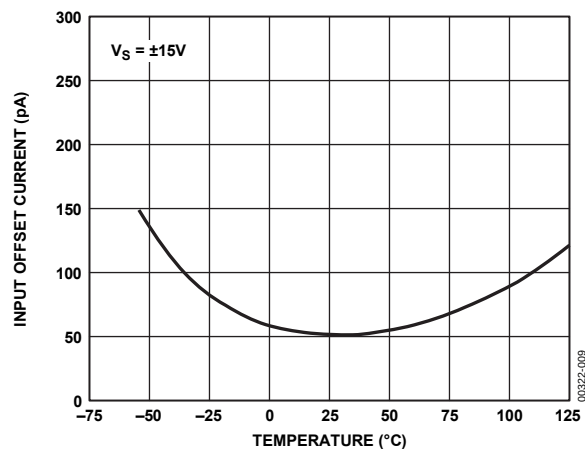


Figure 9. Input Offset Current vs. Temperature

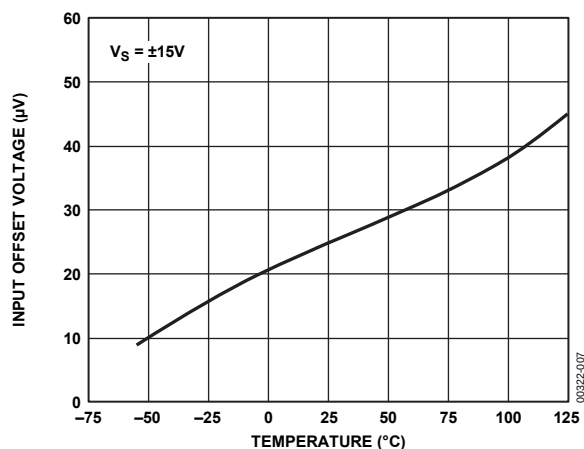


Figure 7. Input Offset Voltage vs. Temperature

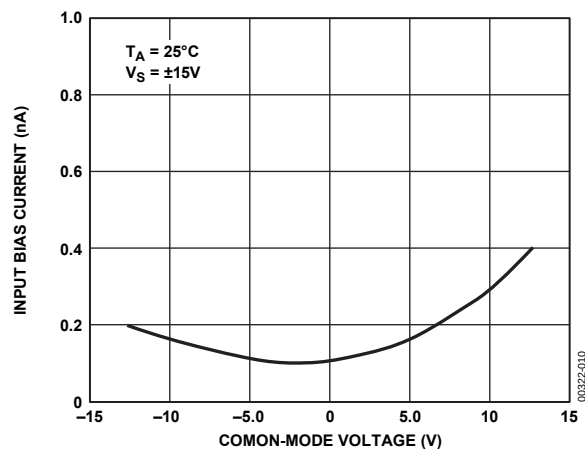


Figure 10. Input Bias Current vs. Common-Mode Voltage

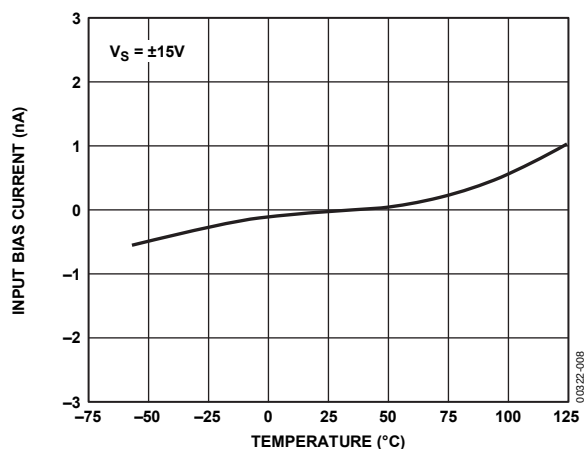


Figure 8. Input Bias Current vs. Temperature

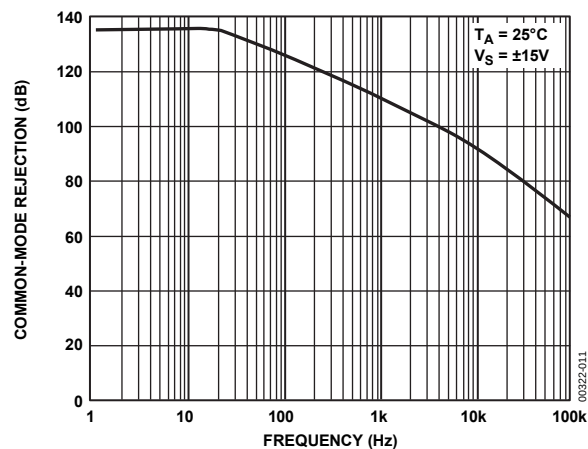


Figure 11. Common-Mode Rejection vs. Frequency



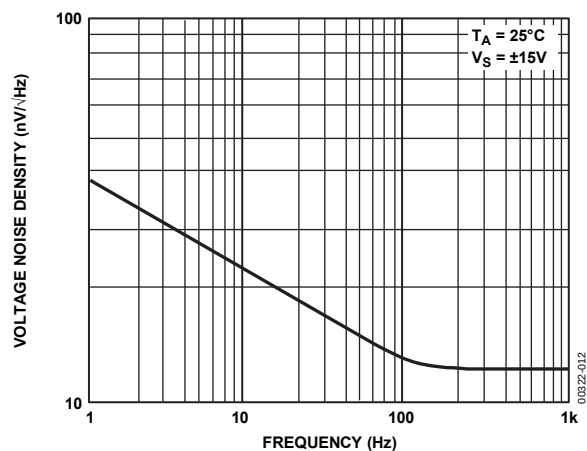


Figure 12. Voltage Noise Density vs. Frequency

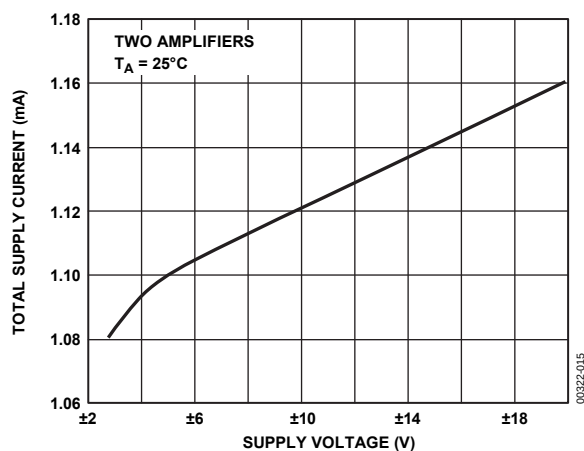


Figure 15. Total Supply Current vs. Supply Voltage

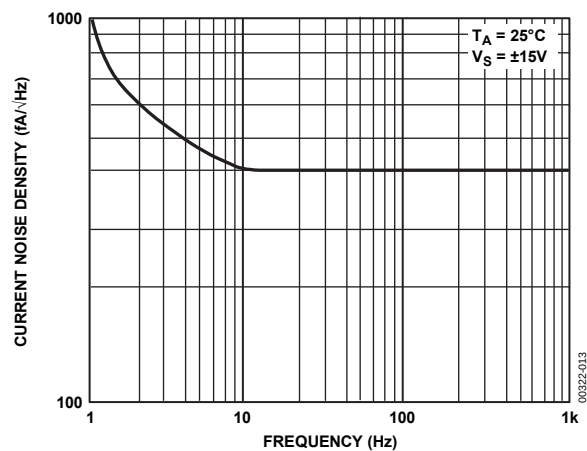


Figure 13. Current Noise Density vs. Frequency

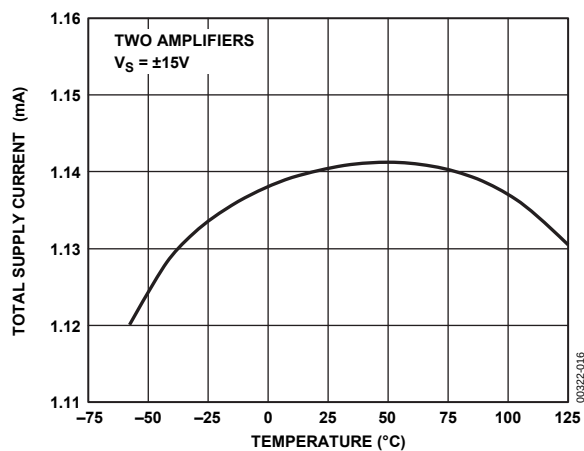


Figure 16. Total Supply Current vs. Temperature

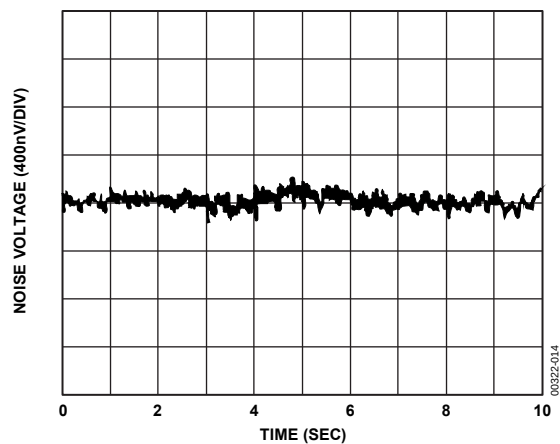


Figure 14. 0.1 Hz to 10 Hz Noise

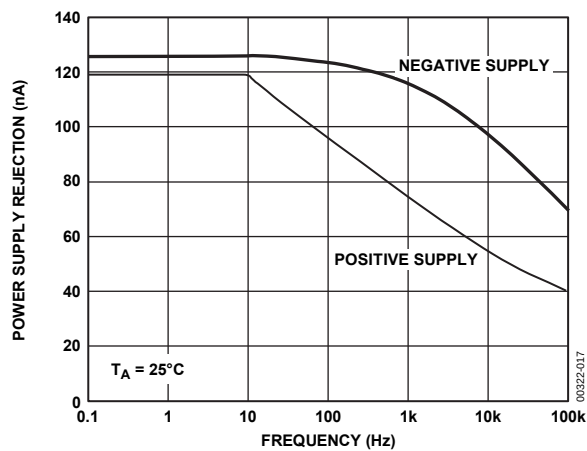


Figure 17. Power Supply Rejection vs. Frequency

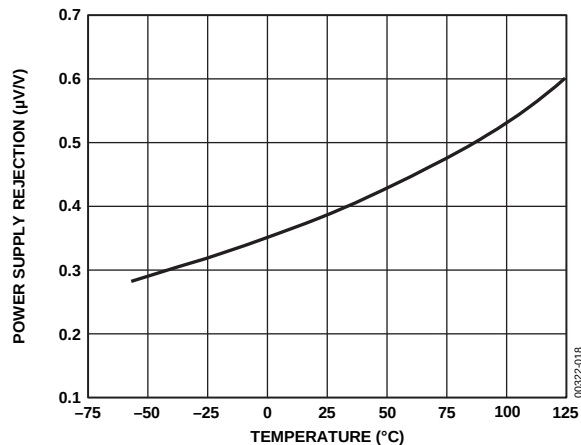


Figure 18. Power Supply Rejection vs. Temperature

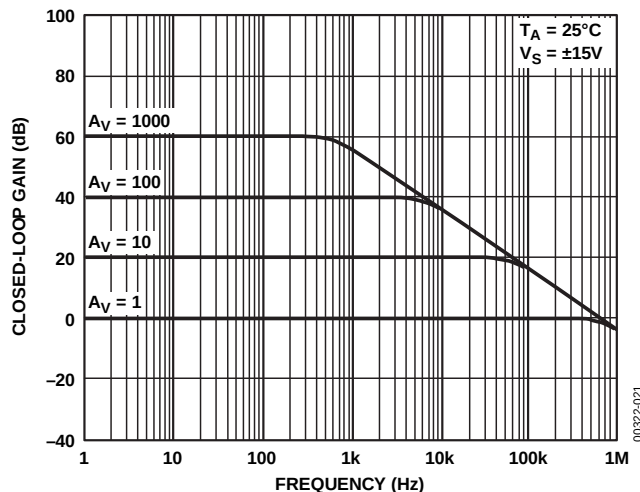


Figure 21. Closed-Loop Gain vs. Frequency

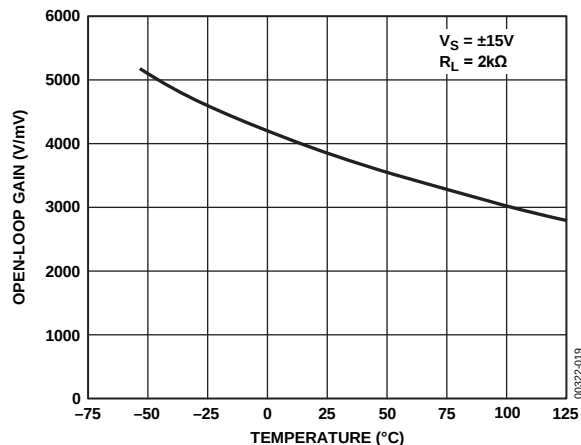


Figure 19. Open-Loop Gain vs. Temperature

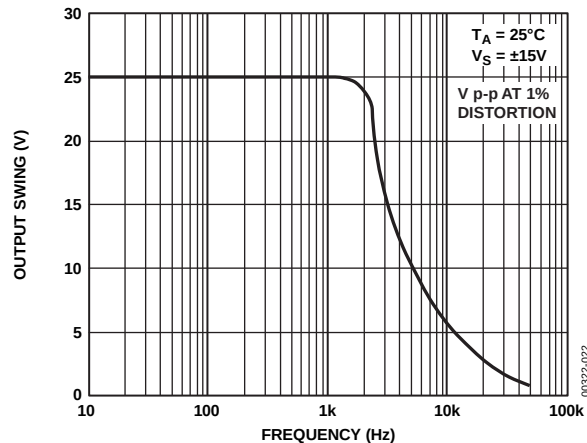


Figure 22. Maximum Output Swing vs. Frequency

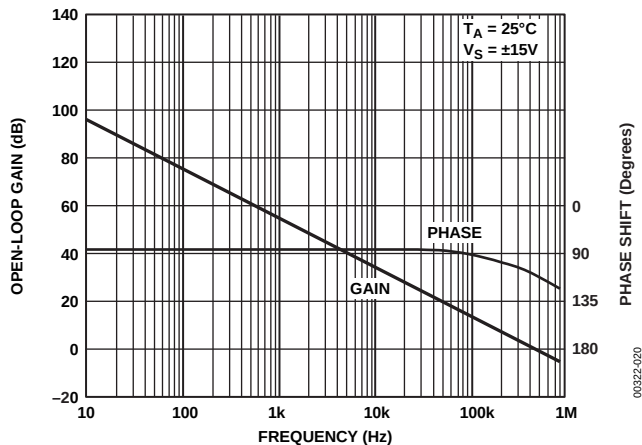


Figure 20. Open-Loop Gain and Phase Shift vs. Frequency

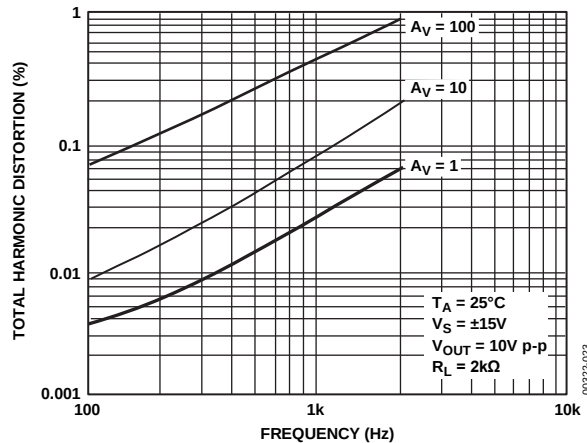


Figure 23. Total Harmonic Distortion vs. Frequency

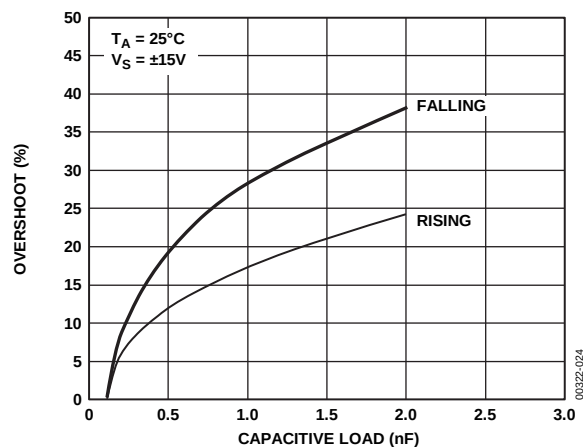


Figure 24. Overshoot vs. Capacitive Load

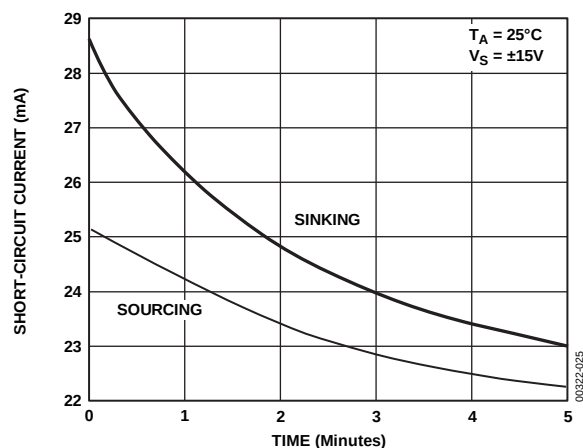


Figure 25. Short-Circuit Current vs. Time

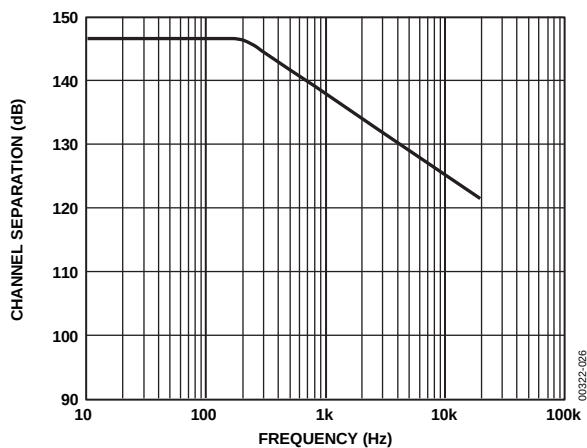


Figure 26. Channel Separation vs. Frequency

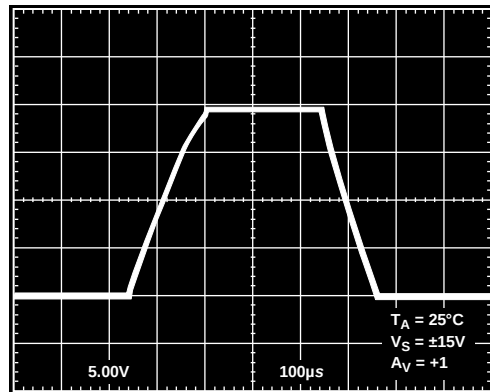


Figure 27. Large Signal Transient Response

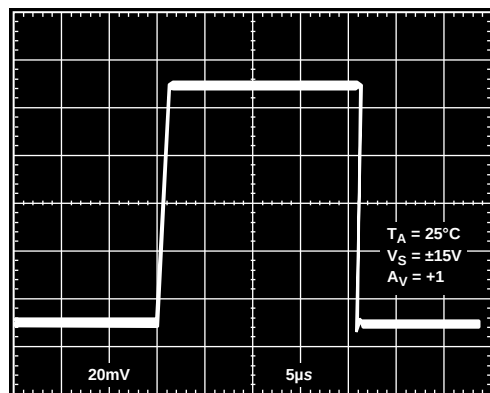
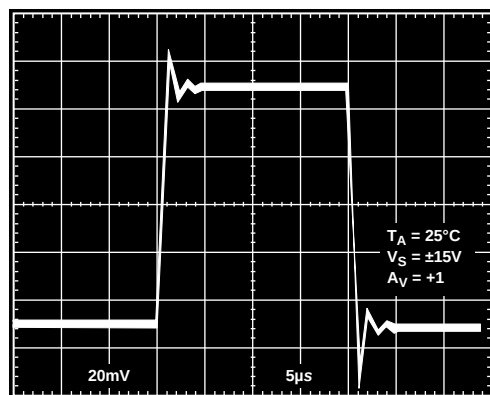


Figure 28. Small Signal Transient Response

Figure 29. Small Signal Transient Response,  $C_{LOAD} = 1\text{ nF}$

## APPLICATIONS INFORMATION

The OP200 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP200.

### DUAL LOW POWER INSTRUMENTATION AMPLIFIER

A dual instrumentation amplifier that consumes less than 33 mW of power per channel is shown in Figure 30. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115 dB (gain = 1000). Offset voltage drift is typically  $0.2 \mu\text{V}/^\circ\text{C}$  over the military temperature range, which is comparable to the best monolithic instrumentation amplifiers. The bandwidth of the low power instrumentation amplifier is a function of gain and is shown in Table 7.

Table 7. Gain Bandwidth

| Gain | Bandwidth |
|------|-----------|
| 5    | 150 kHz   |
| 10   | 67 kHz    |
| 100  | 7.5 kHz   |
| 1000 | 500 Hz    |

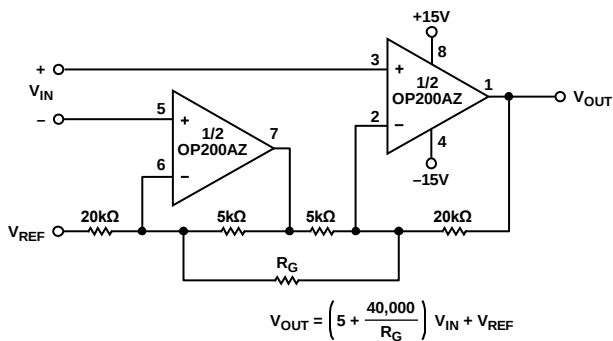


Figure 30. Dual Low Power Instrumentation Amplifier

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from  $-10 \text{ V}$  to  $+10 \text{ V}$  if required.

### PRECISION ABSOLUTE VALUE AMPLIFIER

The circuit in Figure 31 is a precision absolute value amplifier with an input impedance of  $10 \text{ M}\Omega$ . The high gain and low  $\text{TCV}_{OS}$  of the OP200 ensure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMRR of the OP200 exceeds 120 dB, yielding an error of less than 2 ppm.

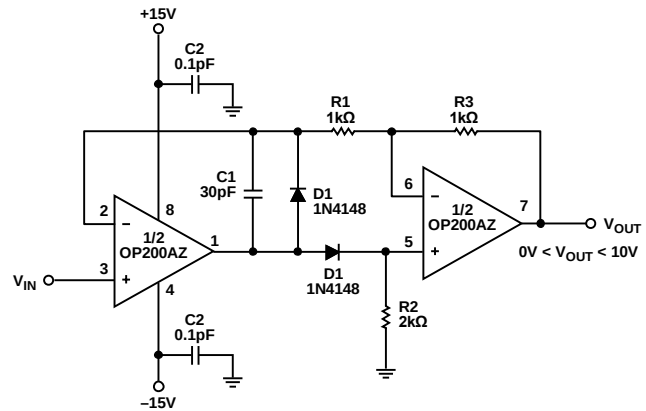


Figure 31. Precision Absolute Value Amplifier

### PRECISION CURRENT PUMP

The maximum output current of the precision current pump shown in Figure 32 is  $\pm 10 \text{ mA}$ . Voltage compliance is  $\pm 10 \text{ V}$  with  $\pm 15 \text{ V}$  supplies. Output impedance of the current transmitter exceeds  $3 \text{ M}\Omega$  with linearity better than 16 bits.

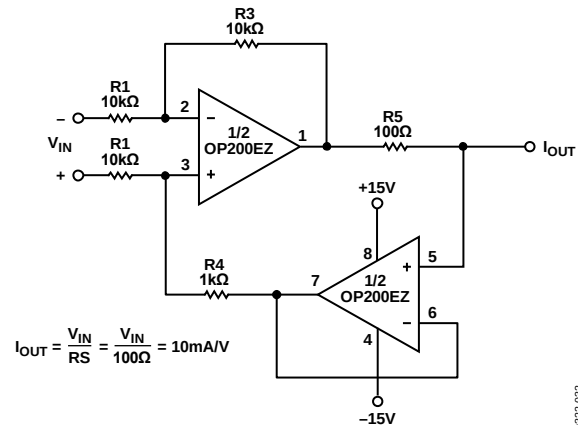


Figure 32. Precision Current Pump

### DUAL 12-BIT VOLTAGE OUTPUT DAC

The dual output DAC shown in Figure 33 is capable of providing untrimmed 12-bit accurate operation over the entire military temperature range. Offset voltage, bias current, and gain errors of the **OP200** contribute less than 1/10 of an LSB error at 12 bits over the military temperature range.

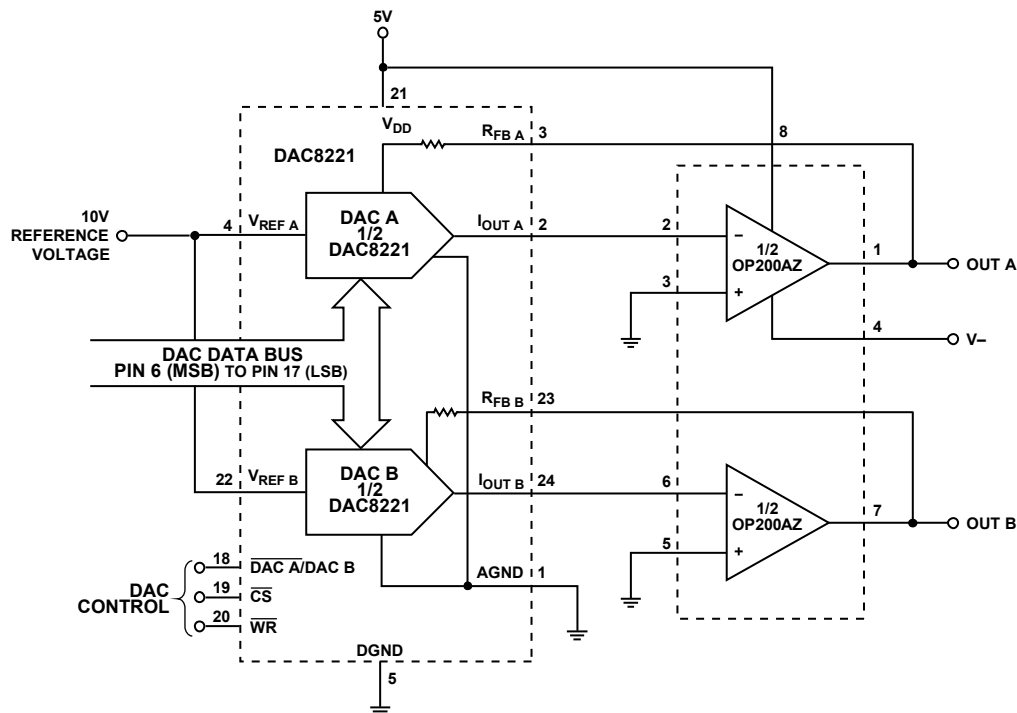


Figure 33. Dual 12-Bit Voltage Output DAC

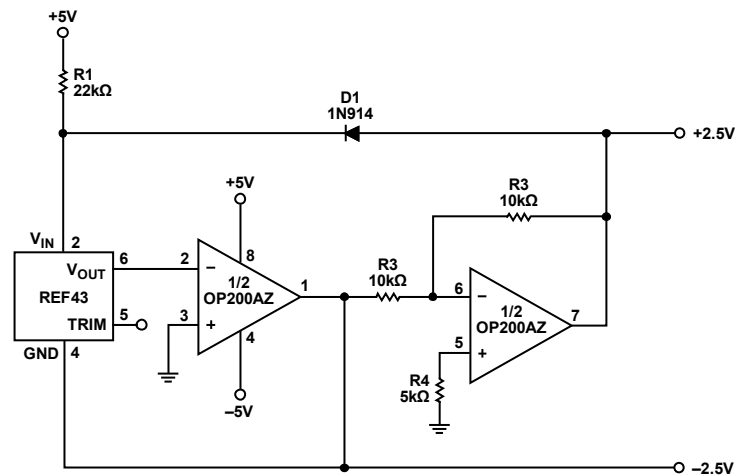


Figure 34. Dual Precision Voltage Reference

# PROGRAMMABLE HIGH RESOLUTION WINDOW COMPARATOR

The programmable window comparator shown in Figure 35 is easily capable of 12-bit accuracy over the full military temperature

range. A dual CMOS 12-bit DAC, the [DAC8221](#), is used in the voltage switching mode to set the upper and lower thresholds (DAC A and DAC B, respectively).

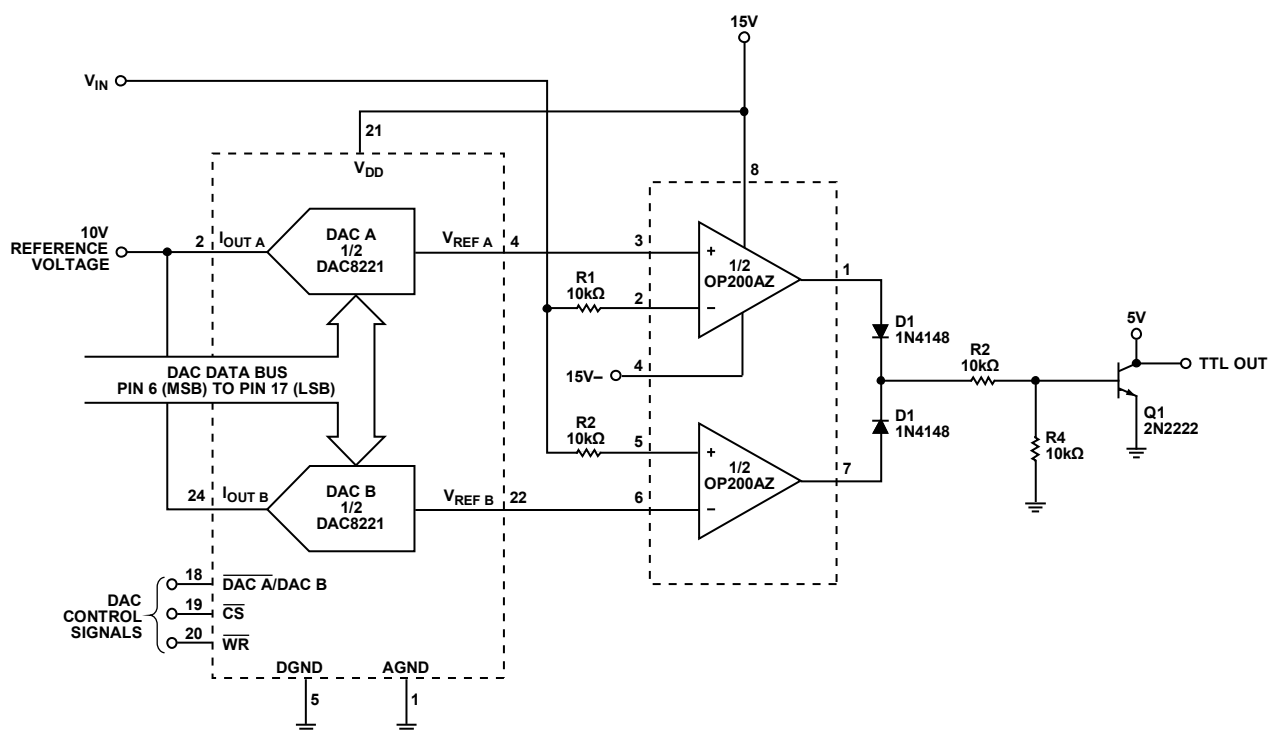
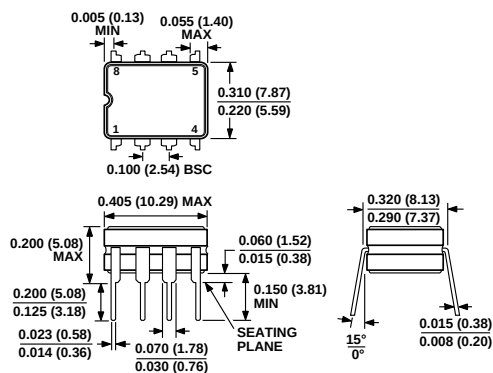


Figure 35. Programmable High Resolution Window Comparator

00322-035

## OUTLINE DIMENSIONS

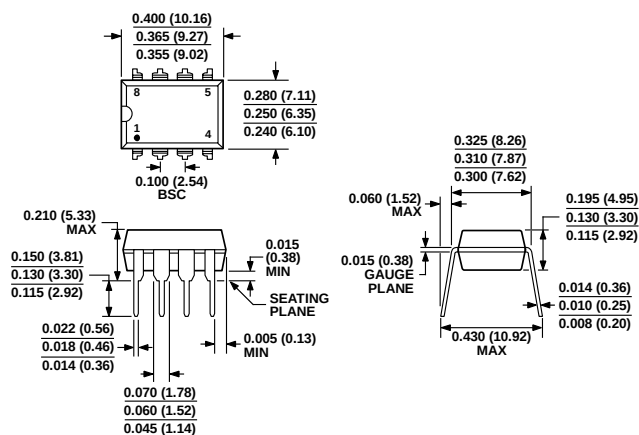


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 8-Lead Ceramic Dual In-Line Package [CERDIP]  
(Q-8)

Z-Suffix

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001

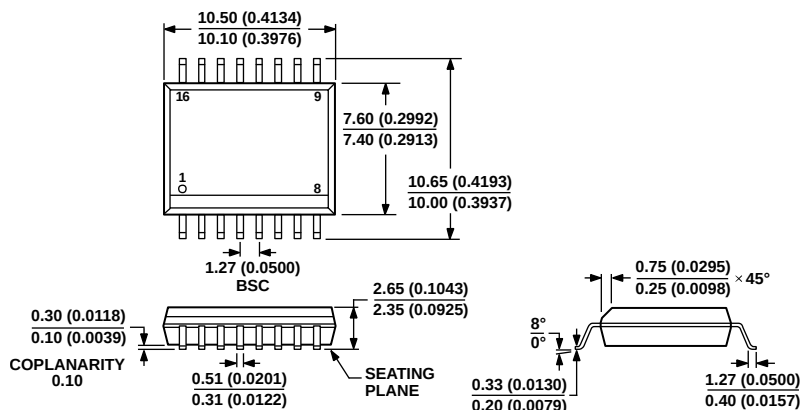
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 37. 8-Lead Plastic Dual In-Line Package [PDIP]  
(N-8)

P-Suffix

Dimensions shown in inches and (millimeters)

071606-A



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 38. 16-Lead Standard Small Outline Package [SOIC\_W]  
Wide Body  
(RW-16)  
S-Suffix

Dimensions shown in millimeters and (inches)

03-27-2007-B

## ORDERING GUIDE

| Model <sup>1</sup> | T <sub>A</sub> = 25°C V <sub>OS</sub> Max (μV) | Temperature Range | Package Description | Package Option   |
|--------------------|------------------------------------------------|-------------------|---------------------|------------------|
| OP200AZ            | 75                                             | –55°C to +125°C   | 8-Lead CERDIP       | Z-Suffix (Q-8)   |
| OP200EZ            | 75                                             | –40°C to +85°C    | 8-Lead CERDIP       | Z-Suffix (Q-8)   |
| OP200GPZ           | 200                                            | –40°C to +85°C    | 8-Lead PDIP         | P-Suffix (N-8)   |
| OP200GSZ           | 200                                            | –40°C to +85°C    | 16-Lead SOIC_W      | S-Suffix (RW-16) |
| OP200GSZ-REEL      | 200                                            | –40°C to +85°C    | 16-Lead SOIC_W      | S-Suffix (RW-16) |

<sup>1</sup> The OP200GPZ, OP200GSZ, and OP200GSZ-REEL are RoHS Compliant Parts.