

## UTC 75323

## LINEAR INTEGRATED CIRCUIT

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### MULTIPLE RS-232 DRIVERS AND RECEIVERS

#### DESCRIPTION

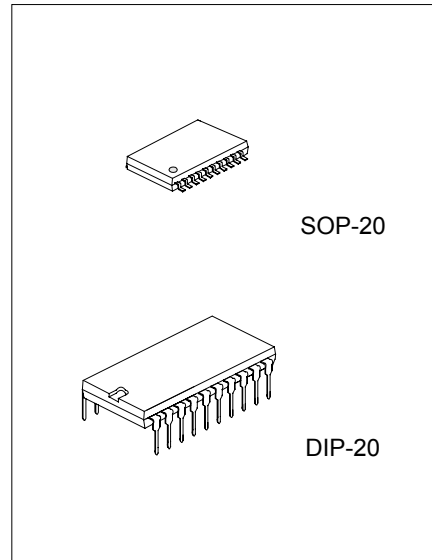
The UTC 75323 combines five drivers and three receivers. The flow-through design of the UTC 75323 decreases the part count, reduces the board space required, and allows easy interconnection of the UART and serial-port connector. The all-bipolar circuits and processing of the UTC 75323 provide a rugged, low-cost solution for this function.

The UTC 75323 complies with the requirements of the ANSI TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signal rates up to 20 Kbit/s. The switching speeds of the UTC 75323 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of ANSI Standard TIA/EIA-423-B and TIA/EIA-422-B and ITU Recommendations V.10 and V.11 are recommended.

The UTC 75323 is characterized for operation over a temperature range of 0°C to 70°C.

#### FEATURES

- \*Single Chip With Easy Interface Between UART and Serial-Port Connector of an External Modem or Other Computer Peripheral
- \*Five Drivers and Three Receivers Meet or Exceed the Requirements of ANSI Standard TIA/EIA-232-F and ITU Recommendation V.28 Standards.
- \*Supports Data Rates up to 120 kbit/s.
- \*Complement to the UTC 75232.



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# UTC

UNISONIC TECHNOLOGIES CO., LTD.

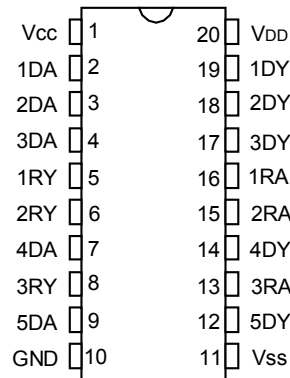
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QW-R113-007.A

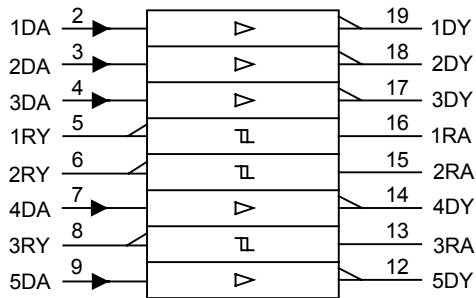
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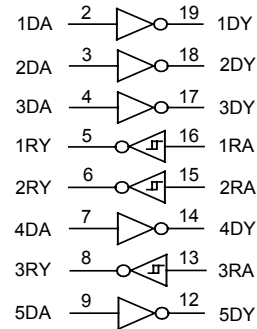
## PIN CONFIGURATION



## LOGIC SYMBOL \*



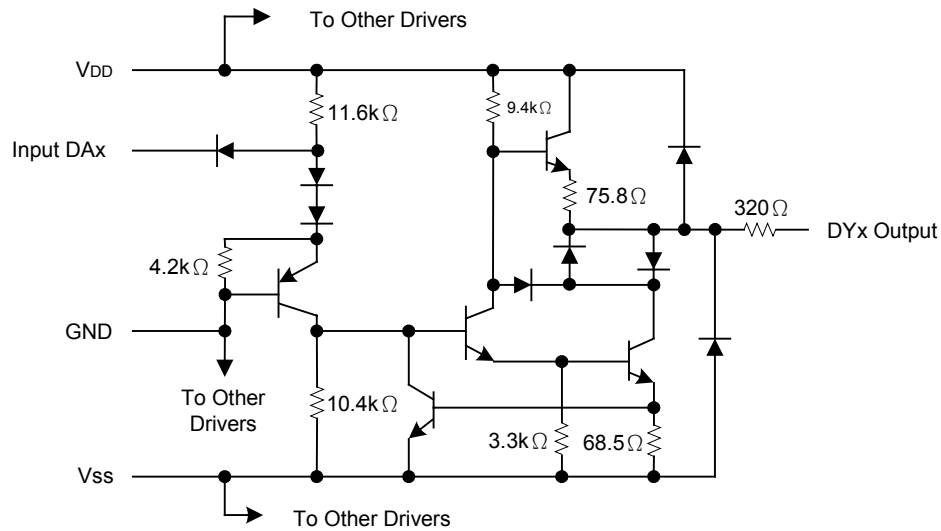
## LOGIC DIAGRAM ( POSITIVE LOGIC )



\* This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

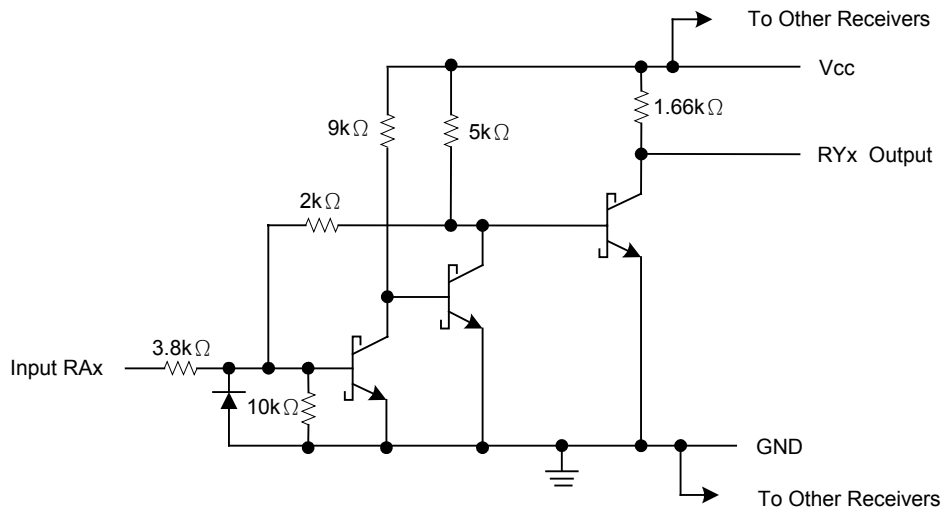
# UTC 75323 LINEAR INTEGRATED CIRCUIT

## SCHEMATIC (EACH DRIVER)



Resistor values shown are nominal.

## SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage (see Note 1)	Vcc	10	V
Supply voltage (see Note 1)	VDD	15	V
Supply voltage (see Note 1)	Vss	-15	V
Input voltage range: Driver	Vi	-15 ~ 7	V
Receiver		-30 ~ 30	
Output voltage range, (Driver)	Vo	-15 ~ 15	V
Low-level output current (Receiver)	IOL	20	mA
Package thermal impedance	θ JA	97	°C/W
SOP-20		67	
DIP-20			
Lead temperature 1.6mm(1/6 inch) from case for 10 seconds	Tlead	260	°C
Storage temperature range	Tstg	-65 ~ 150	°C

note: 1. All voltages are with respect to the network ground terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	VDD	7.5	9	13.5	V
	Vss	-7.5	-9	-13.5	
	Vcc	4.5	5	5.5	
High-level input voltage	Driver	VIH	1.9		V
Low-level input voltage	Driver	VIL		0.8	V
High-level output current	Driver	IOH		-6	mA
	Receiver			-0.5	
High-level output current,	Driver	IOL		6	mA
	Receiver			16	
Operating free-air temperature	Ta	0		70	°C

SUPPLY CURRENTS OVER OPERATING FREE-AIR TEMPERATURE RANGE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply current from VDD	IDD	All inputs at 1.9V, No load	VDD=9V, Vss=-9V	25	mA
			VDD=12V, Vss=-12V	32	
		All inputs at 0.8V, No load	VDD=9V, Vss=-9V	7.5	mA
			VDD=12V, Vss=-12V	9.5	
Supply current from Vss	ISS	All inputs at 1.9V, No load	VDD=9V, Vss=-9V	-25	mA
			VDD=12V, Vss=-12V	-32	
		All inputs at 0.8V, No load	VDD=9V, Vss=-9V	-5.3	mA
			VDD=12V, Vss=-12V	-5.3	
Supply current from Vcc	ICC	Vcc=5V, All inputs at 5V, No load		20	mA

ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE,  $V_{DD}=9V, V_{SS}=-9V, V_{CC}=5V$  (UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	$V_{OH}$	$V_{IL}=0.8V, R_L=3k\Omega$ (See Figure 1)	6	7.5		V
Low-level output voltage(see Note 2)	$V_{OL}$	$V_{IH}=1.9V, R_L=3k\Omega$ (See Figure 1)		-7.5	-6	V
High-level Input current	$I_{IH}$	$V_i=5V$ (See Figure 2)			10	$\mu A$
Low-level input current	$I_{IL}$	$V_i=0$ (See Figure 2)			-1.6	mA
High-level short-circuit output current (see Note 3)	$I_{OS(H)}$	$V_{IL}=0.8V, V_o=0$ (See Figure 1)	-4.5	-9	-19.5	mA
Low-level short-circuit output current	$I_{OS(L)}$	$V_{IH}=2V, V_o=0$ (See Figure 1)	4.5	9	19	mA
Output resistance (see Note 4)	$r_o$	$V_{CC}=V_{DD}=V_{SS}=0, V_o=-2V$ to 2V	300			$\Omega$

- Notes: 2. The algebraic convention, where the more positive(less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10V is maximum, the typical value is a more negative voltage.  
 3. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.  
 4. Test conditions are those specified by TIA/EIA-232-F and as listed above.

SWITCHING CHARACTERISTICS ( $T_a=25^\circ C, V_{DD}=12V, V_{SS}=-12V, V_{CC}=5V \pm 10\%$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time, low- to high-level output	$t_{PLH}$	$R_L=3k\Omega$ to $7k\Omega, C_L=15pF$ (See Figure 3)		315	500	ns
Propagation delay time, high-to low-level output	$t_{PHL}$			75	175	
TTLH Transition time, low-to high-level output	$t_{TLH}$	$R_L=3k\Omega$ to $7k\Omega, C_L=15pF$ (See Figure 3)		60	100	ns
		$R_L=3k\Omega$ to $7k\Omega, C_L=2500pF$ (See Figure 3 and Note 5)		1.7	2.5	$\mu s$
Transition time, high-to low-level output	$t_{THL}$	$R_L=3k\Omega$ to $7k\Omega, C_L=15pF$ (See Figure 3)		40	75	ns
		$R_L=3k\Omega$ to $7k\Omega, C_L=2500pF$ (See Figure 3 and Note 6)		1.5	2.5	$\mu s$

- Note: 5. Measured between -3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.  
 6. Measured between 3-V and -3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP*	MAX	UNIT	
Positive-going input threshold voltage	$V_{IT+}$	See Figure 5	$T_a=25^\circ C$	1.75	1.9	2.3	V
			$T_a=0^\circ C$ to $70^\circ C$	1.55		2.3	
Negative-going input threshold voltage	$V_{IT-}$	See Figure 5	0.75	0.97	1.25	V	
Input hysteresis voltage( $V_{IT+} - V_{IT-}$ )	$V_{Hys}$		0.5				
High-level output voltage	$V_{OH}$	$I_{OH}=-0.5mA$	$V_{IH}=0.75V$	2.6	4	5	V
			Inputs open	2.6			
Low-level output voltage	$V_{OL}$	$I_{OL}=10mA, V_i=3V$		0.2	0.45	V	
High-level input current	$I_{IH}$	$V_i=25V$	3.6		8.3	dB	
		$V_i=3V$	0.43			mA	
Low-level input current	$I_{IL}$	$V_i=-25V$	-3.6		-8.3	mA	
		$V_i=-3V$	-0.43			mA	
Short-circuit output current	$I_{OS}$	See Figure 4		-3.4	-12	mA	

\* All typical values are at  $T_a=25^\circ C, V_{CC}=5V, V_{DD}=9V, V_{SS}=-9V$

SWITCHING CHARACTERISTICS (Ta=25°C, VCC=5V, VDD=12V, VSS= -12V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time, low-to high-level output	t <sub>PLH</sub>	CL=50pF, RL=5kΩ		107	500	ns
Propagation delay time, high- to low-level output	t <sub>PHL</sub>	See Figure 6		42	150	ns
Transition time, low-to high-level output	t <sub>TLH</sub>			175	525	ns
Transition time, high- to low-level output	t <sub>THL</sub>			16	60	ns

PARAMETER MEASUREMENT INFORMATION

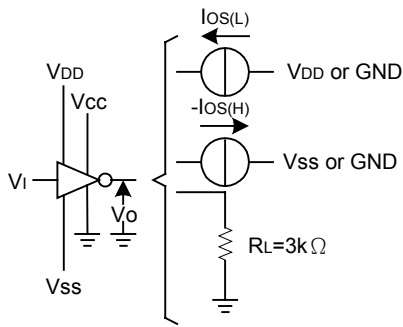


Figure 1. Driver Test Circuit for  $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(H)}$ , and  $I_{OS(L)}$

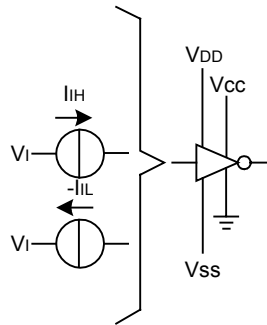
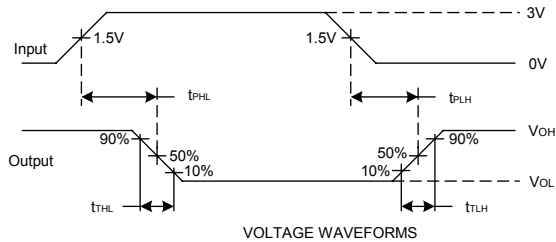
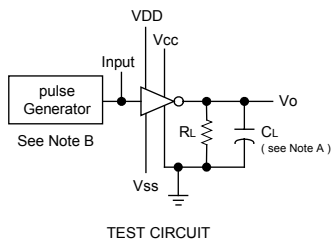


Figure 2. Driver Test Circuit for  $I_{iH}$  and  $I_{iL}$



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics ( $t_w=25\mu s$ ,  $PRR=20kHz$ ,  $Z_o=50\Omega$ ,  $t_r<tf<50ns$ )

Figure 3. Driver Test Circuit and Voltage Waveforms

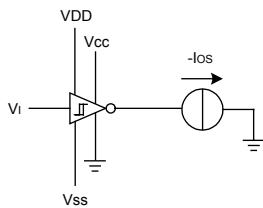


Figure 4. Receiver Test Circuit for  $I_{OS}$

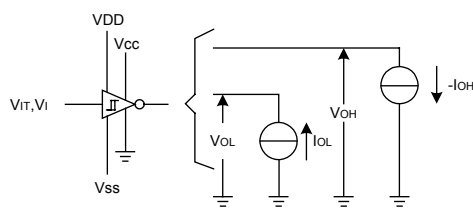
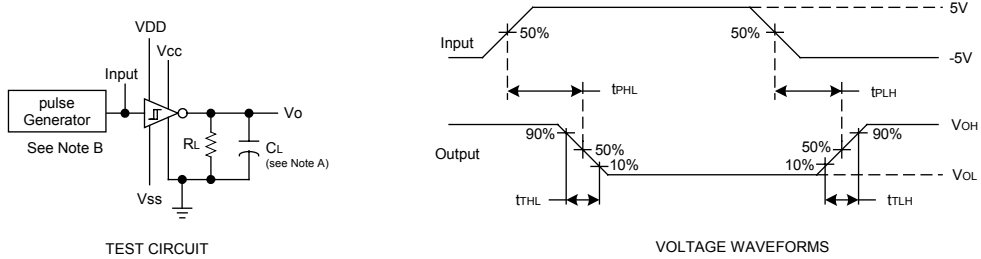


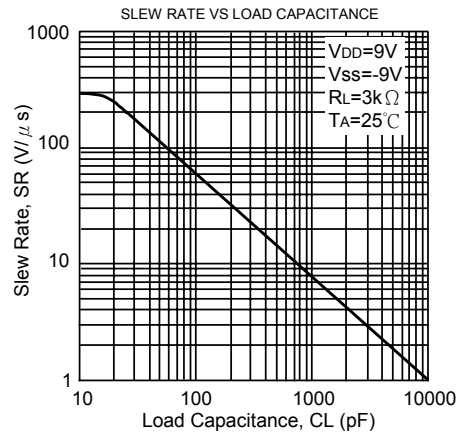
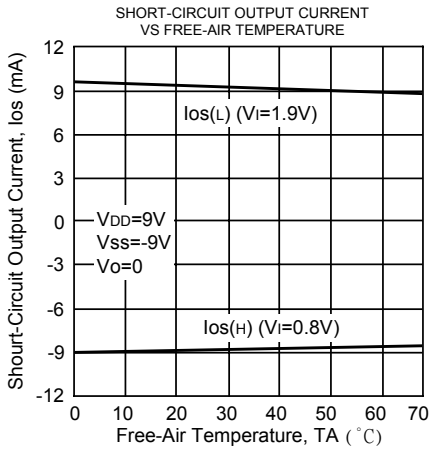
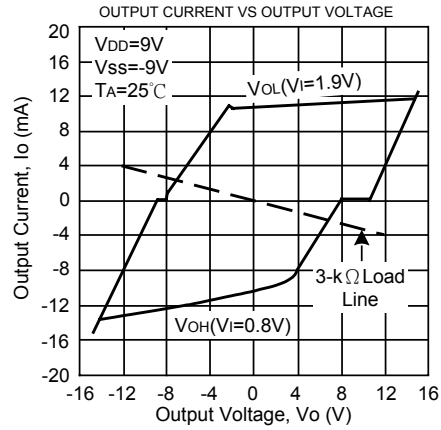
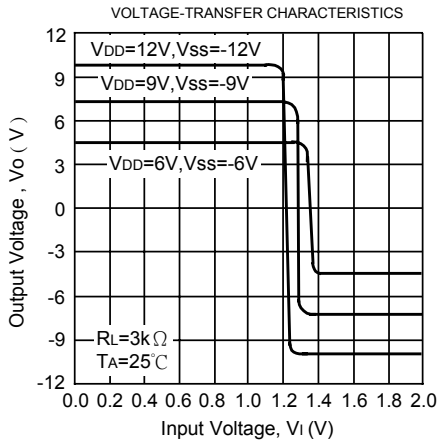
Figure 5. Receiver Test Circuit for  $V_{IT}$ ,  $V_{OH}$ , and  $V_{OL}$

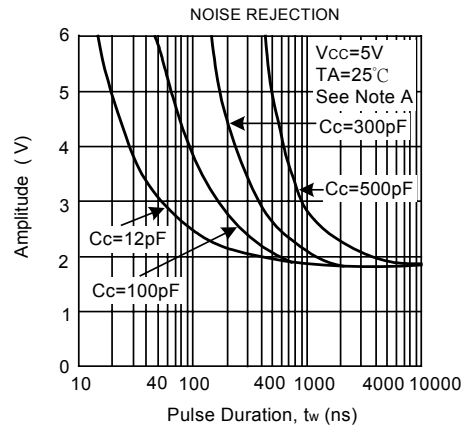
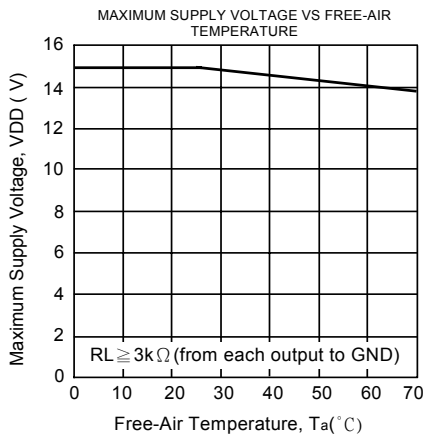
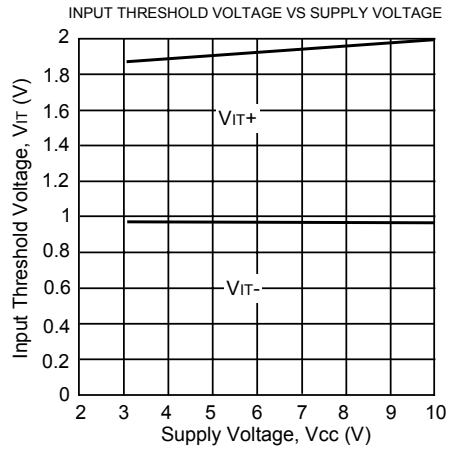
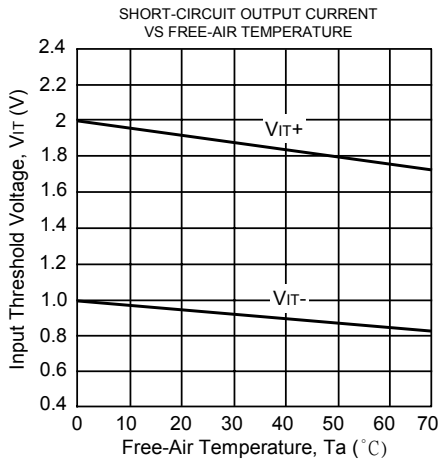


NOTES: A. CL includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics ( $t_w=25\mu s$ , PRR=20kHz,  $Z_o=50\Omega$ ,  $t_r<50ns$ )

Figure 6. Receive Propagation and Transition Times

TYPICAL CHARACTERISTICS DRIVER SECTION





NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0V, does not cause a change of the output level.



# UTC 75323 LINEAR INTEGRATED CIRCUIT

## APPLICATION INFORMATION

Diodes placed in series with the V<sub>DD</sub> and V<sub>SS</sub> leads protect the UTC GD75323 in the fault condition in which the device output are shorted to V<sub>DD</sub> or V<sub>SS</sub>, and the Power supplies are at low and provide low-impedance paths to ground(see Figure 15)

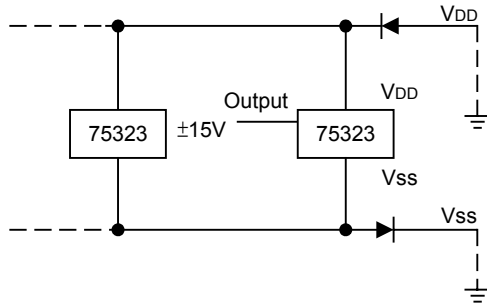
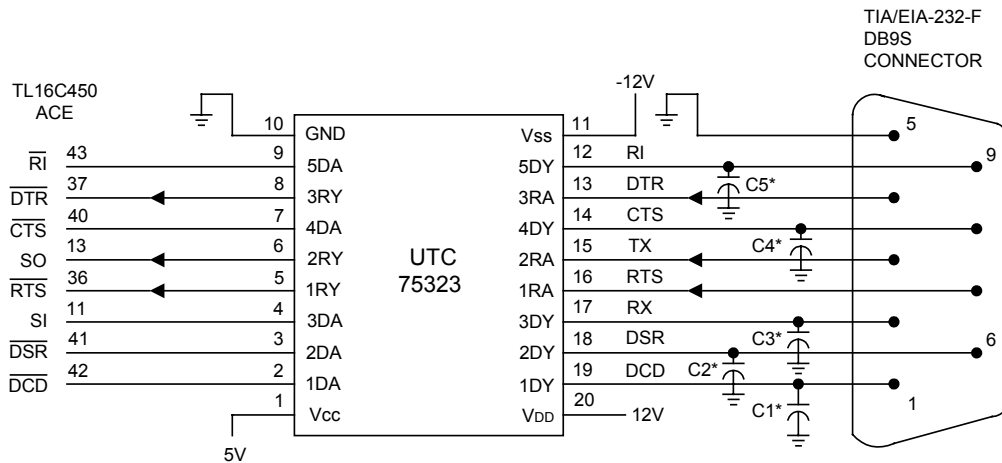


Figure 7. Power-Supply Protection to Meet Power-Off Fault Condition of TIA/EIA-232-F



\*See Figure10 to select the correct values for the loading capacitors(C1,C2,C3,C4 and C5),which may be required to meet the RS-232 maximum slew-rate requirement of 30V/us.The value of the loading capacitors res required depends upon the line length and desired slew rate,but is typically 330pF.

NOTE C:To use the receivers only,V<sub>DD</sub> and V<sub>SS</sub> both must be powered or tied to ground.

Figure 8. Typical Connection

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