CS5333

24-Bit, 96 kHz Stereo A/D Converter

Features

- 24-bit conversion
- Supports 96 kHz sample rates
- 98 dB dynamic range at 3 V supply
- -88 dBFS THD+N
- 1.8 to 3.3 volt supply
- 16-Pin TSSOP package
- Low power consumption
  - 11 mW at 1.8 V
- Internal high pass filter to remove DC offsets
- Linear phase digital anti-alias filter

Description

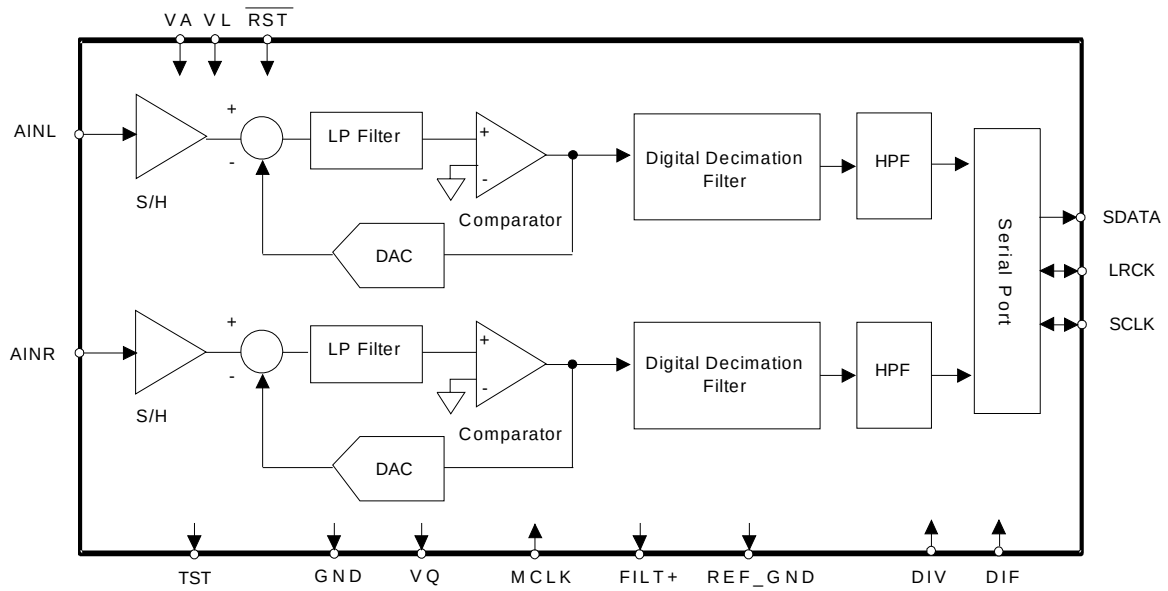
The CS5333 is a highly integrated, 24-bit, 96 kHz audio ADC providing stereo analog-to-digital converters using delta-sigma conversion techniques. This device includes line level inputs in a 16-pin TSSOP package.

The CS5333 is based on delta-sigma modulation allowing infinite adjustment of the sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

The CS5333 operates from a +1.8 V to +3.3 V supply. These features are ideal for set-top boxes, A/V receivers, DVD-karaoke players or any system which requires optimal performance in a minimum of space.

ORDERING INFORMATION

CS5333-KZ	-10 to 70° C	16-pin TSSOP
CDB5333		Evaluation Board



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25° C; GND = 0 V Logic "1" = VL = 1.8 V; Logic "0" = GND = 0 V; MCLK = 12.288 MHz; Fs for Base-rate Mode = 48 kHz, SCLK = 3.072 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for High-Rate Mode = 96 kHz, SCLK = 6.144 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter	Symbol	Base-rate Mode			High-rate Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics for VA = 1.8 V								
Dynamic Range A-weighted		TBD	91	-	TBD	94	-	dB
unweighted		TBD	88	-	TBD	91	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
-1 dB		-	-88	TBD	-	-88	TBD	dB
-20 dB		-	-68	-	-	-68	-	dB
-60 dB		-	-28	-	-	-31	-	dB
Analog Input Characteristics for VA = 3.0 V								
Dynamic Range A-weighted		TBD	96	-	TBD	98	-	dB
unweighted		TBD	93	-	TBD	95	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
-1 dB		-	-88	TBD	-	-85	TBD	dB
-20 dB		-	-68	-	-	-65	-	dB
-60 dB		-	-33	-	-	-35	-	dB
Analog Input Characteristics for VA = 1.8 or 3.0 V								
Interchannel Isolation 1 kHz		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Error with High Pass Filter		-	-	0	-	-	0	LSB
Full Scale Input Voltage		TBD	VA÷3.6	TBD	TBD	VA÷3.6	TBD	Vrms
Voltage Common Mode			VA÷2			VA÷2		V
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF

Notes: 1. Referenced to typical full-scale differential input voltage.

ANALOG CHARACTERISTICS (Continued)

Parameter			Symbol	Base-rate Mode Min	Typ	Max	High-rate Mode Min	Typ	Max	Unit
A/D Decimation Filter Characteristics (Note 2)										
Passband		(Note 3)		0	-	23.5	0	-	47.5	kHz
Passband Ripple				-0.08	-	+0.17	-0.09	-	0	dB
Stopband		(Note 3)		27.5	-	-	64.1	-	-	kHz
Stopband Attenuation		(Note 4)		-60.3	-	-	-48.4	-	-	dB
Group Delay (Fs = Output Sample Rate)		(Note 5)	t_{gd}	-	10/Fs	-	-	2.7/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0.03	-	-	0.007	µs
High Pass Filter Characteristics										
Frequency Response	-3 dB	(Note 3)		-	3.7	-	-	3.7	-	Hz
	-0.1 dB			-	24.2	-	-	24.2	-	Hz
Phase Deviation	@ 20 Hz	(Note 3)		-	10	-	-	10	-	Degree
Passband Ripple		(Note 2)		-	-	0.17	-	-	0.09	dB

Notes:
2. Filter response is guaranteed by design.
3. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.
4. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).
5. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312 µs.

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Units
Power Supplies									
Power Supply Current-	VA=1.8 V	I_A	-	6.0	-	-	7.6	-	mA
Normal Operation	VL=1.8 V	I_{D_IO}	-	150	-	-	300	-	µA
Power Supply Current-	VA=1.8 V	I_A	-	100	-	-	250	-	µA
Power Down Mode (Note 7)	VL=1.8 V	I_{D_IO}	-	0	-	-	0	-	µA
Power Supply Current-	VA=3.0 V	I_A	-	9	-	-	11.5	-	mA
Normal Operation	VL=3.0 V	I_{D_IO}	-	260	-	-	520	-	µA
Power Supply Current-	VA=3.0 V	I_A	-	250	-	-	500	-	µA
Power Down Mode	VL=3.0 V	I_{D_IO}	-	0	-	-	0	-	µA
Total Power Dissipation-	All Supplies=1.8 V		-	11	TBD	-	14.5	TBD	mW
Normal Operation	All Supplies=3.0 V		-	28	TBD	-	36	TBD	mW
Package Thermal Resistance		θ_{JA}	-	75	-	-	75	-	°C/Watt
Power Supply Rejection Ratio	(1 kHz)	PSRR	-	60	-	-	60	-	dB
(Note 6)	(60 Hz)		-	40	-	-	40	-	dB

Notes: 6. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 3.

7. Power Down Mode is defined as reset active with MCLK being applied. To lower power consumption further, remove MCLK.

DIGITAL CHARACTERISTICS (T_A = 25° C; VL = 1.7 V - 3.6 V; GND = 0 V)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7•VL	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.3•VL	V
High-Level Output Voltage	V_{OH}	0.7•VL	-	-	V
Low-Level Output Voltage	V_{OL}	-	-	0.3•VL	V
Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

ABSOLUTE MAXIMUM RATINGS (GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA	-0.3	4.0	V
	Digital I/O	VL	-0.3	4.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
Ambient Temperature		T_A	-10	-	70	°C
DC Power Supplies:	Positive Analog	VA	1.7	-	3.6	V
	Digital I/O	VL	1.7	-	3.6	V

SWITCHING CHARACTERISTICS (T_A = -10 to 70° C; VL = 1.7 V - 3.6 V; Inputs: Logic 0 = GND, Logic 1 = VL, C_L = 20 pF)

Parameters		Symbol	Min	Typ	Max	Units
Input Sample Rate	Base Rate Mode	Fs	2	-	50	kHz
	High Rate Mode	Fs	50	-	100	kHz
MCLK Pulse Width High	MCLK/LRCK = 1024		8	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 1024		8	-	-	ns
MCLK Pulse Width High	MCLK/LRCK = 768		10	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 768		10	-	-	ns
MCLK Pulse Width High	MCLK/LRCK = 512		15	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 512		15	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 384 or 192		21	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 384 or 192		21	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 256 or 128		31	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 256 or 128		31	-	-	ns
Master Mode						
SCLK Falling to LRCK Edge		t_{slrd}	-20	-	20	ns
SCLK Falling to SDATA Valid		t_{sdo}	0	-	20	ns
SCLK Duty Cycle			40	50	60	%
Slave Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period	Base Rate Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
	High Rate Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK Falling to LRCK Edge		t_{slrd}	-20	-	20	ns
SCLK Falling to SDATA Valid	Base Rate Mode	t_{dss}	-	-	$\frac{1}{(512)Fs}$	ns
	High Rate Mode	t_{dss}	-	-	$\frac{1}{(256)Fs}$	ns

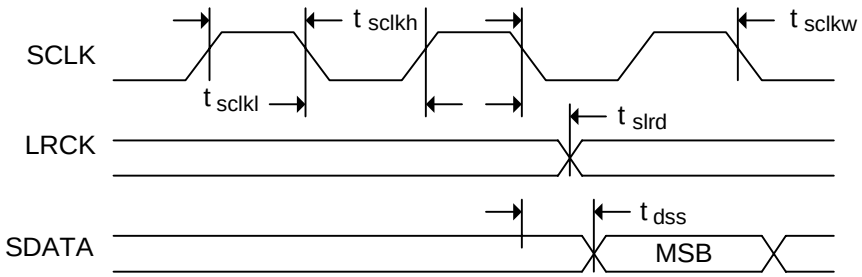


Figure 1. SCLK to LRCK and SDATA, Slave Mode

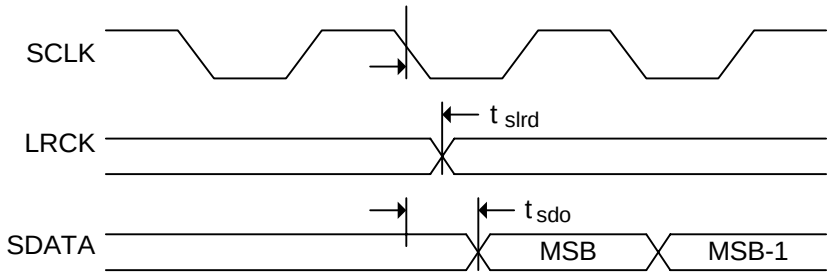


Figure 2. SCLK to LRCK and SDATA, Master Mode

2. TYPICAL CONNECTION DIAGRAM

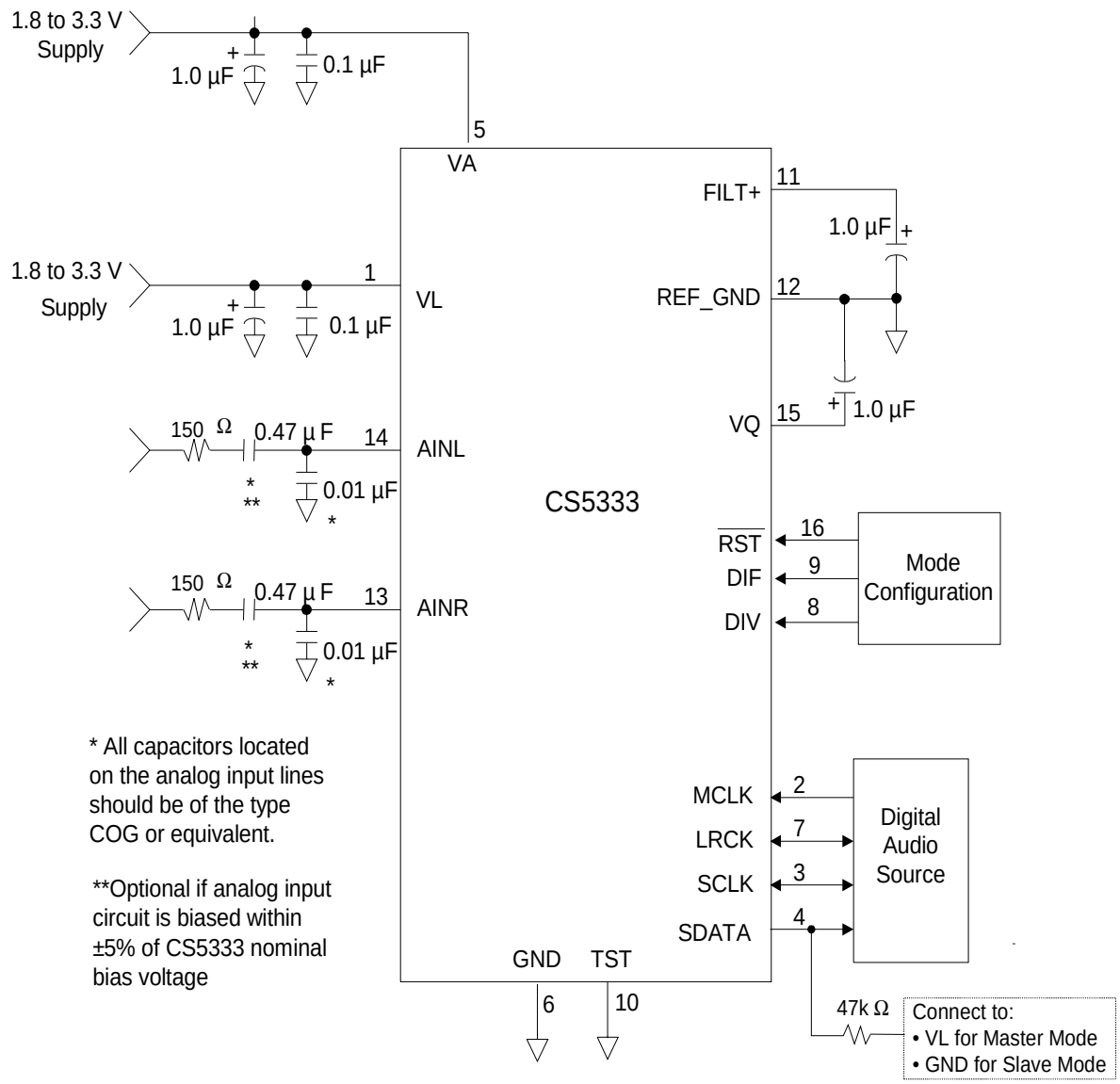
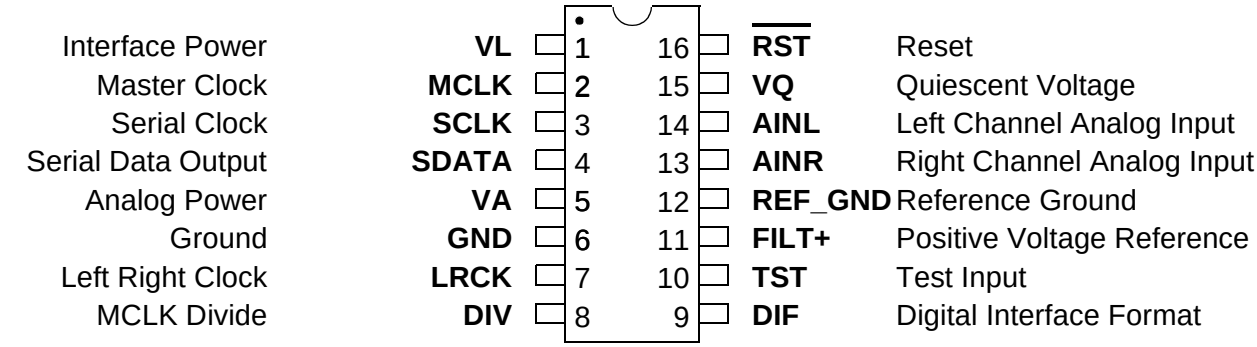


Figure 3. Typical Connection Diagram

3. PIN DESCRIPTION



Interface Power	1	**VL** (*Input*) - Digital interface power supply. Typically 1.8 to 3.3 VDC.
Master Clock	2	**MCLK** (*Input*) - The master clock frequency must be either 256x, 384x, 512x, 768x or 1024x the input sample rate in Base Rate Mode (BRM) and 128x, 192x, 256x, 384x the input sample rate in High Rate Mode (HRM). Table 1 illustrates several standard audio sample rates and the required master clock frequencies.
Serial Clock	3	**SCLK** (*Input*/*Output*) - Clocks the individual bits of the serial data out of the SDOUT pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF pin.
Serial Audio Data Out (M/S select)	4	**SDATA** (*Output*) - This pin serves two functions. First: two's complement MSB-first serial data is output on this pin. The data is clocked out of SDOUT via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF pin. Second: Master/Slave mode selection is determined, at startup, by a 47 kOhm pullup/pull-down on this line. A pullup to VL selects Master mode and a pulldown to GND selects Slave mode.
Analog Power	5	**VA** (*Input*) - Analog power supply. Typically 1.8 to 3.3 VDC.
Ground	6	**GND** (*Input*) - Ground Reference.

Sample Rate (kHz)	MCLK (MHz)								
	HRM				BRM				
	128x	192x	256x*	384x*	256x	384x	512x	768x*	1024x*
32	4.0960	6.1440	8.1920	12.2880	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	5.6448	8.4672	11.2896	16.9344	11.2896	16.9344	22.5792	32.7680	45.1584
48	6.1440	9.2160	12.2880	18.4320	12.2880	18.4320	24.5760	36.8640	49.1520
64	8.1920	12.2880	16.3840	24.5760	-	-	-	-	-
88.2	11.2896	16.9344	22.5792	33.8688	-	-	-	-	-
96	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-

** DIV= Hi*

Table 1. Common Clock Frequencies

Left/Right Clock	7	**LRCK** (*Input*/*Output*) - The Left/Right clock determines which channel is currently being output on the serial audio data line SDOUT. The frequency of the Left/Right clock must be at the input sample rate. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF pin.
MCLK Divide Enable	8	**DIV** (*Input*) **-** This pin serves different functions in Master and Slave modes. In Master mode: When high, the chip will enter High Rate Mode; When this pin is low, the chip will enter Base Rate Mode. In Slave mode: When high, MCLK is divided internally by 2; When low, MCLK is not changed.
Digital Interface Format	9	**DIF** (*Input*) **-** The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format.

DIF	DESCRIPTION
0	I^2S, up to 24-bit data
1	Left Justified, up to 24-bit data

Table 2. Digital Interface Format - DIF

Test Input	10	**TST** (*Input*) - Must be connected directly to ground.
Positive Voltage Reference	11	**FILT+** (*Output)* - Positive reference for internal sampling circuits. An external capacitor is required from FILT+ to ground, as shown in Figure 3. The recommended value will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 60 Hz. FILT+ is not intended to supply external current. FILT+ has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.
Reference Ground	12	**REF_GND** (*Input*) - Ground reference for the internal sampling circuits. Must be connected to ground.
Analog Inputs	13,14	**AINR, AINL** (*Input*) **-** The full scale analog input level is specified in the Analog Characteristics specification table.
Quiescent Voltage	15	**VQ** (*Output*) - Filter connection for internal A/D converter quiescent reference voltage. A capacitor must be connected from VQ to ground. VQ is not intended to supply external current. VQ has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.
Reset	16	**$\overline{\text{RST}}$** (*Input*) - When low the device enters a low power mode and the part is in reset. When high, the part returns to normal operation within 1024 LRCK cycles.

4. APPLICATIONS

4.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5333 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 show the recommended power arrangement with VA and VL connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible.

4.2 Oversampling Modes

The CS5333 operates in one of two oversampling modes. Base Rate Mode supports input sample rates up to 50 kHz while High Rate Mode supports input sample rates up to 100 kHz. See Table 1 for more details.

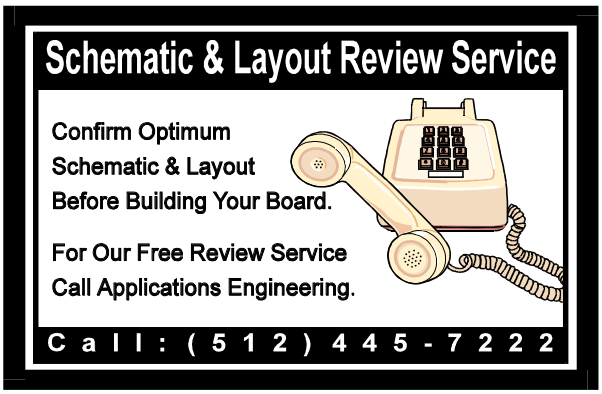
4.3 Recommended Power-up Sequence

1) Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, VQ will remain low.

2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low and will initiate the power-up sequence. This power-up sequence takes approximately 1024 LRCK cycles to complete.

4.4 Master/Slave Mode

In Master, Base Rate Mode (Pull-up on SDATA, DIV=0), the CS5333 requires a 256x MCLK and provide a 64x SCLK. In Master, High Rate Mode (Pull-up on SDATA, DIV=1), the CS5333 requires a 128x MCLK and provide a 64x SCLK. The various clocking ratios required in Slave Mode (Pull-down on SDATA) are listed under the description of MCLK, on page 11.



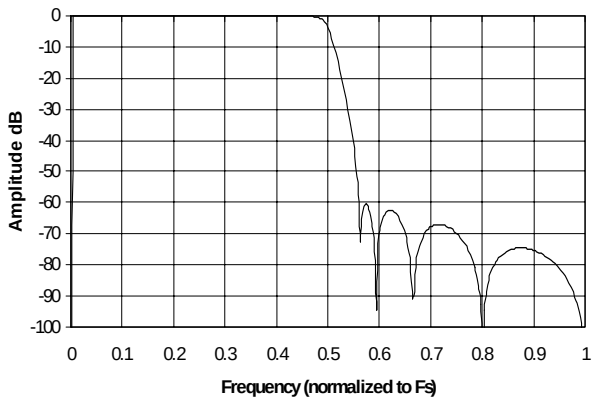


Figure 4. Base-Rate Stopband Rejection

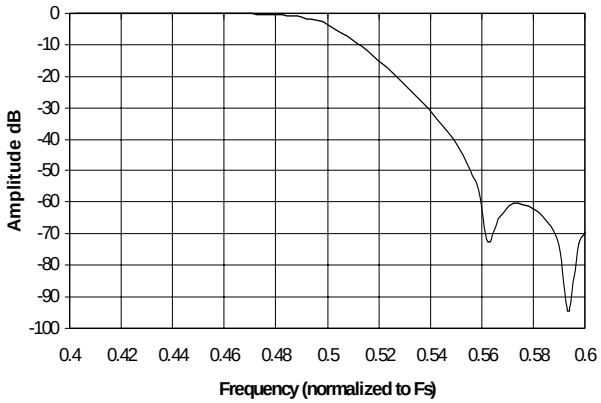


Figure 5. Base-Rate Transition Band

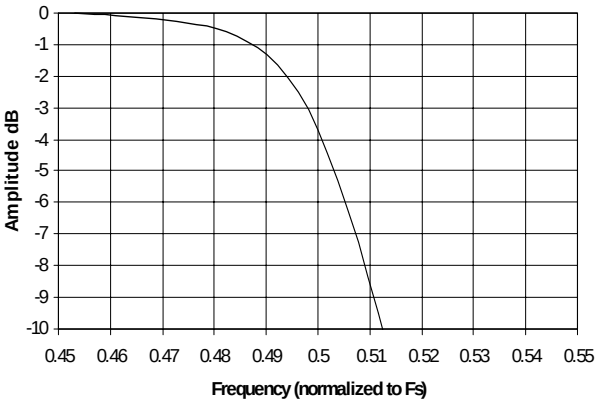


Figure 6. Base-Rate Transition Band (Detail)

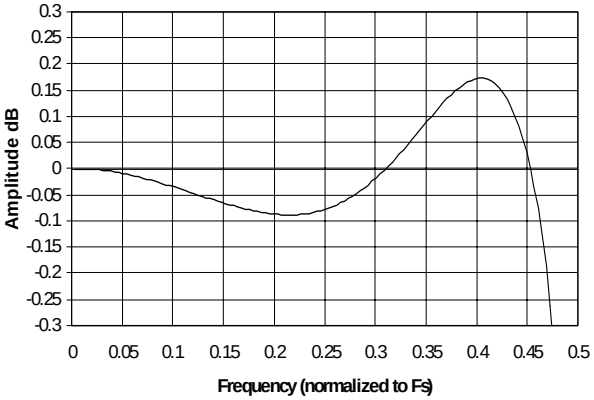


Figure 7. Base-Rate Passband Ripple

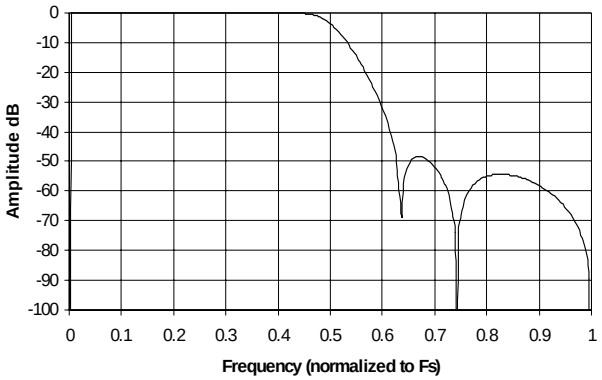


Figure 8. High-Rate Stopband Rejection

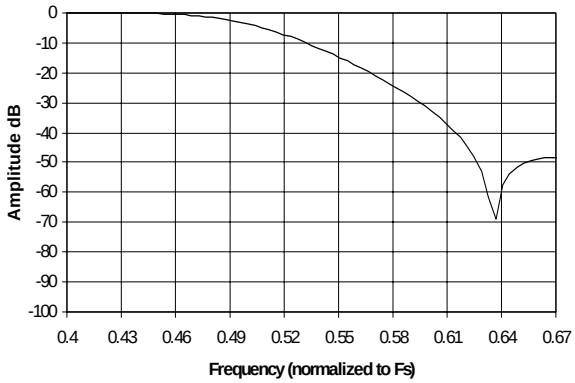


Figure 9. High-Rate Transition Band

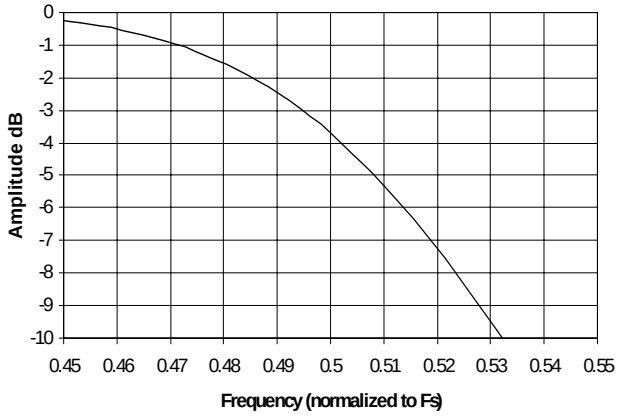


Figure 10. High-Rate Transition Band (Detail)

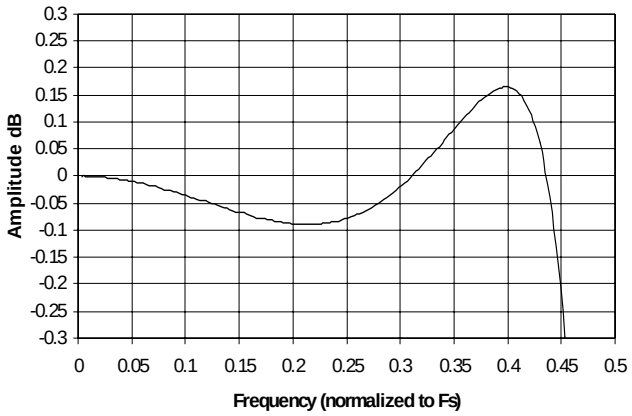


Figure 11. High-Rate Passband Ripple

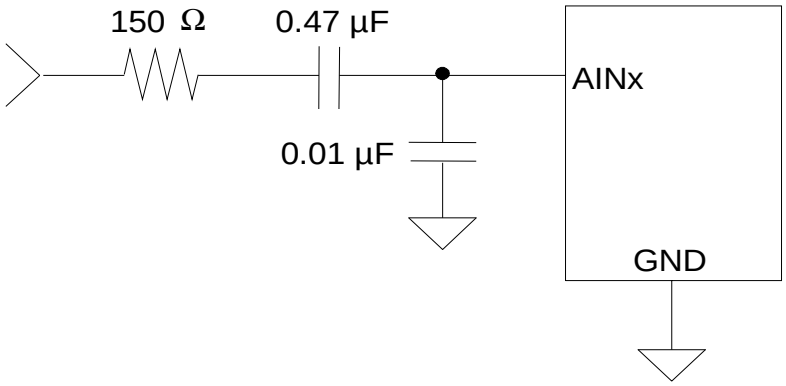
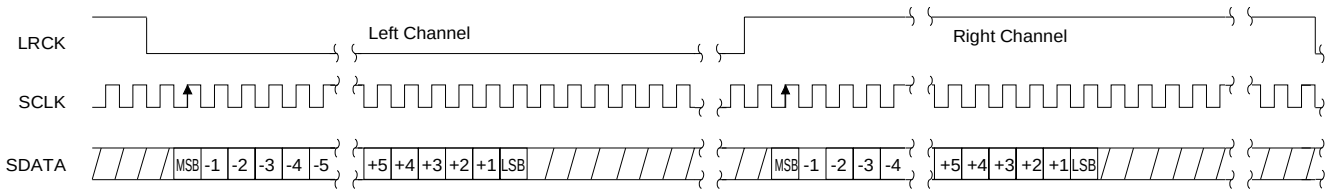
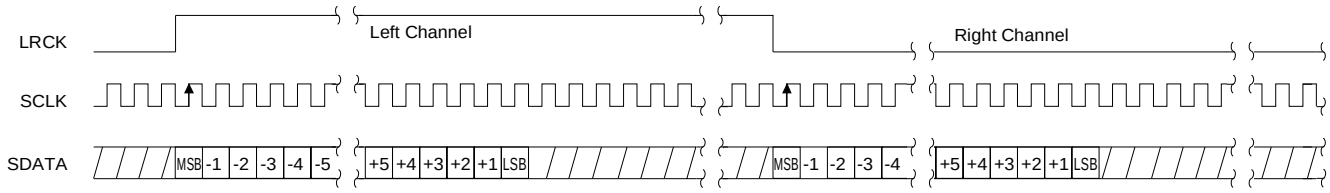


Figure 12. Line Input Test Circuit



I²S, up to 24-Bit Data. Data Valid on Rising Edge of SCLK

Figure 13. CS5333 - Serial Audio Format 0



Left Justified, up to 24-Bit Data. Data Valid on Rising Edge of SCLK.

Figure 14. CS5333 - Serial Audio Format 1

5. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

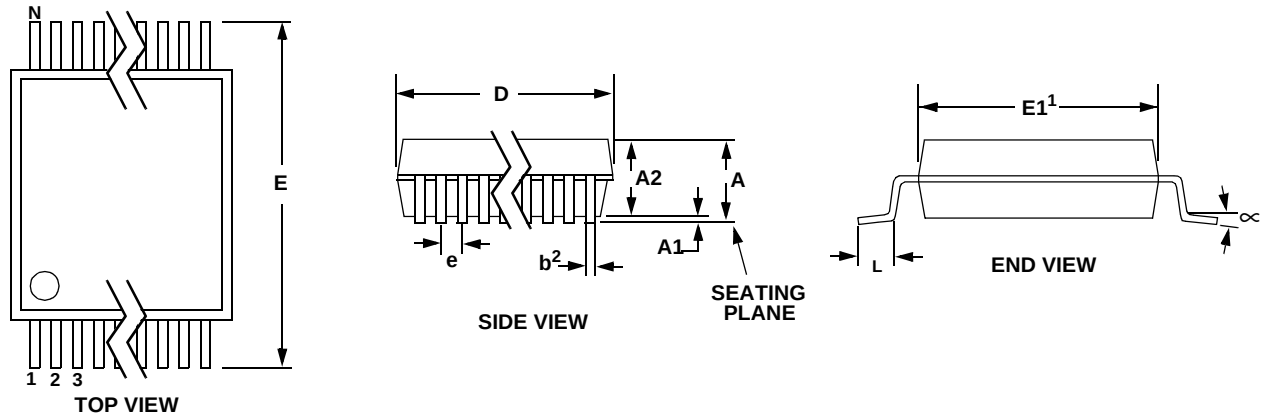
The change in gain value with temperature. Units in ppm/°C.

6. REFERENCES

1. "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
2. CDB5333 Evaluation Board Datasheet.

7. PACKAGE DIMENSIONS

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.065 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips

• Notes •


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