

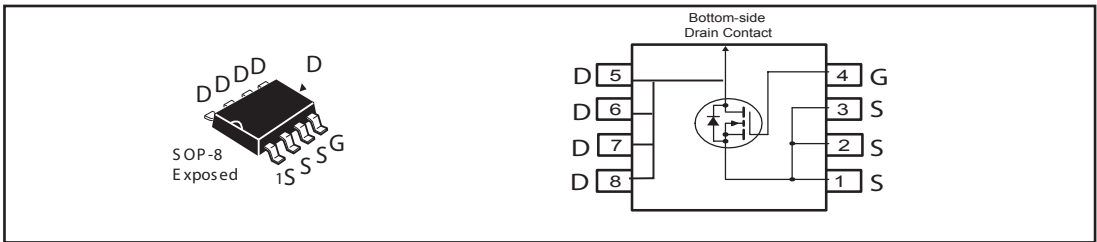


## N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> ( mΩ ) Typ
30V	13A	9 @ V <sub>GS</sub> = 10V
		13 @ V <sub>GS</sub> = 4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.
- Thermal Pad Exposed with Standard SOP-8 Outline



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous <sup>a</sup> @ T <sub>J</sub> =25°C -Pulsed <sup>b</sup>	I <sub>D</sub>	13	A
	I <sub>DM</sub>	40	A
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	1.7	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	3.0	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R <sub>θJA</sub>	40	°C/W
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ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	1	1.7	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A		9	12.5	m ohm
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A		13	18	m ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	10			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10A		25		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V f = 1.0MHz		2300		pF
Output Capacitance	C <sub>OSS</sub>			300		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			140		pF
Gate resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1.0MHz		3		ohm
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 15V I <sub>D</sub> = 1 A V <sub>GS</sub> = 10V R <sub>GEN</sub> = 6 ohm		21		ns
Rise Time	t <sub>r</sub>			20		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			75		ns
Fall Time	t <sub>f</sub>			17		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 12A, V <sub>GS</sub> = 10V		39.5		nC
		V <sub>DS</sub> = 15V, I <sub>D</sub> = 12A, V <sub>GS</sub> = 4.5V		17.5		nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 12A		5		nC
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>GS</sub> = 10V		7		nC

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## ELECTRICAL CHARACTERISTICS ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = 1.7A$		0.76	1.3	V

### Notes

a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .

b. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

c. Guaranteed by design, not subject to production testing.

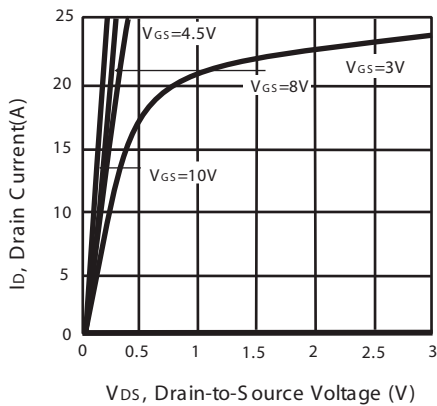


Figure 1. Output Characteristics

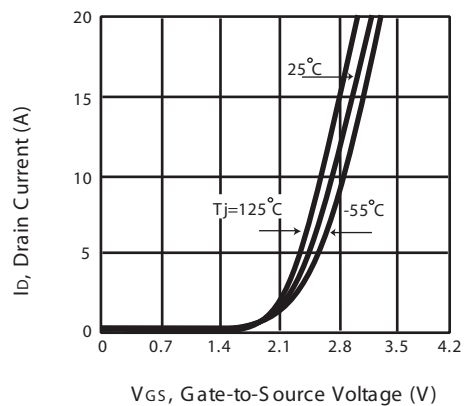


Figure 2. Transfer Characteristics

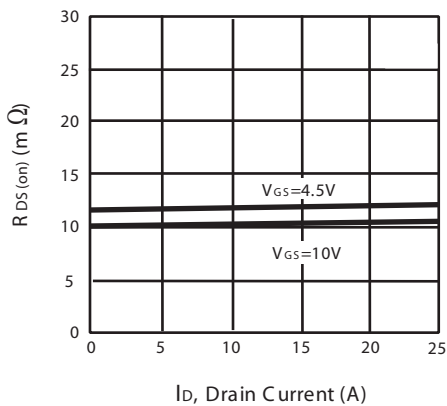


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

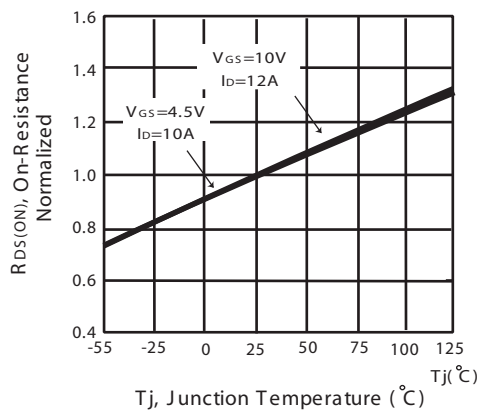


Figure 4. On-Resistance Variation with Drain Current and Temperature

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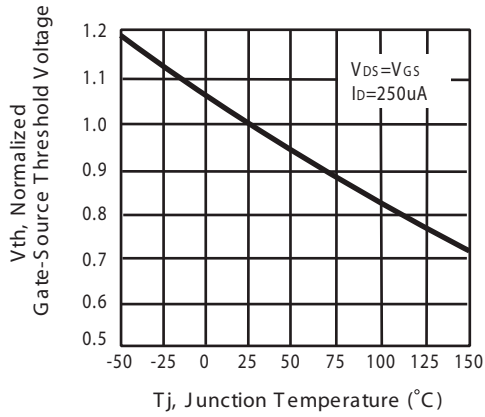


Figure 5. Gate Threshold Variation with Temperature

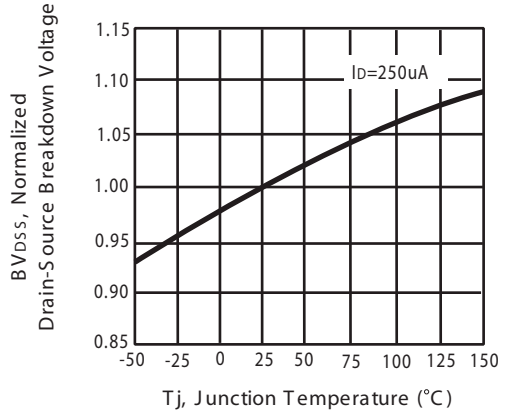


Figure 6. Breakdown Voltage Variation with Temperature

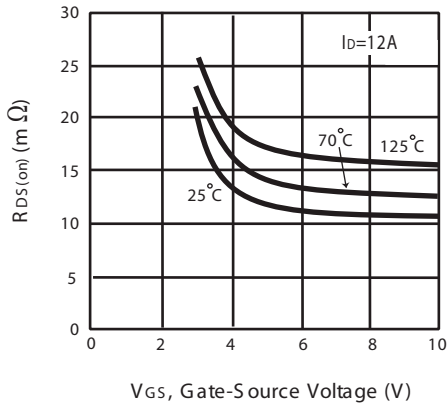


Figure 7. On-Resistance vs. Gate-Source Voltage

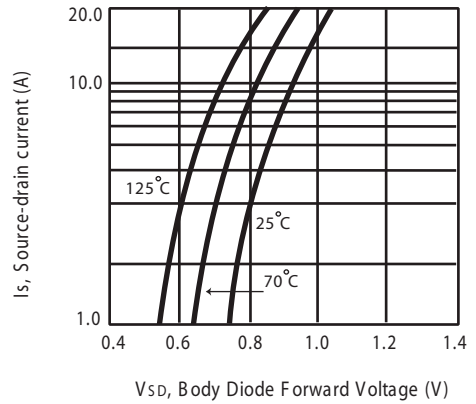


Figure 8. Body Diode Forward Voltage Variation with Source Current

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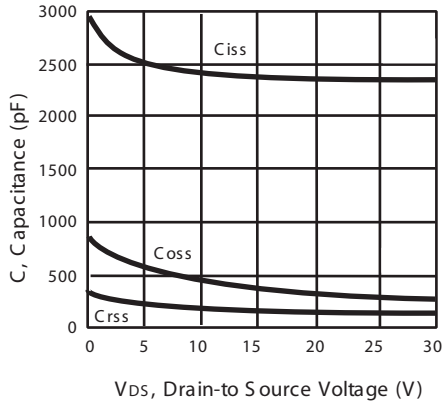


Figure 9. Capacitance

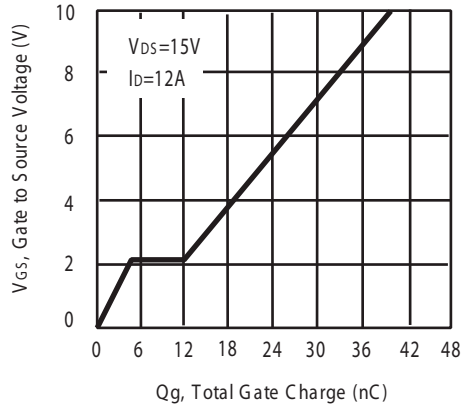


Figure 10. Gate Charge

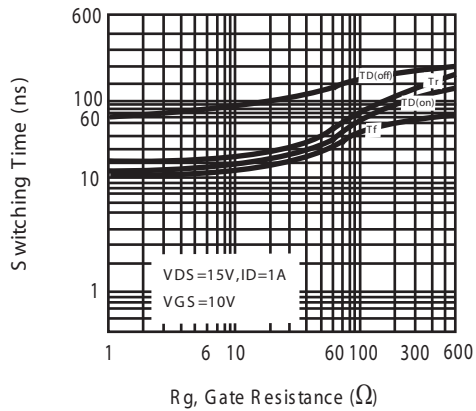


Figure 11. switching characteristics

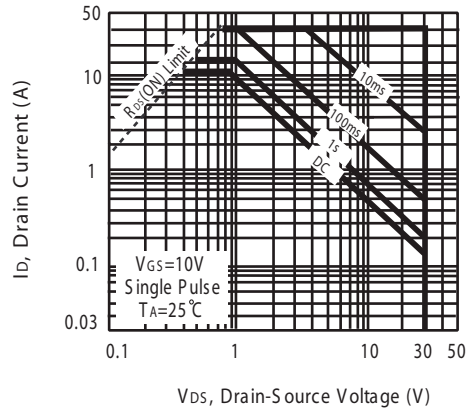


Figure 12. Maximum Safe Operating Area

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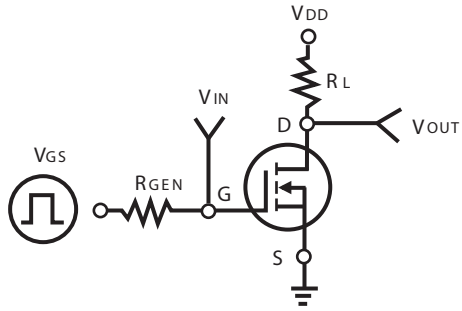


Figure 11. Switching Test Circuit

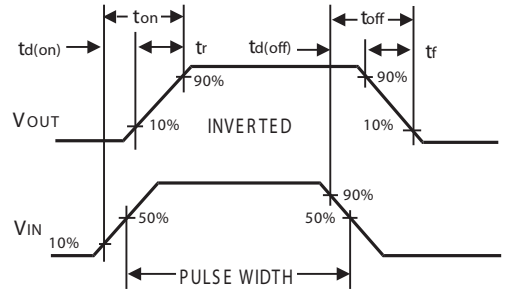
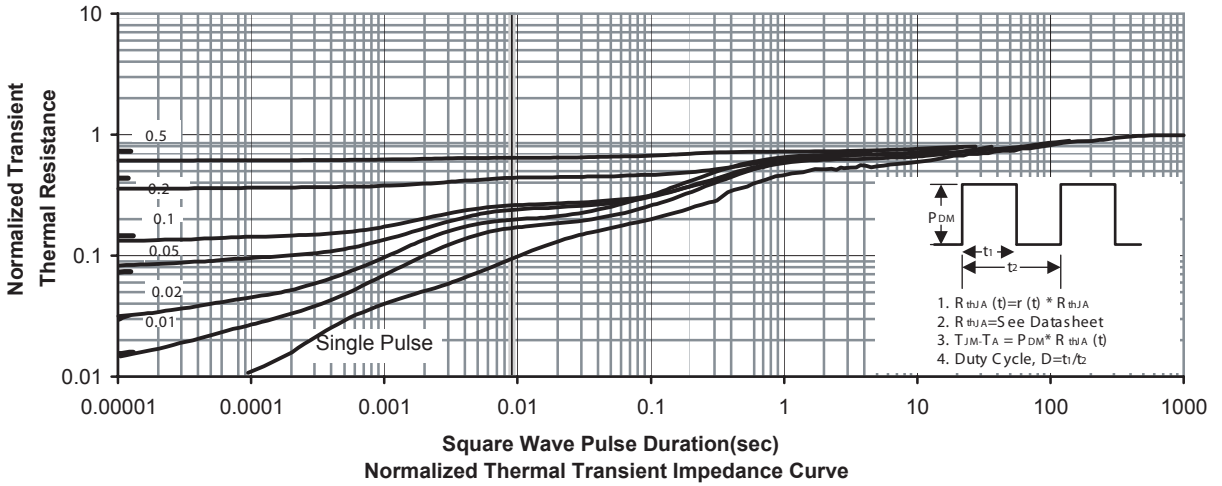


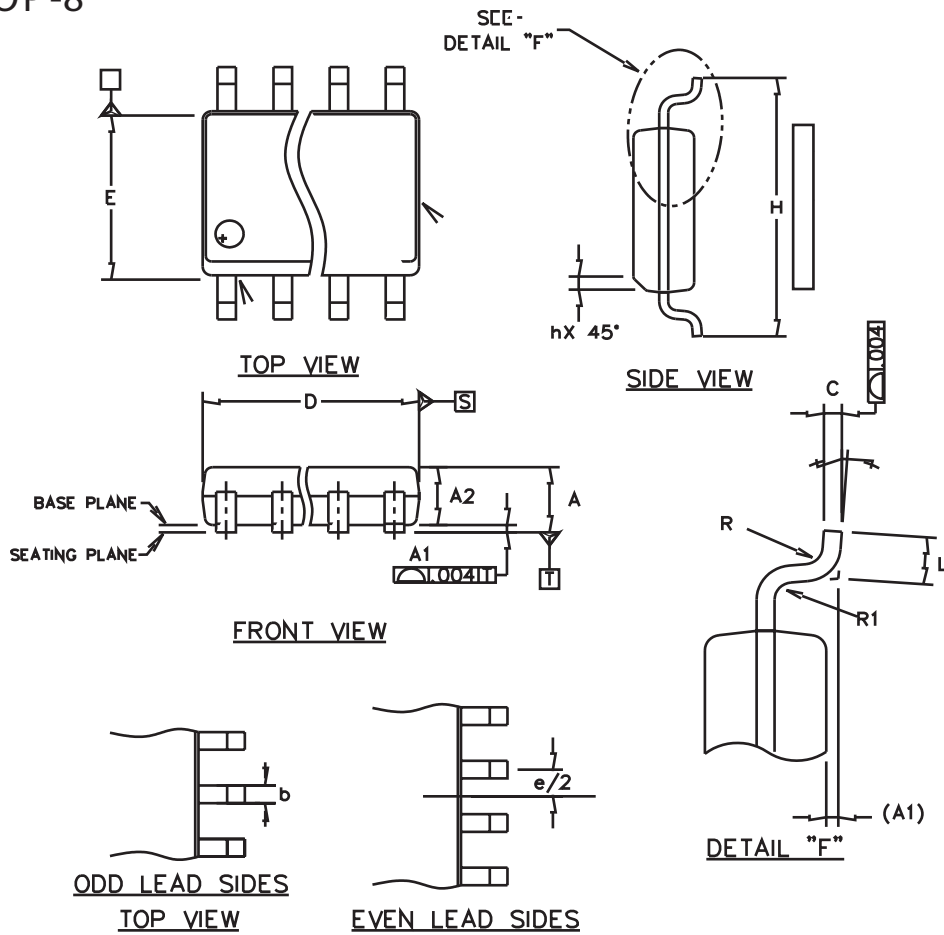
Figure 12. Switching Waveforms



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## PACKAGE OUTLINE DIMENSIONS

SOP-8



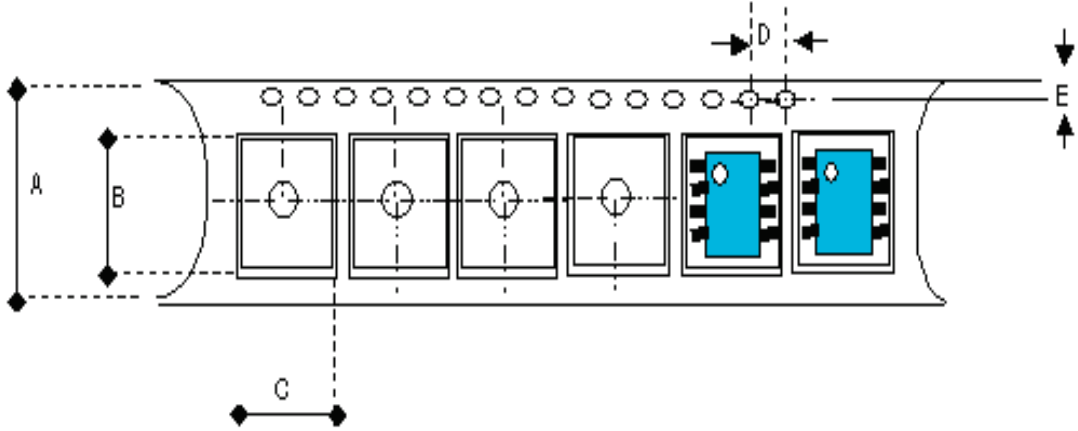
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	.055	—	.069	1
A1	.0005	—	.004	1,5
A2	.050	—	.064	1
b	.013	—	.020	1
C	.008	—	.010	1,5
R	.003	—	—	1
R1	.003	—	—	1
e	.050 BSC.			1
E	.150	—	.157	1,4
h	.010	—	.019	1
H	.228	—	.244	1,5
L	.020	—	.028	1,6
Q1	0°	—	8°	1

VAR	D			N
	MIN.	NOM.	MAX.	
AA	0.189	—	—	8
AB	0.337	—	—	14
AC	0.386	—	—	16
NOTES	1,3	—	—	16

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## SO-8 Tape and Reel Data

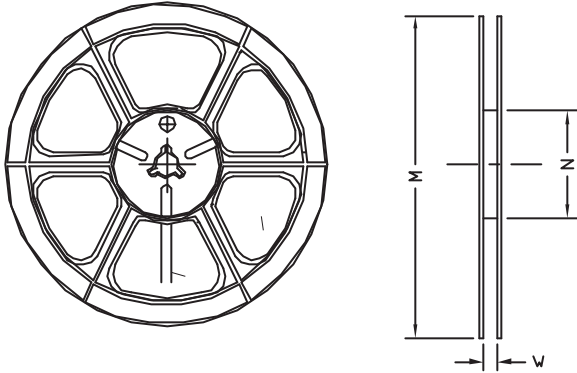
### SO-8 Carrier Tape



unit:mm

PACKAGE	A	B	C	D	E
SOP 8N	12.0	5.0	4.0	6.5	1.5
150mil	±0.3	±0.1	±0.1	±0.1	±0.1

### SO-8 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W
12 mm	φ 300	300	101	10 ± 0.2