Features

- **ARM7TDMI® ARM® Thumb® Processor Core**
  - **High-performance 32-bit RISC Architecture**
  - **Embedded ICE (In-circuit Emulation)**
- **On-chip SDRAM Controller for Embedded ARM7TDMI**
- **Multi-layer AMBA™ Architecture**
- **Dual Ethernet 10/100 Mbps MAC Interface**
- **Two USARTs with Modem Control Lines**
- **Industry-standard Serial Peripheral Interface (SPI)**
- **Flexible External Bus Interface with Programmable Chip Selects**
- **Multi-level Priority, Individually-maskable, Vectored Interrupt Controller**
- **Three 16-bit Timer/Counters**
- **Additional Watchdog Timer**
- **Up to 48 General-purpose I/O Pins**
- **JTAG Debug Interface**
- **Software Development Tools Available for ARM7TDMI**
- **Supported by a Wide Range of Ready-to-use Application Software, Including Multi-tasking Operating System and Networking Functions**
- **2.5V Power Supply for the Core and PLL Pins, 3.3V for Other I/O Pins**
- **Available in 208-lead PQFP and in 256-ball PBGA Packages**
- **Supports Commercial and Industrial Temperature Range**

Description

The AT75C140 Smart Internet Appliance Processor (SIAP™) is a high-performance processor specially designed for network-enabling consumer and industrial applications, such as printers, fax machines, industrial automation, data acquisition equipment and test equipment.

The AT75C140 is built around an ARM7TDMI microcontroller core running at 40 MHz with a dual Ethernet 10/100 Mbps MAC interface. The specific architecture of the AT75C140 delivers unmatched performance for low power consumption.

On top of the AT75C140 hardware platform, Atmel provides a special port of the Linux kernel as the proposed operating system with device drivers for the peripherals.

Smart Internet Appliance Processor (SIAP™)

AT75C140 Advance Information

Rev. 2659A–INTAP–09/02

AT75C140 Pin Configuration

Table 1. AT75C140 Pinout in 208-lead PQFP Package

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	43	MB_TXCLK	85	D4	127	NCE0	169	PA11
2	GND	44	MB_RXD0	86	VDD3V3	128	NCE1	170	PA10
3	VDD3V3	45	MB_RXD1	87	D5	129	NCE2	171	PA9
4	GND	46	MB_RXD2	88	D6	130	VDD3V3	172	PA8
5	NC	47	MB_RXD3	89	D7	131	NCE3	173	PA7
6	GND	48	MB_RXER	90	D8	132	NWE0	174	PA6
7	NTRST	49	MB_RXCLK	91	D9	133	NWE1	175	VDD3V3
8	MA_COL	50	MB_RXDV	92	D10	134	NWE2	176	NC
9	MA_CRS	51	MB_MDC	93	D11	135	VDD3V3	177	PA5
10	MA_TXER	52	VDD3V3	94	D12	136	GND	178	PA4
11	MA_TXD0	53	GND	95	D13	137	NWE3	179	PA3
12	MA_TXD1	54	MB_MDIO	96	D14	138	NWR	180	PA2
13	MA_TXD2	55	MB_LINK	97	VDD2V5	139	NSOE	181	PA1
14	MA_TXD3	56	A0	98	GND	140	GND	182	PA0
15	MA_TXEN	57	A1	99	D15	141	VDD2V5	183	GND
16	VDD3V3	58	A2	100	VDD3V3	142	NWAIT	184	RXDA
17	MA_TXCLK	59	A3	101	GND	143	MISO	185	TXDA
18	GND	60	A4	102	NREQ	144	MOSI	186	NRTSA
19	MA_RXD0	61	A5	103	NGNT	145	SPCK	187	NCTSA
20	MA_RXD1	62	A6	104	VDD3V3	146	NPCSS	188	NDTRA
21	MA_RXD2	63	A7	105	GND	147	VDD3V3	189	NDSRA
22	MA_RXD3	64	A8	106	DCK	148	GND	190	NDCDA
23	MA_RXER	65	A9	107	NCS	149	NRESET	191	RXDB
24	MA_RXCLK	66	A10	108	A10	150	FIQ	192	TXDB
25	GND	67	A11	109	NRAS	151	IRQ0	193	GND
26	VDD2V5	68	A12	110	NCAS	152	TST	194	PB0
27	MA_RXDV	69	VDD3V3	111	NC	153	GND	195	PB1
28	MA_MDC	70	GND	112	NWE	154	VDD2V5	196	PB2
29	MA_MDIO	71	A13	113	DQM0	155	NC	197	PB3
30	MA_LINK	72	A14	114	DQM1	156	VDD3V3	198	PB4
31	MB_COL	73	A15	115	DQM2	157	GND	199	PB5
32	MB_CRS	74	A16	116	GND	158	VDD3V3	200	PB6
33	GND	75	A17	117	DQM3	159	TDO	201	PB7
34	VDD2V5	76	A18	118	VDD2V5	160	TDI	202	PB8
35	VDD3V3	77	A19	119	GND	161	TMS	203	PB9
36	MB_TXER	78	A20	120	PLL_VDD	162	TCK	204	VDD3V3
37	MB_TXD0	79	A21	121	XREF240	163	PA19	205	DBW32
38	MB_TXD1	80	D0	122	PLL_GND	164	VDD2V5	206	GND
39	MB_TXD2	81	D1	123	GND	165	GND	207	BO256
40	GND	82	D2	124	XTALOUT	166	PA12	208	VDD3V3
41	MB_TXD3	83	D3	125	XTALIN	167	GND		
42	MB_TXEN	84	GND	126	VDD2V5	168	VDD3V3		

Note: NC: Not connected

Table 2. AT75C140 Pinout in 256-ball PBGA Package

Pin	Signal
A01	GND
A02	PB9
A03	PB4
A04	PB1
A05	NDSRB
A06	NRTSB
A07	RXDB
A08	NDSRA
A09	TXDA
A10	PA2
A11	PA3
A12	PA6
A13	PA10
A14	PA13
A15	PA15
A16	PA19
A17	PA22
A18	PA23
A19	TDO
A20	NC
B01	BO256
B02	PB8
B03	PB7
B04	PB3
B05	PB0
B06	NDTRB
B07	TXDB
B08	NDCDA
B09	NRTSA
B10	PA1
B11	PA5
B12	PA7
B13	PA11
B14	VDD3V3
B15	PA16
B16	PA20
B17	TMS
B18	TDI
B19	NC
B20	NC
C01	PB10
C02	PA28

Pin	Signal
C03	DBW32
C04	PB6
C05	PB2
C06	NRIB
C07	NCTSB
C08	NRIA
C09	NCTSA
C10	PA0
C11	PA4
C12	PA8
C13	PA12
C14	PA14
C15	PA18
C16	PA21
C17	TCK
C18	NC
C19	NC
C20	PA31
D01	PB11
D02	PA27
D03	PA26
D04	GND
D05	PB5
D06	VDD3V3
D07	NDCDB
D08	GND
D09	NDTRA
D10	RXDA
D11	VDD3V3
D12	PA9
D13	GND
D14	PA17
D15	VDD3V3
D16	PA24
D17	GND
D18	PA29
D19	VDD3V3
D20	IRQ1
E01	NC
E02	GND
E03	GND
E04	PA25

Pin	Signal
E17	PA30
E18	TST
E19	IRQ0
E20	NC
F01	PB13
F02	PB12
F03	GND
F04	VDD3V3
F17	VDD3V3
F18	FIQ
F19	NC
F20	SPCK
G01	MA_COL
G02	PB15
G03	PB14
G04	NTRST
G17	NRESET
G18	NPCSS
G19	MOSI
G20	MISO
H01	MA_TXD0
H02	MA_TXER
H03	MA_CRS
H04	GND
H17	GND
H18	NWAIT
H19	VDD3V3
H20	NSOE
J01	MA_TXEN
J02	MA_TXD3
J03	MA_TXD2
J04	MA_TXD1
J17	NWR
J18	NWE3
J19	NC
J20	NWE2
K01	MA_RXD0
K02	MA_TXCLK
K03	NC
K04	VDD3V3
K17	NWE1
K18	NWE0

Pin	Signal
K19	NCE3
K20	NCE2
L01	MA_RXD1
L02	MA_RXD2
L03	MA_RXD3
L04	MA_RXER
L17	VDD3V3
L18	NCE0
L19	VDD2V5
L20	NCE1
M01	MA_RXCLK
M02	VDD3V3
M03	MA_RXDV
M04	MA_MDC
M17	XREF240
M18	PLL_GND
M19	XTALOUT
M20	XTALIN
N01	MA_MDIO
N02	MA_LINK
N03	MB_COL
N04	GND
N17	GND
N18	DQM3
N19	VDD3V3
N20	PLL_VDD
P01	MB_CRS
P02	VDD2V5
P03	MB_TXD0
P04	MB_TXD3
P17	NRAS
P18	DQM0
P19	DQM1
P20	DQM2
R01	MB_TXER
R02	MB_TXD1
R03	MB_TXEN
R04	VDD3V3
R17	VDD3V3
R18	A10
R19	NCAS
R20	NWE

Pin	Signal
T01	MB_TXD2
T02	MB_TXCLK
T03	MB_RXD1
T04	MB_RXER
T17	D28
T18	D31
T19	DCLK
T20	NCS
U01	MB_RXD0
U02	MB_RXD2
U03	MB_RXCLK
U04	GND
U05	A1
U06	VDD3V3
U07	A8
U08	GND
U09	A17
U10	VDD3V3
U11	D3
U12	D7
U13	GND
U14	D16
U15	VDD3V3
U16	D22
U17	GND
U18	D27
U19	NC
U20	D30
V01	MB_RXD3
V02	MB_RXDV
V03	NC
V04	A0
V05	A4
V06	A7
V07	A11
V08	A14
V09	A18
V10	A22
V11	D2
V12	D6
V13	D10
V14	D14

Table 2. AT75C140 Pinout in 256-ball PBGA Package (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
V15	NC	W05	A5	W15	VDD3V3	Y05	A6	Y15	D13
V16	D19	W06	A9	W16	D17	Y06	A10	Y16	D15
V17	D23	W07	A12	W17	D20	Y07	A13	Y17	D18
V18	D26	W08	A15	W18	D24	Y08	A16	Y18	D21
V19	NC	W09	A19	W19	NREQ	Y09	A20	Y19	D25
V20	D29	W10	A21	W20	NC	Y10	A23	Y20	NGNT
W01	MB_MDC	W11	D1	Y01	NC	Y11	D0		
W02	NC	W12	D5	Y02	MB_MDIO	Y12	D4		
W03	NC	W13	D9	Y03	A2	Y13	D8		
W04	MB_LINK	W14	D12	Y04	A3	Y14	D11		

Note: NC: Not connected

Table 3. AT75C140 Pin Description List in 208-lead PQFP Package and 256-ball PBGA Package

Block	Pin Name in Package Type		Function	Active Level	Type
	256-ball PBGA	208-lead PQFP			
Common Bus	A[23:0]	A[21:0]	Address Bus	-	Output, TS[1]
	D[31:0]	D[15:0]	Data Bus	-	I/O[2]
	NREQ	NREQ	Bus Request	Low	Input
	NGNT	NGNT	Bus Grant	Low	Output
Synchronous Dynamic Memory Controller	DCLK	DCLK	SDRAM Clock	-	Output
	DQM[3:0]	DQM[1:0]	SDRAM Byte Masks	-	Output
	NCS	NCS	SDRAM Chip Select	Low	Output
	A10	A10	SDRAM Auto Precharge	-	Output
	NRAS	NRAS	Row Address Strobes	Low	Output
	NCAS	NCAS	Column Address Strobes	Low	Output
	NWE	NWE	SDRAM Write Enable	Low	Output
Static Memory Controller	NCE[3:0]	NCE[3:0]	Chip Select	Low	Output, TS
	NWE[3:0]	NWE[3:0]	Byte Select/Write Enable	Low	Output
	NSOE	NSOE	Output Enable	Low	Output, TS
	NWR	NWR	Memory Block Write Enable	Low	Output
	NWAIT	NWAIT	Enable Wait States	Low	Input
I/O Port A	PA[12:0] PA[19]	PA[12:0] PA[19]	General-purpose I/O lines. Multiplexed with peripheral I/Os	-	I/O
	PA[18:13] PA[31:20]	-			I/O, PD[3]
I/O Port B	PB[9:0]	PB[9:0]	General-purpose I/O lines. Multiplexed with peripheral I/Os	-	I/O
	PB[15:10]	-			I/O,PD

Table 3. AT75C140 Pin Description List in 208-lead PQFP Package and 256-ball PBGA Package (Continued)

Block	Pin Name in Package Type		Function	Active Level	Type
	256-ball PBGA	208-lead PQFP			
Timer/Counter 0	TCLK0	TCLK0	Timer 0 External Clock	-	Input
	TIOA0	TIOA0	Timer 0 Signal A	-	I/O
	TIOB0	TIOB0	Timer 0 Signal B	-	I/O
Timer/Counter 1	TCLK1	TCLK1	Timer 1 External Clock	-	Input
	TIOA1	TIOA1	Timer 1 Signal A	-	I/O
	TIOB1	TIOB1	Timer 1 Signal B	-	I/O
Watchdog	NWDOVF	NWDOVF	Watchdog Overflow	Low	Output
Serial Peripheral Interface	MISO	MISO	Master In/Slave Out	-	I/O
	MOSI	MOSI	Master Out/Slave In	-	I/O
	SPCK	SPCK	Serial Clock	-	I/O
	NPCSS	NPCSS	Peripheral Chip Select/Slave Select	Low	I/O
	NPCS1	NPCS1	Optional SPI Chip Select 1	Low	Output
USART A	RXDA	RXDA	Receive Data	-	Input
	TXDA	TXDA	Transmit Data	-	Output
	NRTSA	NRTSA	Ready to Send	Low	Output
	NCTSA	NCTSA	Clear to Send	Low	Input
	NDTRA	NDTRA	Data Terminal Ready	Low	Output
	NDSRA	NDSRA	Data Set Ready	Low	Input
	NDCDA	NDCDA	Data Carrier Detect	Low	Input
	NRIA	-	Ring Indicator	Low	Input, PU[4]
USART B	RXDB	RXDB	Receive Data	-	Input
	TXDB	TXDB	Transmit Data	-	Output
	NRTSB	-	Ready to Send	Low	Output
	NCTSB	-	Clear to Send	Low	Input, PU
	NDTRB	-	Data Terminal Ready	Low	Output
	NDSRB	-	Data Set Ready	Low	Input, PU
	NDCDB	-	Data Carrier Detect	Low	Input, PU
	NRIB	-	Ring Indicator	Low	Input, PU
JTAG Interface	NTRST	NTRST	Test Reset	Low	Input
	TCK	TCK	Test Clock	-	Input
	TMS	TMS	Test Mode Select	-	Input
	TDI	TDI	Test Data Input	-	Input
	TDO	TDO	Test Data Output	-	Output

Table 3. AT75C140 Pin Description List in 208-lead PQFP Package and 256-ball PBGA Package (Continued)

Block	Pin Name in Package Type		Function	Active Level	Type
	256-ball PBGA	208-lead PQFP			
MAC A Interface	MA_COL	MA_COL	MAC A Collision Detect	-	Input
	MA_CRS	MA_CRS	MAC A Carrier Sense	-	Input
	MA_TXER	MA_TXER	MAC A Transmit Error	-	Output, TS
	MA_TXD[3:0]	MA_TXD[3:0]	MAC A Transmit Data Bus	-	Output, TS
	MA_TXEN	MA_TXEN	MAC A Transmit Enable	-	Output, TS
	MA_TXCLK	MA_TXCLK	MAC A Transmit Clock	-	Input
	MA_RXD[3:0]	MA_RXD[3:0]	MAC A Receive Data Bus	-	Input
	MA_RXER	MA_RXER	MAC A Receive Error	-	Input
	MA_RXCLK	MA_RXCLK	MAC A Receive Clock	-	Input
	MA_RXDV	MA_RXDV	MAC A Receive Data Valid	-	Input
	MA_MDC	MA_MDC	MAC A Management Data Clock	-	Output, TS
	MA_MDIO	MA_MDIO	MAC A Management Data Bus	-	I/O, PD
	MA_LINK	MA_LINK	MAC A Link Interrupt	-	Input
MAC B Interface	MB_COL	MB_COL	MAC B Collision Detect	-	Input
	MB_CRS	MB_CRS	MAC B Carrier Sense	-	Input
	MB_TXER	MB_TXER	MAC B Transmit Error	-	Output, TS
	MB_TXD[3:0]	MB_TXD[3:0]	MAC B Transmit Data Bus	-	Output, TS
	MB_TXEN	MB_TXEN	MAC B Transmit Enable	-	Output, TS
	MB_TXCLK	MB_TXCLK	MAC B Transmit Clock	-	Input
	MB_RXD[3:0]	MB_RXD[3:0]	MAC B Receive Data Bus	-	Input
	MB_RXER	MB_RXER	MAC B Receive Error	-	Input
	MB_RXCLK	MB_RXCLK	MAC B Receive Clock	-	Input
	MB_RXDV	MB_RXDV	MAC B Receive Data Valid	-	Input
	MB_MDC	MB_MDC	MAC B Management Data Clock	-	Output, TS
	MB_MDIO	MB_MDIO	MAC B Management Data Bus	-	I/O, PD
	MB_LINK	MB_LINK	MAC B Link Interrupt	-	Input
Power	GND	GND	Ground	-	Ground
	PLL_GND	PLL_GND	PLL Ground	-	Ground
	PLL_VDD	PLL_VDD	PLL Power	-	Power
	VDD2V5	VDD2V5	2.5V Nominal Supply	-	Power
	VDD3V3	VDD3V3	3.3V Nominal Supply	-	Power

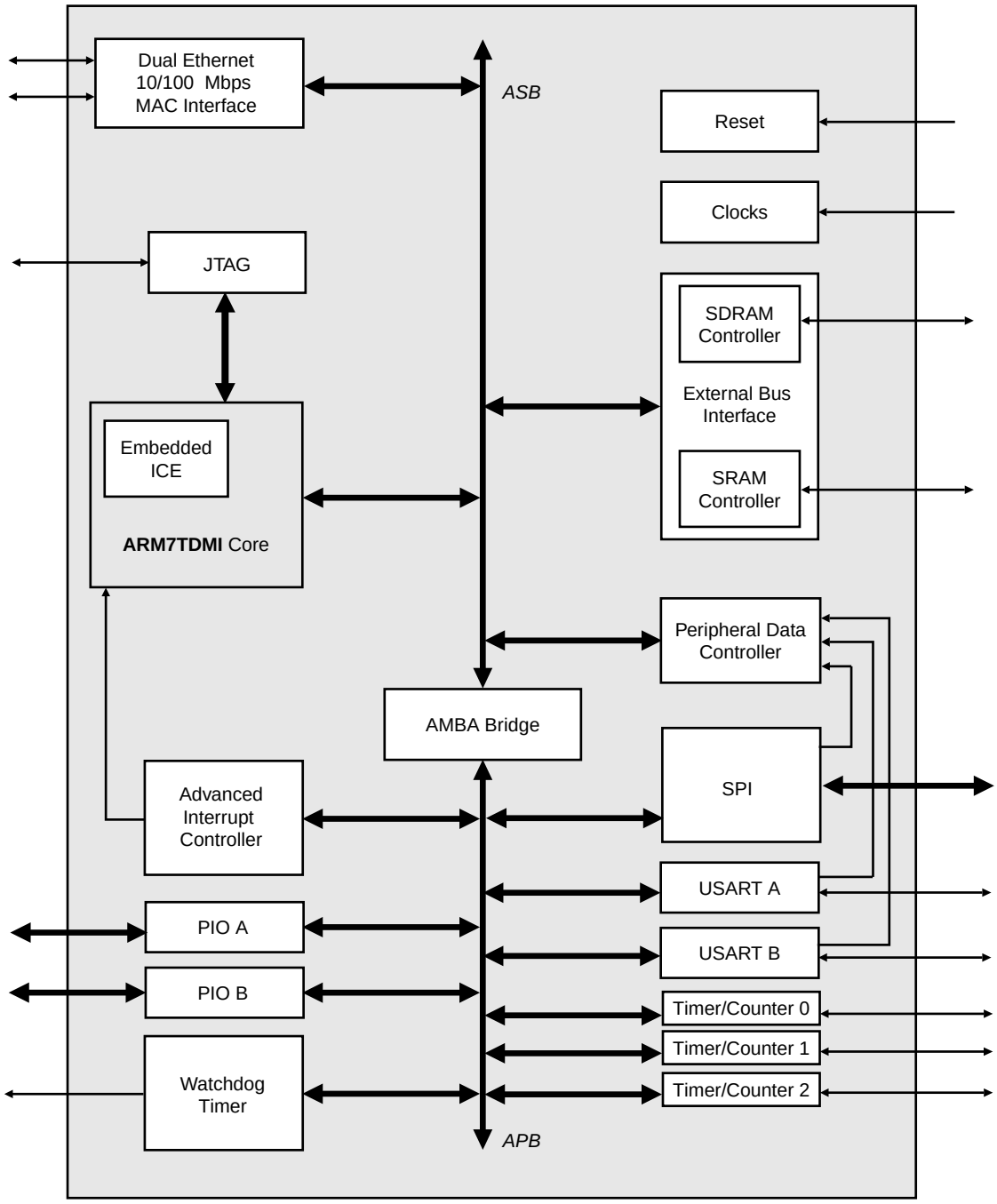
Table 3. AT75C140 Pin Description List in 208-lead PQFP Package and 256-ball PBGA Package (Continued)

Block	Pin Name in Package Type		Function	Active Level	Type
	256-ball PBGA	208-lead PQFP			
Miscellaneous	BO256	BO256	Package Size Option	-	Input
	DBW32	DBW32	External Data Bus Width for NCS	-	Input
	FIQ/LOWP	FIQ/LOWP	Fast Interrupt/Low Power	-	Input
	IRQ0	IRQ0	External Interrupt Requests	-	Input
	IRQ1	-			Input, PD
	NRESET	NRESET	Power on Reset	Low	Input
	TST	TST	Test Mode	High	Input
	XREF240	XREF240	External PLL loop filter	-	Input
	XTALIN	XTALIN	External Crystal Input	-	Input, PD
	XTALOUT	XTALOUT	External Crystal Output	-	Output

Notes:
1. TS: Three-state
2. I/O: Input/Output
3. PD: Internal Pull-down Resistor
4. PU: Internal Pull-up Resistor

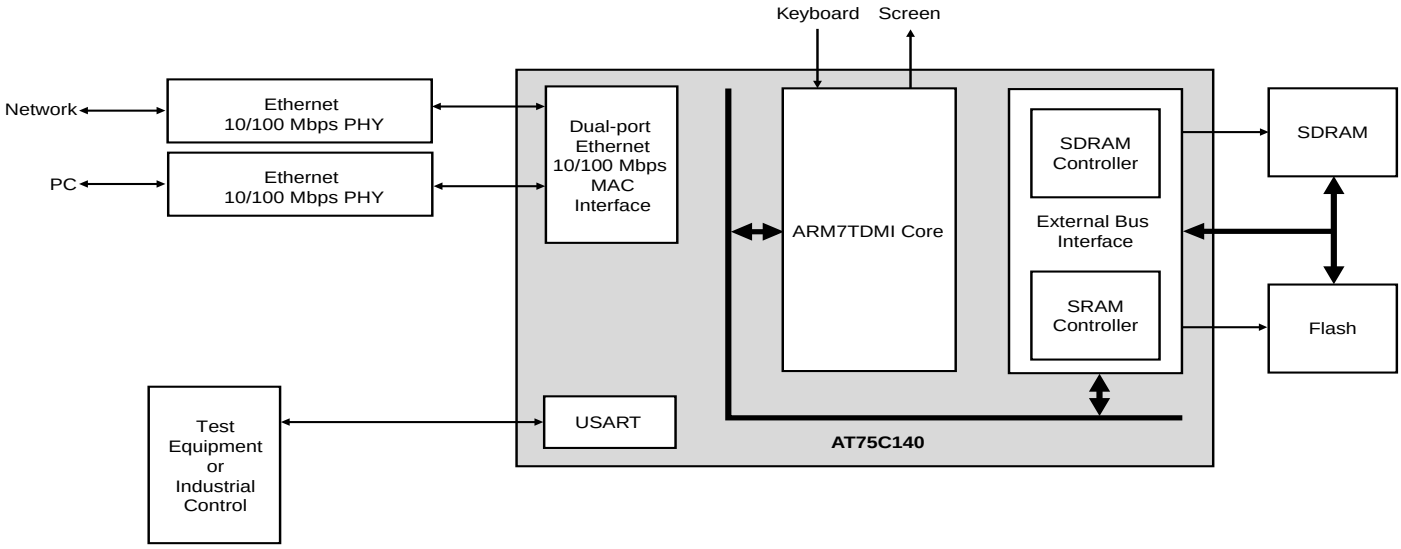
Block Diagram

Figure 1. AT75C140 Block Diagram



Application Example

Figure 2. Process Control



Functional Description

ARM7TDMI Core

The ARM7TDMI is a three-stage pipeline, 32-bit RISC processor. The processor architecture is Von Neumann load/store architecture, characterized by a single data and address bus for instructions and data. The CPU has two instruction sets: the ARM and the Thumb instruction set. The ARM instruction set has 32-bit wide instructions and provides maximum performance. Thumb instructions are 16-bit wide and give maximum code density.

Instructions operate on 8-bit, 16-bit and 32-bit data types.

The CPU has seven operating modes. Each operating mode has dedicated banked registers for fast exception handling. The processor has a total of 37 32-bit registers, including six status registers.

Ethernet MAC

The AT75C140 contains an Ethernet subsystem mainly composed of three independent parts: two identical independent Ethernet MACs and a packet buffer of 32K bytes, connected together with a local bus.

The Ethernet MACs exhibit the following features:

- Support for 10 and 100 Mbps operation
- Support for full- and half-duplex
- Standard MII interface
- Broadcast, multicast and four unicast address filters
- Automatic CRC generation
- Automatic zero padding
- Pause and jamming support
- Transmit and receive FIFOs
- Integrated DMA

The local packet buffer is filled/emptied by the MACs' DMA. This memory is used to store the received/transmitted packets temporarily. Its size allows it to hold enough packets to cope with most situations. Should an overflow occur, a part of the external system memory can be used as an overflow buffer to avoid data loss.

The main benefit of having a local bus is that the majority of packets can be received from one MAC and transmitted through the other with minor software intervention.

EBI: External Bus Interface

The EBI generates the signals which control access to external memory or memory-mapped peripherals. The EBI is fully programmable. The interface to external devices is composed of common address and data buses and separate control lines to allow the connection of static or dynamic devices.

The main common features of the EBI are:

- External memory mapping
- 32- or 16-bit data bus width
- Support for both static and SDRAM-type memories

Various features specific to static memories or SDRAM memories are listed below.

Static Memories	SDRAM Memories
Up to four chip select lines	Byte, half-word and word access supported
Byte write or byte select lines	CAS latency of two clock cycles supported
Two different read protocols	Auto-precharge command
Programmable wait state generation	Programmable refresh rate
Programmable data float time	Supports two or four internal banks
	From 256 up to 2048 columns supported
	From 2048 up to 8192 rows supported

AIC: Advanced Interrupt Controller

The AT75C140 has an 8-level priority interrupt controller. The interrupt controller outputs are connected to the fast interrupt request (NFIQ) and the normal interrupt request (NIRQ) of the ARM7TDMI core. The processor's NFIQ can only be asserted by the external fast interrupt request input (FIQ). The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals or by the external interrupt request line IRQ0.

An 8-level priority encoder allows the application to define the priority between the different interrupt sources. Internal sources are programmed to be level sensitive or edge sensitive. External sources can be programmed to be positive- or negative-edge triggered, or low- or high-level sensitive.

PIO: Parallel I/O Controller

The AT75C140 has up to 48 programmable I/O lines. They can all be programmed as inputs or outputs. To optimize the use of available package pins, most of them are multiplexed with external signals of on-chip peripherals.

The PIO lines are controlled by two separate and identical PIO controllers called PIOA and PIOB.

The PIO controllers enable the generation of an interrupt on input change on each PIO line. Some I/O lines have enough drive capability to power a LED.

USART: Universal Synchronous/ Asynchronous Receiver/ Transmitter

The AT75C140 provides two identical full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:

- Programmable baud rate generator
- Parity, framing and overrun error detection
- Line break generation and detection
- Automatic echo, local loopback and remote loopback channel modes
- Multi-drop mode: address detection and generation
- Interrupt generation
- Four dedicated peripheral data controller channels
- 6-, 7- and 8-bit character length (9 bits in multi-drop mode)

SPI: Serial Peripheral Interface

The AT75C140 includes an SPI which provides communication with external devices in master or slave mode.

The SPI contains two dedicated peripheral data controller channels and one external chip select which can be connected to up to 2 devices. The data length is programmable from 8 to 16 bits.

Timer/Counter

The AT75C140 features three identical 16-bit timer/counters. They can be independently programmed to perform a wide range of functions, including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

The triple timer/counter block provides three external clock inputs, five internal clock inputs and two multi-purpose signals which can be configured by the user. Each timer drives an internal interrupt signal which can be programmed to generate processor interrupts via the Advanced Interrupt Controller.

Watchdog Timer

The AT75C140 is equipped with an internal Watchdog Timer that can be used to prevent system lock-up if the software becomes trapped in a deadlock.

PDC: Peripheral Data Controller

The AT75C140 is furnished with a six-channel peripheral data controller (PDC) dedicated to the two on-chip USARTs and the SPI. One PDC channel is connected to the receiver and one to the transmitter of each peripheral requiring a high data throughput.

The user interface of a PDC channel is integrated in the memory space of each USART or SPI channel. It contains a 32-bit address pointer register and a 16-bit transfer counter register. When the programmed number of bytes is transferred, an end-of-transfer interrupt is generated by either the corresponding USART or the SPI.

Special Functions

The AT75C140 provides registers which implement the following special functions:

- Chip identification
- Reset status
- Power management
- Temperature range selection

Application Software

The AT75C140 is supported by a comprehensive range of software modules. As a result of the widespread use of the ARM7TDMI, a wide range is available directly from Atmel, from Atmel's qualified software partner or from other third parties.

The application software modules are OS level.

The AT75C140 is supplied with a customized port of the Linux kernel. It features device drivers for all the on-chip peripherals and supports file system usage. It also supports the native TCP/IP facilities which have made Linux a success in Internet applications. This kernel is available in source code under the terms of the Gnu Public License.

Development Tools

The ARM7TDMI is an industry-standard core. It is supported by a comprehensive range of state-of-the-art development tools, including assemblers, C-compilers, source level debuggers and hardware emulators.

Packaging

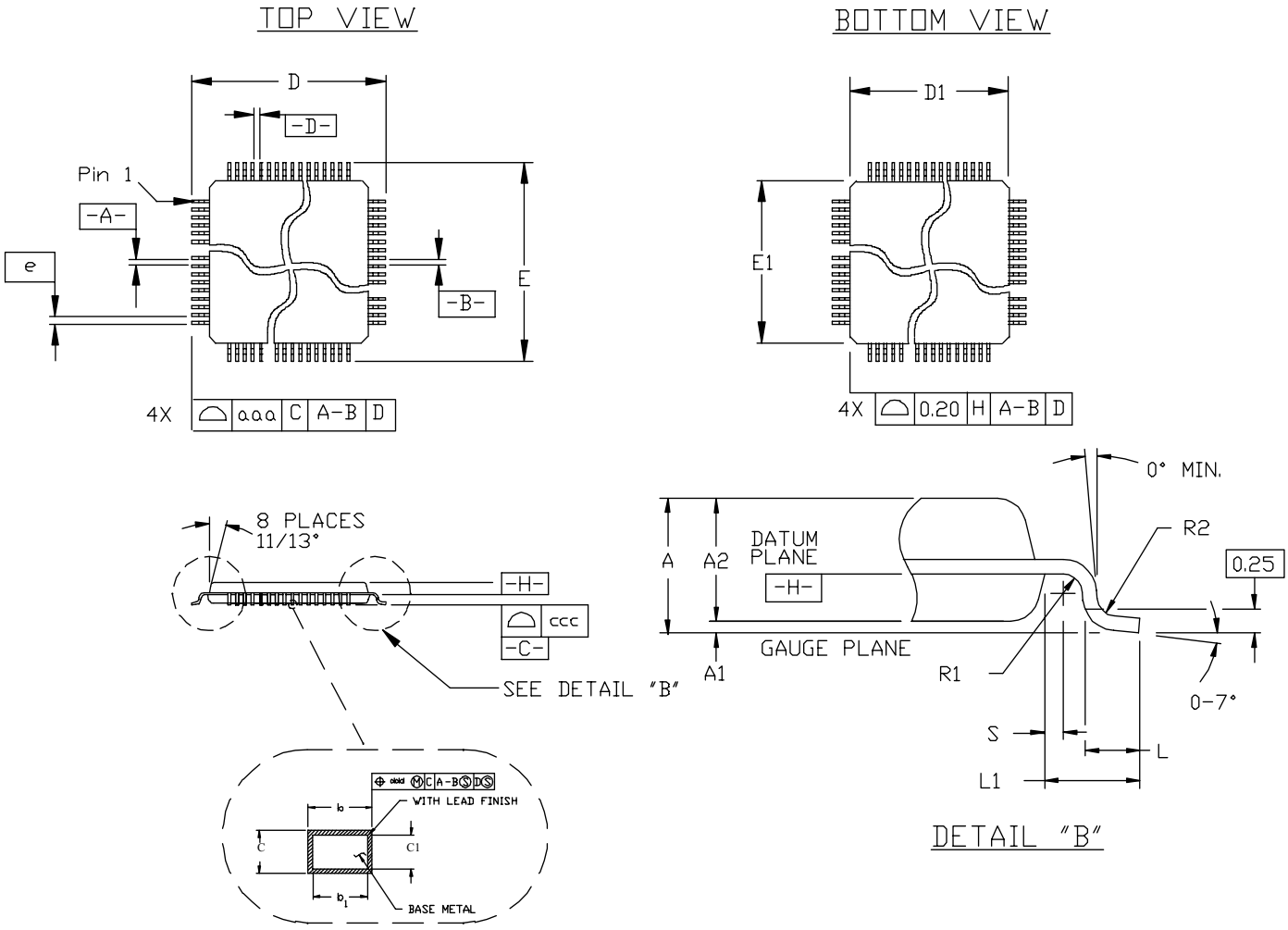
The AT75C140 is supplied in a 208-lead PQFP package. This provides the best compromise between external connectivity and cost.

An alternative 256-ball PBGA package is also available. It provides the application developer with a larger I/O capability and improved CPU performance.

Although this 256-ball PBGA package is primarily dedicated to development, it can also be used in production for systems which require a high level of connectivity. It offers up to 48 general-purpose I/Os and a full-width system bus (24 address bits and 32 data bits).

Package Details

Figure 3. PQFP Package Drawing



For package data, see Table 4, Table 5 and Table 6 below.

Table 4. PQFP Package Dimensions (mm)

Symbol	Min	Nom	Max
c	0.11		0.23
c1	0.11	0.15	0.19
L	0.65	0.88	1.03
L1		1.60 REF	
R2	0.13		0.3
R1	0.13		
S	0.4		
Tolerances of Form and Position			
aaa		0.25	
ccc			0.10

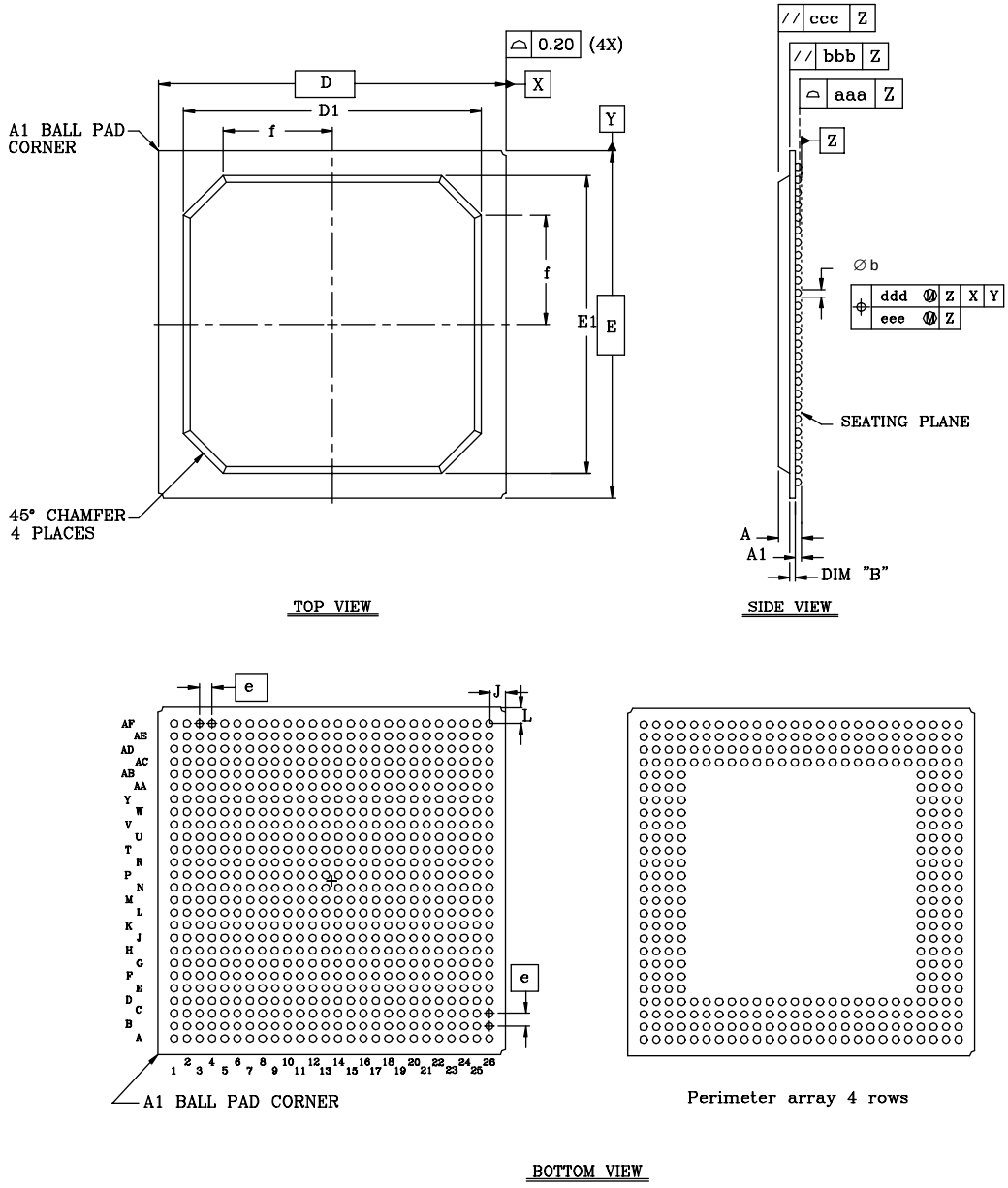
Table 5. Dimensions specific to 208-lead PQFP Package (mm)

A	A1	A2			b		b1			D	D1	E	E1	e	ddd
Max	Min	Min	Nom	Max	Min	Max	Min	Nom	Max	BSC	BSC	BSC	BSC	BSC	BSC
4.10	0.25	3.20	3.40	3.60	0.17	0.27	0.17	0.20	0.23	31.20	28.00	31.20	28.00	0.50	0.10

Table 6. 208-lead PQFP Package Electrical Characteristics

Body Size	R (mΩ)		C_s (pF)		C_m (pF)		L_s (nH)		L_m (nH)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
28 x 28	53	71	1.4	1.7	0.56	0.73	6.7	8.4	3.9	5.1

Figure 4. PBGA Package Drawing



For package data, see Table 7, Table 8 and Table 9 below.

Table 7. PBGA Package Dimensions (mm)

Symbol	Min	Nom	Max
A1	0.50	0.60	0.70
Diameter B	0.60	0.75	0.90
aaa		0.30	
bbb		0.25	
ccc		0.35	
ddd		0.30	
eee		0.15	

Table 8. Dimensions depending on Layer Number of the Package Board (mm)

	A			Dim B		
Layer	Min	Nom	Max	Min	Nom	Max
2	1.92	2.13	2.34	0.28	0.32	0.38
4	2.12	2.33	2.56	0.44	0.52	0.60

Table 9. Dimensions specific to 256-ball PBGA Package (mm)

		D/E			D1/E1				
e REF	Body Row Array	Min	Nom	Max	Min	Nom	Max	f REF	J/L REF
1.27	P4R	26.8	27.0	27.2		24.0	24.7	8.05	1.44

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