



U74AHC1G79

CMOS IC

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

DESCRIPTION

The **UTC U74AHC1G79** is a positive-edge-triggered D-type flip-flop.

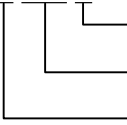
Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

FEATURES

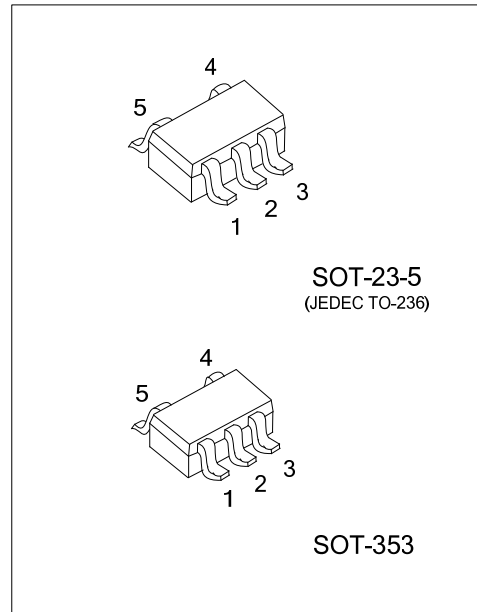
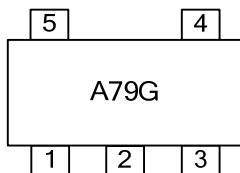
- * Wide supply voltage range from 2.0V to 5.5V
- * Symmetrical output impedance
- * Balanced propagation delays
- * High noise immunity

ORDERING INFORMATION

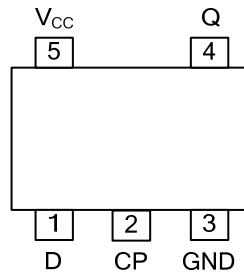
Ordering Number	Package	Packing
U74AHC1G79G-AE5-R	SOT-23-5	Tape Reel
U74AHC1G79G-AL5-R	SOT-353	Tape Reel

<p>U74AHC1G79G-AE5-R</p>  <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) AE5: SOT-23-5, AL5: SOT-353 (3) G: Halogen Free and Lead Free</p>
--	---

MARKING



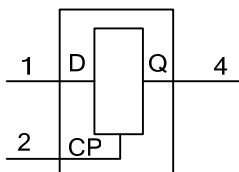
■ PIN CONFIGURATION



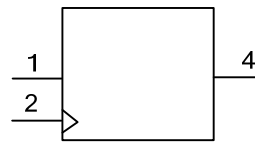
■ FUNCTION TABLE (each gate)

INPUTS		OUTPUT
CP	D	Q
↑	L	L
↑	H	H
L	X	Q

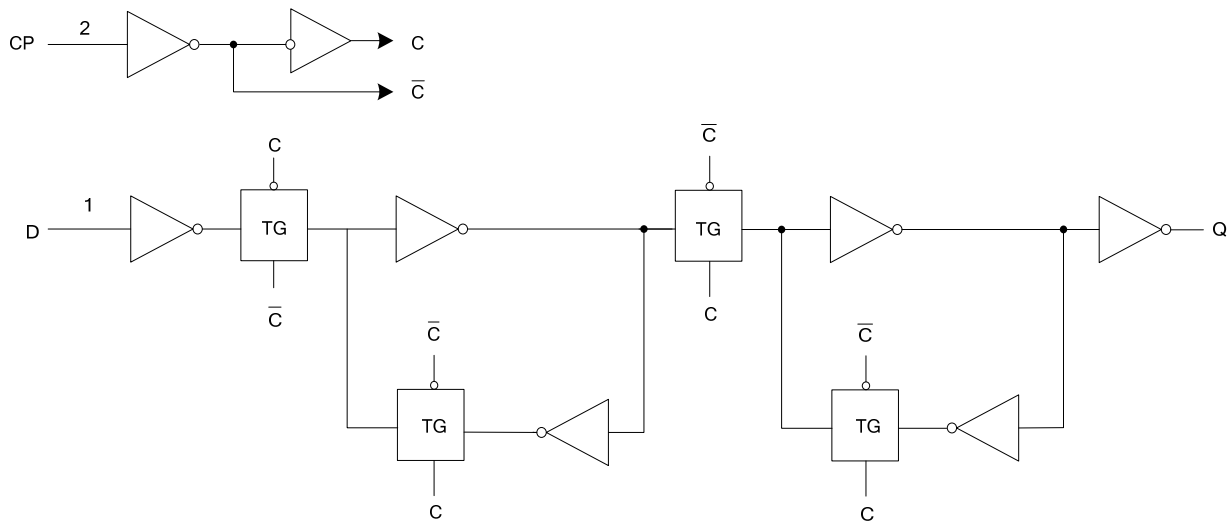
■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ +7.0	V
Output Voltage	V_{OUT}		-0.5 ~ $V_{CC} + 0.5$	V
Continuous V_{CC} or GND Current	I_{CC}		±50	mA
Continuous Output Current	I_{OUT}	$-0.5V < V_{OUT} < V_{CC} + 0.5V$	±25	mA
Input Clamp Current	I_{IK}	$V_{IN} < -0.5$	-20	mA
Output Clamp Current	I_{OK}	$V_{OUT} < -0.5$ or $V_{OUT} > V_{CC} + 0.5V$ (Note 2)	±20	mA
Operating Temperature	T_{OPR}		-40 ~ + 85	°C
Storage Temperature Range	T_{STG}		-65 ~ + 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2.0	5.0	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Operating Temperature	T_A		-40		+85	°C
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC} = 3.3 \pm 0.3V$			100	ns/V
		$V_{CC} = 5.0 \pm 0.5V$			20	ns/V

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	$V_{CC} = 2.0V$	1.5			V
		$V_{CC} = 3.0V$	2.1			V
		$V_{CC} = 5.5V$	3.85			V
Low-level Input Voltage	V_{IL}	$V_{CC} = 2.0V$			0.5	V
		$V_{CC} = 3.0V$			0.9	V
		$V_{CC} = 5.5V$			1.65	V
High-level output voltage (all outputs)	V_{OH}	$V_{CC} = 2.0V$	1.9	2.0		V
		$V_{CC} = 3.0V$	2.9	3.0		V
		$V_{CC} = 4.5V$	4.4	4.5		V
High-Level Output Voltage	V_{OH}	$V_{CC} = 3.0V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -4.0mA$	2.58			V
		$V_{CC} = 4.5V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -8.0mA$	3.94			V
Low-level output voltage (all outputs)	V_{OL}	$V_{CC} = 2.0V$			0.1	V
		$V_{CC} = 3.0V$			0.1	V
		$V_{CC} = 4.5V$			0.1	V
Low-Level Output Voltage	V_{OL}	$V_{CC} = 3.0V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = 4.0mA$			0.36	V
		$V_{CC} = 4.5V, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = 8.0mA$			0.36	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC} = 5.5V, V_{IN} = V_{CC}$ or GND			±0.1	µA
Quiescent Supply Current	I_{CC}	$V_{CC} = 5.5V, V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$			1.0	µA
Input Capacitance	C_{IN}	$V_{IN} = V_{CC}$ or GND		1.5	10	pF

■ SWITCHING CHARACTERISTICS (GND=0V, $t_r = t_f \leq 3.0\text{ns}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
maximum clock pulse frequency	f_{Max}	$V_{\text{CC}}=4.5\text{V} \sim 5.5\text{V}$	90			MHz
Propagation delay from input (CP) to output (Q)	$t_{\text{PLH}} / t_{\text{PHL}}$	$C_L=15\text{pF}$	$V_{\text{CC}}=3.0\text{V} \sim 3.6\text{V}$	4.9	8.4	ns
			$V_{\text{CC}}=4.5\text{V} \sim 5.5\text{V}$	3.5	5.6	ns
		$C_L=50\text{pF}$	$V_{\text{CC}}=3.0\text{V} \sim 3.6\text{V}$	6.9	12	ns
			$V_{\text{CC}}=4.5\text{V} \sim 5.5\text{V}$	5.1	8	ns

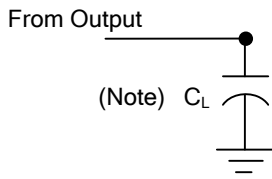
■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
clock pulse width High or Low	t_w	$V_{\text{CC}}=4.5\text{V} \sim 5.5\text{V}$	3.0			ns
set-up time D to CP	t_{su}	$V_{\text{CC}}=4.5\text{V} \sim 5.5\text{V}$	3.0	1.0		ns
hold time D to CP	t_h	$V_{\text{CC}}=4.5\text{V} \sim 5.5\text{V}$	2.0	1.0		ns

■ OPERATING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

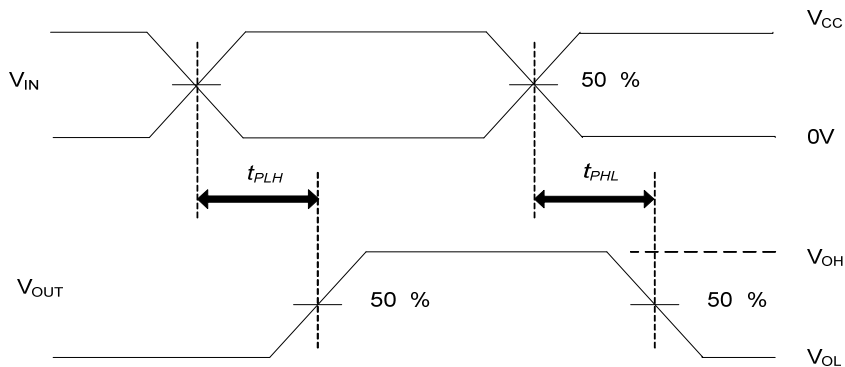
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$C_L=50\text{pF}$, $f=1\text{MHz}$		15		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{IN} INPUT	V_M INPUT	V_M OUTPUT
GND to V_{CC}	50% V_{CC}	50% V_{CC}
GND to 3.0V	1.5V	50% V_{CC}



PROPAGATION DELAY TIMES

- Notes: 1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_0 = 50\Omega$, $t_r \leq 3ns$, $t_f \leq 3ns$.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.