

Feature

- Tow anti-paralled thyristors on si-wafer
- Hermetic metal cases with ceramic insulators
- Capsule packages for double sided cooling

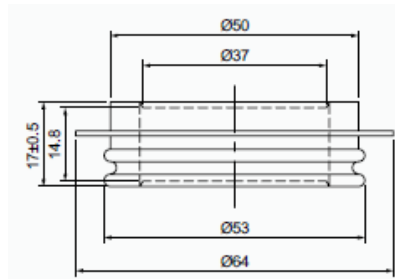
Typical Application

- High power industrial and power transmissior
- DC ang AC motor control
- AC controllers

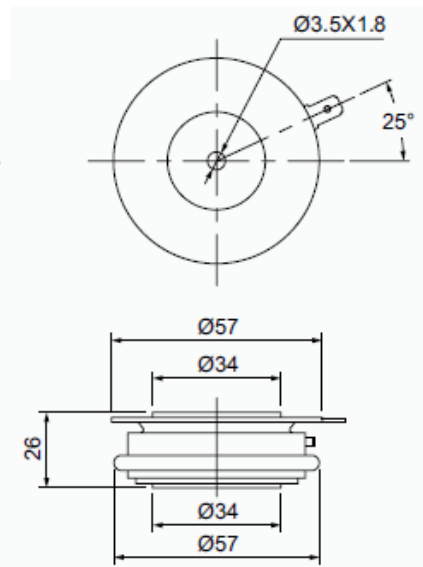
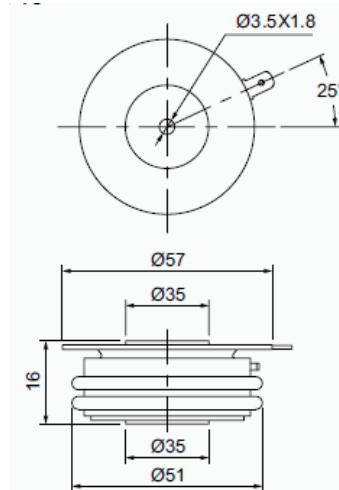
$I_{T(RMS)}$	500A
V_{DRM}/V_{RRM}	100-2000V
I_{TMS}	4KA
I^2t	245 $10^3 a^2s$

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_J (°C)	VALUE		UNIT
				Min	Max	
$I_{T(RMS)}$	Mean on-state current	180° half sine wawe 50Hz Double side cooled, THS=97°C	125		500	A
$I_{T(RMS)}$	RMS current	180° half sine wawe 50Hz Double side cooled, THS=55°C	125		972	A
V_{DRM}	Repettive peak reverse voltage	$V_{DRM} \& V_{RRM} tp=10ms$ $V_{DSM} \& V_{RSM} = V_{DRM} \& V_{RRM} + 100V$	125	100	2000	V
I_{DRM}	Repetitive peak current	$V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$	125		40	mA
I_{TSM}	Surge on-state current	10ms half sine wave $V_R = 0.6 V_{RRM}$	125		4	KA
I^2t	I^2t for fusing coordination				245	$A^2S \cdot 10$
V_{TO}	Threshold voltage		125		0.90	V
r_T	On-state slop resistance				1.02	mΩ
V_{TM}	Peak on-state voltage	$I_{TM} = 628A, F = 15KN$	25		2.40	V
dv/dt	Critical rate of rise of-state voltage	$V_{DM} = 0.67 V_{DRM}$	125		800	V/us
di/dt	Critical rate of rise of on-state current	$V_{DM} = 67\% V_{DRM}$ TO 1000A, Gate pulse $tr \leq 0.5us$ $I_{GM} = 1.5A$	125		50	A/us
I_{GT}	Gate trigger current	$V_A = 12V, I_A = 1A$	25	20	300	mA
V_{GT}	Gate trigger voltage			0.8	3.0	V
I_H	Holding current			20	300	mA
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At 180° sine double side cooled Clamping force 5.0kn			0.040	°C/W
F_M	Mounting force			10	20	KN
T_{stq}	Stored temperature			-40	140	°C
W_t	Weight					g
Outline						

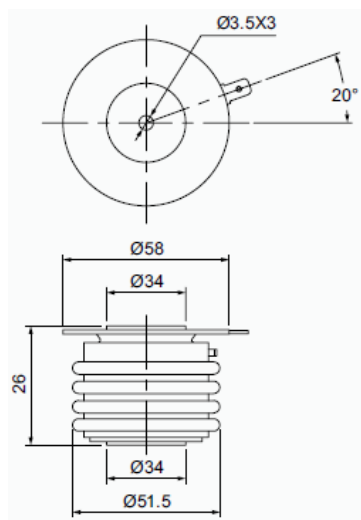
Outline:



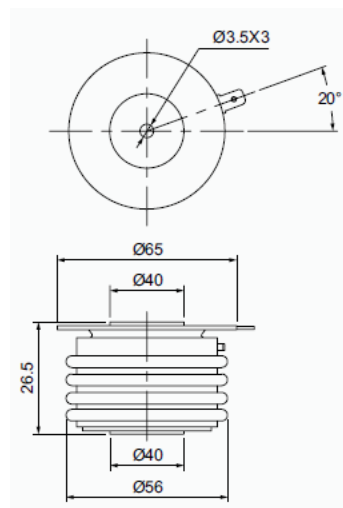
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