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August 2000 File Number 3037.3

Radiation Hardened 3-Line to 8-Line Decoder/Demultiplexer

The Intersil HS-54C138RH is a radiation hardened 3- to 8-line decoder fabricated using a radiation hardened EPI-CMOS process. It features low power consumption, high noise immunity, and high speed. Also featured are pin and function compatibility with the 54LS138 industry standard part. The HS-54C138RH is ideally suited for high speed memory chip select address decoding. It is intended for use with the Intersil HS-80C85RH radiation hardened microprocessor, but it can also be utilized as a demultiplexer in any low power rad-hard application.

The HS-54C138RH contains a one of eight binary decoder. A three bit binary input is used to select and activate each of the eight outputs, provided the three chip enable inputs are also present (see truth table).

The HS-54C138RH has an on-chip enable gate. The active high (G1) and both active low ($\overline{G2A}$, $\overline{G2B}$) inputs are Anded together to provide a single enable input to the device. The use of both active high and active low inputs minimizes the need for external gates when expanding a system.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95825. A "hot-link" is provided on our homepage for downloading.
www.intersil.com/spacedefense/space.asp

Ordering Information

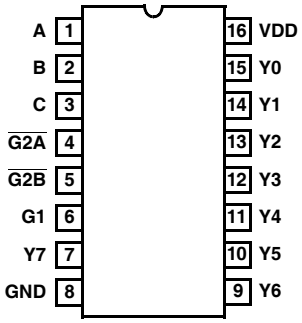
ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^oC)
5962R9582501QEC	HS1-54C138RH-8	-55 to 125
5962R9582501QXC	HS9-54C138RH-8	-55 to 125
5962R9582501V9A	HS0-54C138RH-Q	25
5962R9582501VEC	HS1-54C138RH-Q	-55 to 125
5962R9582501VXC	HS9-54C138RH-Q	-55 to 125

Features

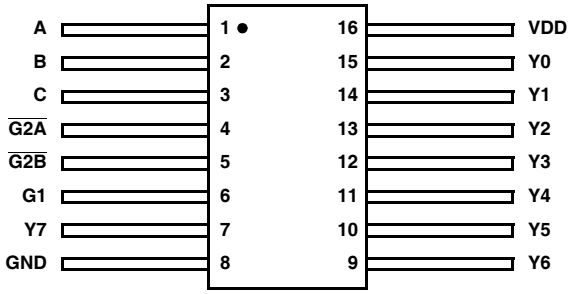
- Electrically Screened to SMD # 5962-95825
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardened EPI-CMOS
  - Total Dose . . . . . 1 x 10^5RAD(Si)
  - Latch-Up Immune . . . . . >1 x 10^{12}RAD(Si)/s
- Multiple Input Enable for Easy Expansion
- Single Power Supply . . . . . +5V
- Outputs Active Low
- Low Standby Power . . . . . .0.5mW Max at +5V
- High Noise Immunity
- Equivalent to Sandia SA2995
- Bus Compatible with Intersil Rad-Hard 80C85RH
- Full Military Temperature Range . . . . . -55^{o}C to 125^{o}C

Pinouts

16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T16
TOP VIEW



16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F16
TOP VIEW



Typical Applications

Typical applications include systems which require multiple input/output ports and memories. When the HS-54C138RH is enabled one of the eight outputs will go low. This output can be used to select a particular device or a group of devices. The HS-54C138RH can also be cascaded to provide an enabling scheme for larger systems and allow one decoder to control eight other decoders as in Figure 1.

Figure 2 shows a configuration that can be used to enable multiple I/O ports or memory devices. Up to 24 memory devices or I/O ports can be controlled using this circuit.

For demultiplexer operation, one of the three enable inputs is used as the data input while the other two inputs are enable. The transmitted data is distributed to the proper output as determined by the 3-line select inputs. See Figure 3.

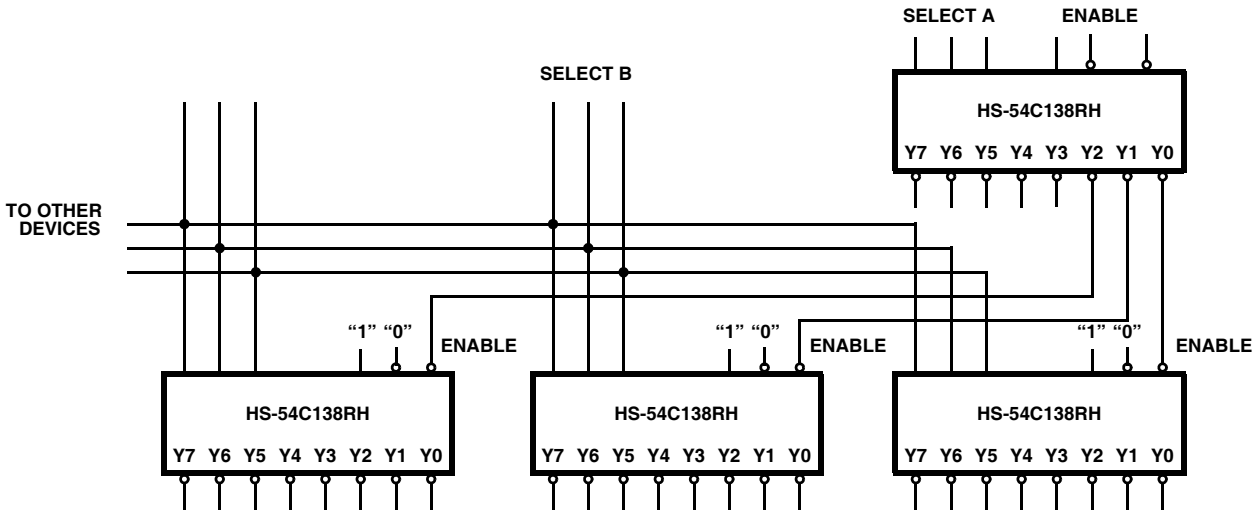


FIGURE 1.

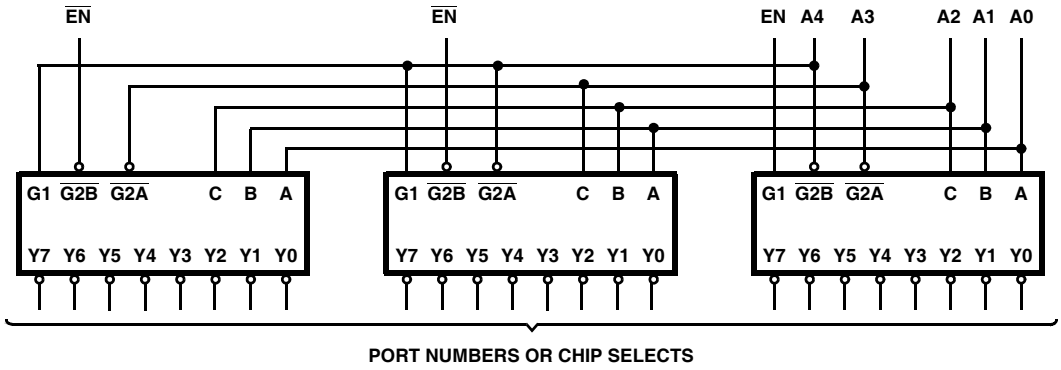


FIGURE 2.

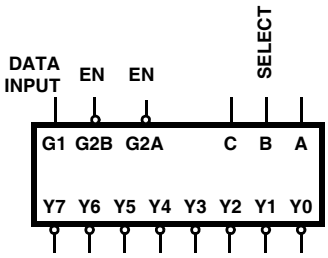


FIGURE 3.

Die Characteristics

DIE DIMENSIONS:

76 mils x 63 mils x 14 mils ±1 mil

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

INTERFACE MATERIALS:

Glassivation:

Type: SiO2
Thickness: 8kÅ ±1kÅ

Top Metallization:

Type: AlSi
Thickness: 11kÅ ±2kÅ

Substrate:

Radiation Hardened Silicon Gate,
Dielectric Isolation

Backside Finish:

Silicon

Metallization Mask Layout

HS-54C138RH