AvnetCore: Datasheet

Version 1.0, July 2006

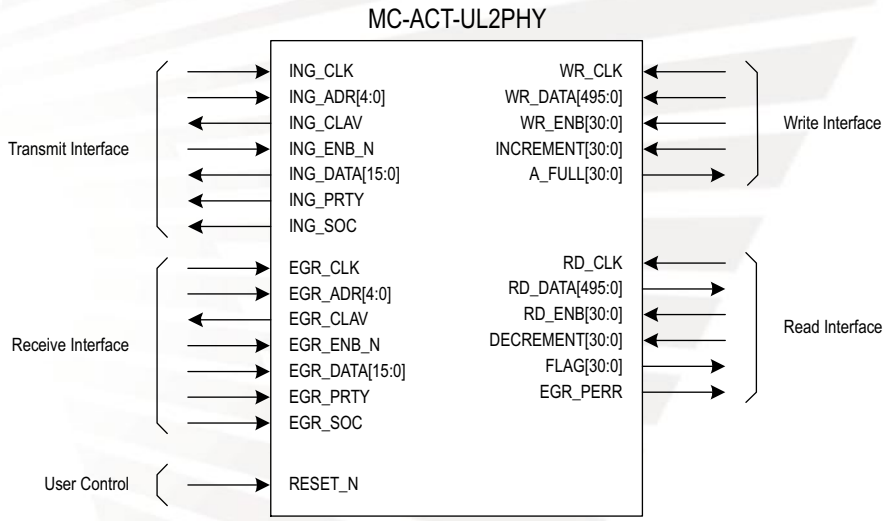
UTOPIA Level 2 PHY

Features:

- Supports Actel Axcelerator devicesI/O Peripherals
- Compliant with ATM Forum af-phy-0017.000 and af-phy-0039.000
- Supports up to 31 PHYs
- Special single PHY mode for smaller footprint
- Automatic PHY polling and selection
- Supports both 8-bit and 16-bit interfaces
- Supports 52-byte and 54-byte cell lengths
- Sync or Asynch FIFOs using RAM blocks

Applications:

- ATM cell processors
- ATM switch fabrics



MC-ACT-UL2PHY Logic Symbol

UTOPIA (Universal Test and Operations PHY Interface for ATM) Level 2 defines the interface between the ATM or LINK layer and a Physical Layer (PHY) device. The UTOPIA Level 2 standard defines a full duplex interface with a Master/Slave format. The Slave or LINK layer device responds to the requests from the PHY or Master device. The Master performs PHY arbitration and initiates data transfers to and from the Slave. The ATM forum has defined the UTOPIA Level 2 as either 8 or 16 bits in width, at up to 50 MHz, supporting an OC12 channel at 622Mbps.

CompanionCore Facts

Core Metrics	
See Table 1	
Provided with Core	
Documentation	User Guide, Data Sheet
Design File Formats	VHDL RTL, targeted netlist
Constraint Files	None
Verification Method	HDL Testbench
Design Tool Requirements	
Simulation Tool	Model*Sim*® Actel 5.8b
Synthesis Tool	Synplify® for Actel 7.5.1a
Place & Route Tool	Designer 6.0
Support	
Core support provided by Avnet Memec; Additional customization provided by Avnet Memec.	

Actel CompanionCore

AVNET Memec

Functional Description

UL2PHY
This is the top level of the core. Its only purpose is to serve as a container to instantiate the transmit (TX) & receive (RX) blocks. UL2PHY is also where the generics are located that configure the core. These parameters are then passed down to the TX & RX blocks.

INGRESS_MPHY_SLAVE
This block comprises the transmit portion of the interface. The Ingress Multi-PHY Slave block is responsible for sending cells from selected queues to the Link device. As per the NUMPHYS generic, an Ingress Single PHY Slave, Packet Counter and FIFO are instantiated for each PHY.

EGRESS_MPHY_SLAVE
This block comprises the receive portion of the interface. The Egress Multi-PHY Slave block is responsible for accepting cells sent by the link device. As per the NUMPHYS generic, an egress Single PHY Slave, Packet Counter and FIFO are instantiated for each PHY.

INGRESS_SPHY_SLAVE
The Ingress Single PHY Slave block is responsible for sending cells as requested by the Ingress Multi-PHY Slave block.

EGRESS_SPHY_SLAVE
The Egress Single PHY Slave block is responsible for accepting cells as requested by the Egress Multi-PHY Slave block.

FIFO_16 & FIFO_8
The FIFO module contains one FIFO per PHY polled (i.e. this module is instantiated N times, where N = number of PHY ports). The FIFOs are created by utilizing the available RAM blocks in the FPGA. The FIFO may be operated in synchronous (same clock for read & write) and asynchronous (different clocks for read & write) systems.

The FIFO_16 block is used when the UL2 data buses are configured to be 16 bits wide. Likewise, the FIFO_8 block is used when the UL2 data buses are configured to be 8 bits wide. Either is capable of storing up to 9 cells.

PACKET_COUNTER
The packet counter module (one per PHY port) is responsible for generating the cell available flags for the rest of the design. Every time a cell is written into the FIFO increment gets set and the cell count goes up and when a cell is read, decrement is set and the cell count goes down.

VERIFICATION METHODS
This core has been simulated with an extensive suite of testbenches to FPGAs by Avnet Memec. This core has also been implemented in hardware at multiple customer sites.

Recommended Design Experience

Users should be familiar with Actel Libero IDE, Synplify, and Model*Sim*. Users should have experience instantiating netlists, sometimes called “black boxes”, into designs.

Device Requirements

Family	Device	C cells	R cells	Tiles	RAM's	Speed
Axcelerator	AX125	55%	98%	n/a	4	98 MHz
ProASIC^{PLUS}	APA075	n/a	n/a	67%	8	68 MHz
ProASIC3	A3P250	n/a	n/a	28%	4	76 MHz

Table 1: Core Implementation Data (2 PHY’s)

Notes:
1. Specified devices are minimum size and speed recommended.
2. Assumes all core I/Os are routed off chip.

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Direction	Description
RESET_N	Input	Active low reset.
ING_CLK	Input	Transmit Clock. See UL2 Specification for details.
ING_ADDR(4:0)	Input	Transmit Polling Address. See UL2 Specification for details.
ING_CLAV	Output	Transmit Cell Available. See UL2 Specification for details.
ING_ENB_N	Input	Transmit Enable. See UL2 Specification for Details.
ING_DATA(N:0)	Output	Transmit Data, where N is 7 + (8*SIZE_16). See UL2 Specification for details.
ING_PRTY	Output	Transmit Parity. See UL2 Specification for details.
ING_SOC	Output	Transmit Start-of-Cell. See UL2 Specification for details.
EGR_CLK	Input	Receive Clock. See UL2 Specification for details.
EGR_ADDR(4:0)	Input	Receive Polling Address. See UL2 Specification for details.
EGR_CLAV	Output	Receive Cell Available. See UL2 Specification for details.
EGR_ENB_N	Input	Receive Enable. See UL2 Specification for Details.
EGR_DATA(N:0)	Input	Receive Data, where N is 7 + (8*SIZE_16). See UL2 Specification for details.
EGR_PRTY	Input	Receive Parity. See UL2 Specification for details.
EGR_SOC	Input	Receive Start-of-Cell. See UL2 Specification for details.
WR_CLK	Input	Write Clock. Maximum Frequency is 50 MHz.
WR_DATA(M*N:0)	Input	Write Data Bus, where M*N is NUMPHYS times (8 + (8*SIZE_16)) minus one.
WR_ENB(M:0)	Input	Write Enable, where M is NUMPHYS minus one. Asserted for each write of a valid byte of a cell.
INCREMENT(M:0)	Input	Packet Counter Increment, where M is NUMPHYS minus one. Asserted on the last valid byte of a cell.
A_FULL(M:0)	Output	Almost Full, where M is NUMPHYS minus one. Asserted when the write FIFO does not have enough space for an additional cell.
RD_CLK	Input	Read Clock. Maximum Frequency is 50 MHz.
RD_DATA(M*N:0)	Output	Read Data Bus, where M*N is NUMPHYS times (8 + (8*SIZE_16)) minus one.
RD_ENB(M:0)	Input	Read Enable, where M is NUMPHYS minus one. Asserted for each read of a valid byte of a cell. There is a one clock latency on each read.
DECREMENT(M:0)	Input	Packet Counter Decrement, where M is NUMPHYS minus one. Asserted on the first byte read of a cell.
FLAG(M:0)	Output	Cell Available Flag, where M is NUMPHYS minus one. Asserted when there is at least one cell available to be read.
EGR_PERR	Output	Receive Data Parity Error. Asserted when a parity error was detected on the Receive Data bus.

Table 2: Utopia Level 2 PHY Signal List

Ordering Information

The Utopia Level 2 PHY core is provided under license from Avnet Memec for use in Actel programmable logic devices. Please contact Avnet Memec for pricing and more information.

Related Information

af-phy-0017.000
Dated March 1994, this is the official public specification describing the Utopia Level 1 interface.

af-phy-0039.000
Dated June 1995, this is the official public specification describing the Utopia Level 2 interface by expanding the Utopia Level 1 document.

Utopia Level 2 PHY Users Guide

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Ordering Information:

Part Number	Hardware	Resale
MC-ACT-UL2PHY	Actel UTOPIA Level 2 PHY	Contact for pricing

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