

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 7 μ A
- Ultra low active power
 - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

Functional Description

The CY62136ESL is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that reduces power consumption when addresses are

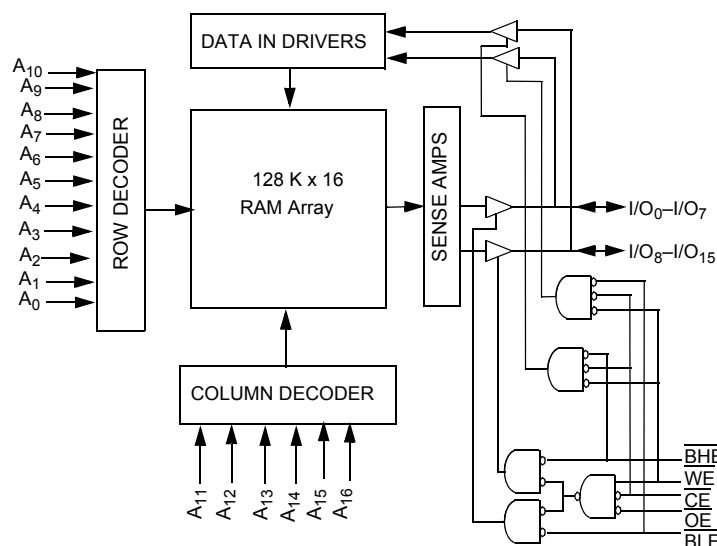
not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the Truth Table on page 11 for a complete description of read and write modes.

The CY62136ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

Logic Block Diagram

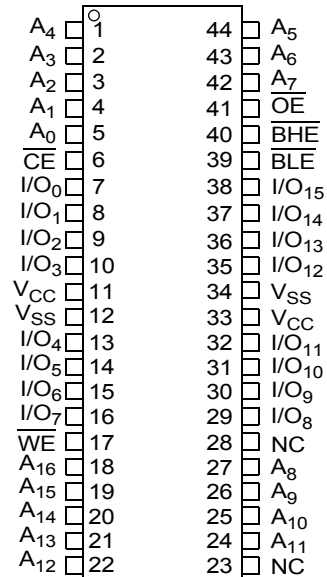


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Pin Configuration

Figure 1. 44-pin TSOP II (Top View) ^[1]



Product Portfolio

Product	Range	V _{CC} Range (V) ^[2]	Speed (ns)	Power Dissipation					
				Operating I _{CC} (mA)				Standby, I _{SB2} (μA)	
				f = 1MHz		f = f _{max} = 1/TRC			
				Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY62136ESL	Industrial	2.2 V to 3.6 V and 4.5 V to 5.5 V	45	2	2.5	15	20	1	7

Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.5 V to 6.0 V
DC voltage applied to outputs in High Z State ^[4, 5]	-0.5 V to 6.0 V
DC input voltage ^[4, 5]	-0.5 V to 6.0 V

Output current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	>2001 V
Latch up current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62136ESL	Industrial	-40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ ^[7]	Max	
V _{OH}	Output HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OH} = -0.1 mA	2.0	-	-	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OH} = -1.0 mA	2.4	-	-	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OH} = -1.0 mA	2.4	-	-	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OH} = -0.1 mA	-	-	3.4 ^[8]	
V _{OL}	Output LOW voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA	-	-	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1 mA	-	-	0.4	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OL} = 2.1 mA	-	-	0.4	
V _{IH}	Input HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7		1.8	-	V _{CC} + 0.3	V
		2.7 ≤ V _{CC} ≤ 3.6		2.2	-	V _{CC} + 0.3	
		4.5 ≤ V _{CC} ≤ 5.5		2.2	-	V _{CC} + 0.5	
V _{IL}	Input LOW voltage	2.2 ≤ V _{CC} ≤ 2.7		-0.3	-	0.6	V
		2.7 ≤ V _{CC} ≤ 3.6		-0.3	-	0.8	
		4.5 ≤ V _{CC} ≤ 5.5		-0.5	-	0.8	
I _{IX}	Input leakage current	GND ≤ V _{in} ≤ V _{CC}		-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , Output disabled		-1	-	+1	μA
I _{CC}	V _{CC} Operating supply current	f = f _{max} = 1/t _{RC}	V _{CC} = V _{CCmax} I _{OUT} = 0 mA, CMOS levels	-	15	20	mA
		f = 1 MHz		-	2	2.5	
I _{SB1} ^[9]	Automatic CE power-down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = f_{max}$ (Address and data only), $f = 0$ (OE, BHE, BLE and WE), $V_{CC} = V_{CC(max)}$		-	1	7	μA
I _{SB2} ^[9]	Automatic CE power-down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$, $V_{CC} = V_{CC(max)}$		-	1	7	μA

Notes

- V_{IL}(min) = -2.0 V for pulse durations less than 20 ns.
- V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.
- Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
- Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

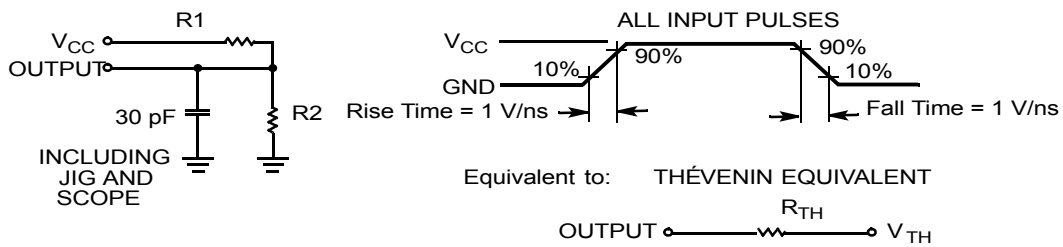
Parameter ^[10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		13	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Note

10. Tested initially and after any design or process changes that may affect these parameters.

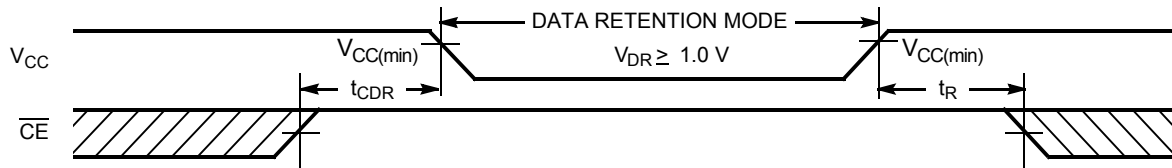
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} ^[12]	Data retention current	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	0.8	3	μA
t_{CDR} ^[13]	Chip deselect to data retention time		0	–	–	ns
t_R ^[14]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^\circ\text{C}$.
12. Chip enable (\overline{CE}) and byte enables (\overline{BHE} and \overline{BLE}) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[15, 16]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[17]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[17, 18]	–	18	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[17]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[17, 18]	–	18	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to ower-down	–	45	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[17]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[17, 18]	–	18	ns
Write Cycle ^[19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE} LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[17, 18]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[17]	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 2 on page 5](#).
16. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See [application note AN13842](#) for further clarification.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
19. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled [20, 21]

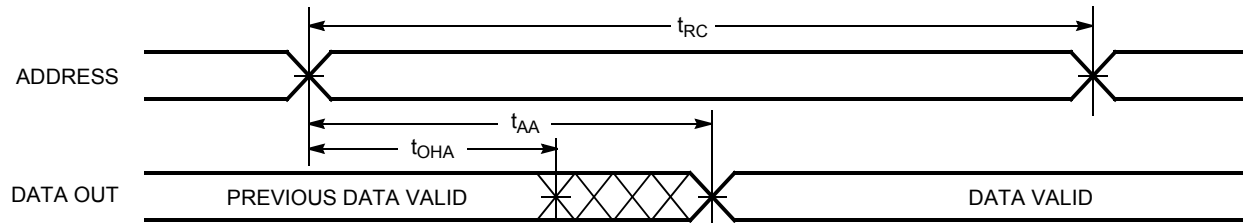
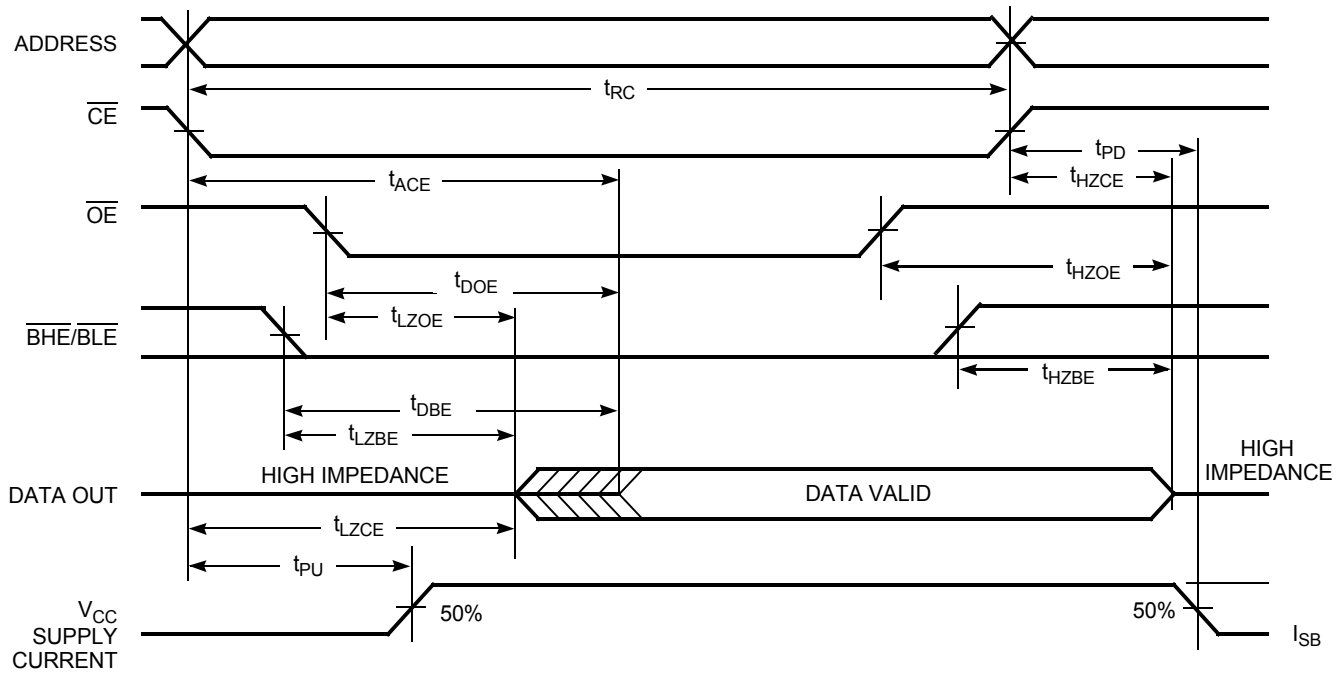


Figure 5. Read Cycle No. 2: \overline{OE} Controlled [21, 22]



Notes

- 20. The device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} , \overline{BHE} , \overline{BLE} , or both = V_{IL} .
- 21. \overline{WE} is HIGH for read cycle.
- 22. Address valid before or similar to \overline{CE} , \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No 1: \overline{WE} Controlled [23, 24, 25]

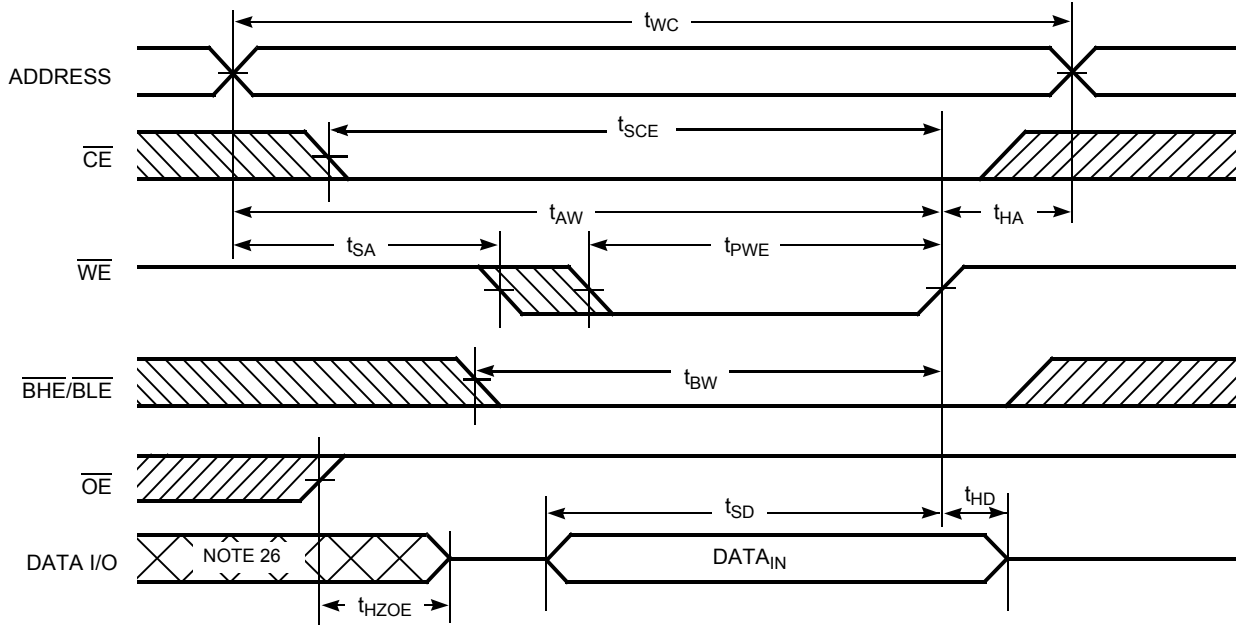
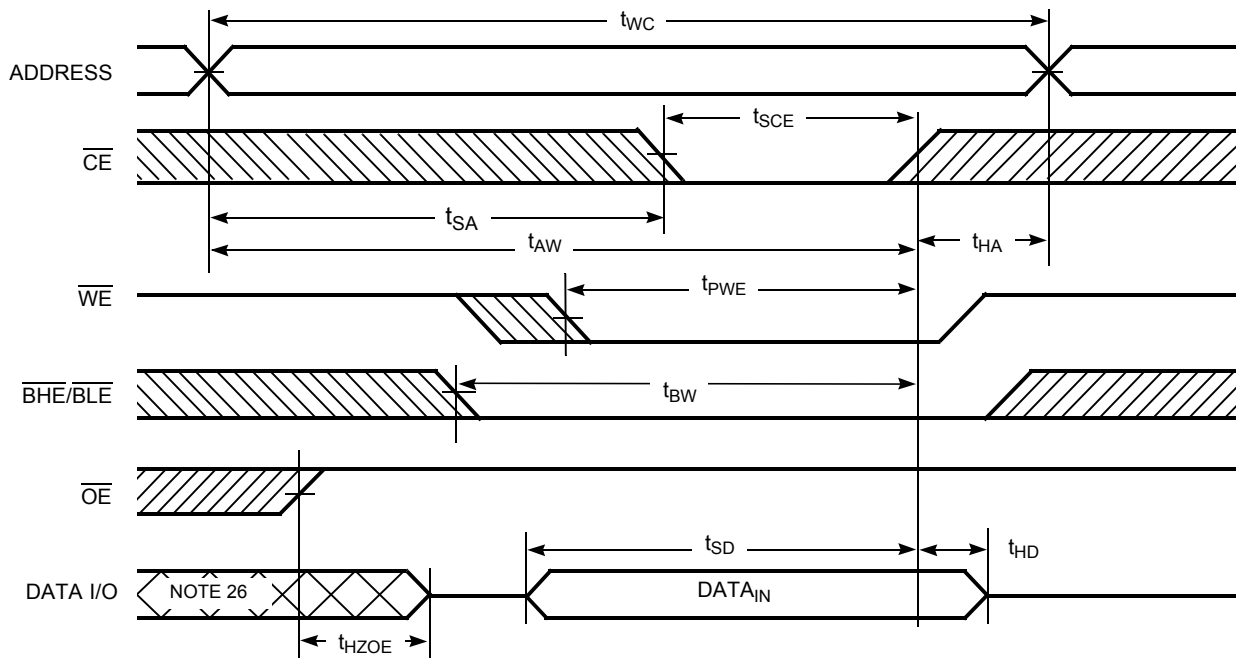


Figure 7. Write Cycle 2: \overline{CE} Controlled [23, 24, 25]



Notes

- 23. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.
- 24. Data I/O is high impedance if $OE = V_{IH}$.
- 25. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle 3: \overline{WE} Controlled, \overline{OE} LOW [27]

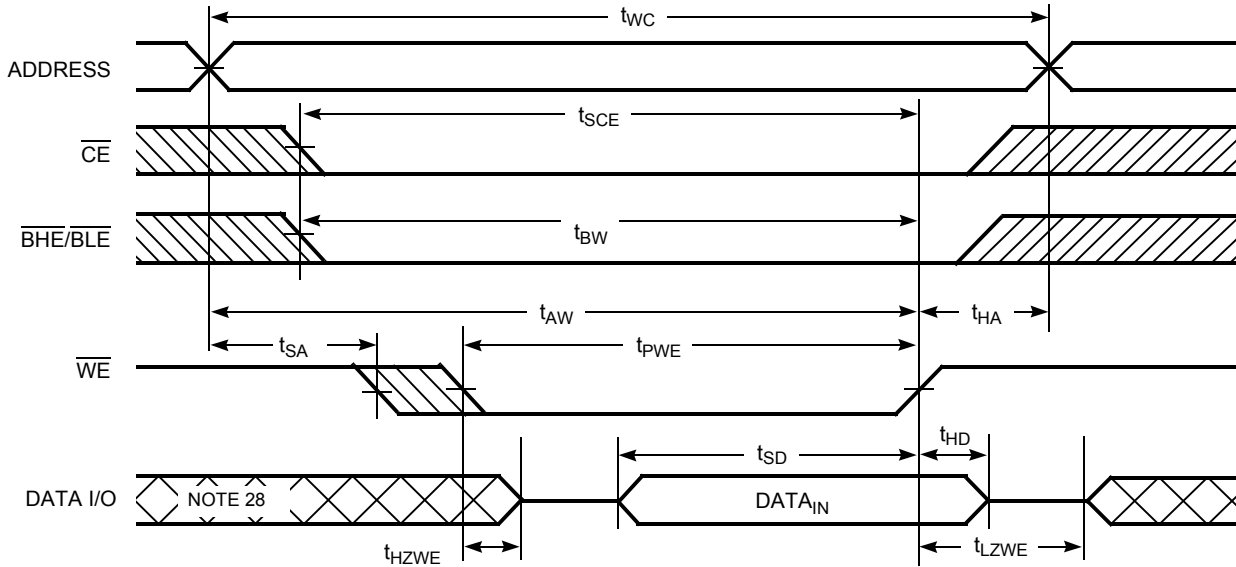
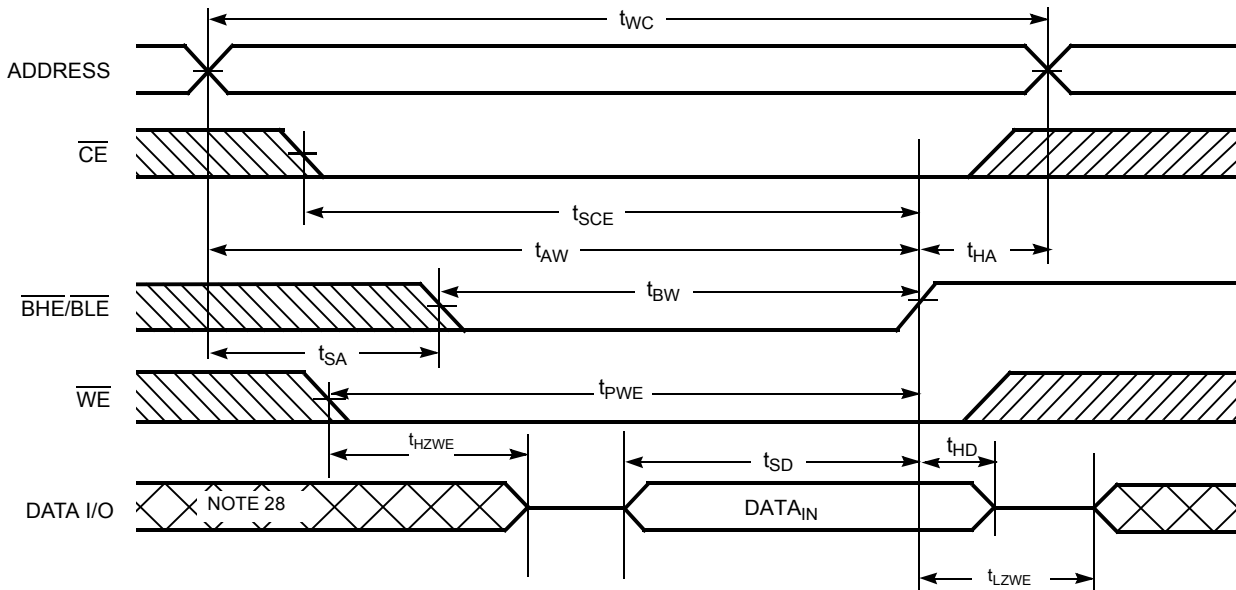


Figure 9. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW [27]



Notes

- 27. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 28. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{\text{CE}}^{[29]}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	$\chi^{[29]}$	$\chi^{[29]}$	High Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

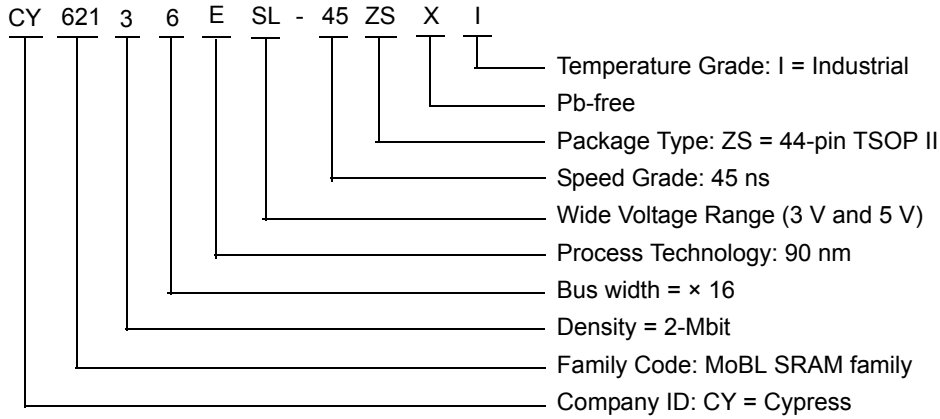
Note

29. The 'X' (Don't care) state for the Chip enable ($\overline{\text{CE}}$) and Byte enables ($\overline{\text{BHE}}$ and $\overline{\text{BLE}}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

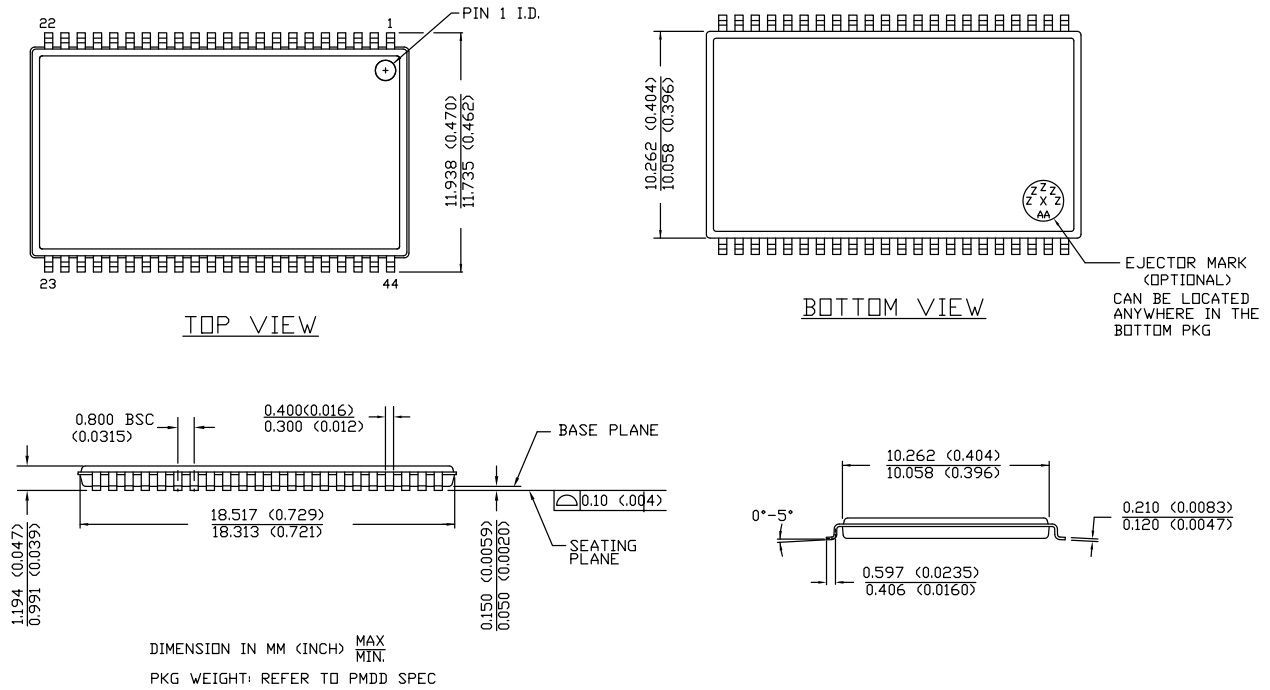
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136ESL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62136ESL MoBL [®] , 2-Mbit (128 K × 16) Static RAM Document Number: 001-48147				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2615537	VKN / PYRS	12/03/08	New data sheet.
*A	2718906	VKN	06/15/2009	Post to external web.
*B	2944332	VKN	06/04/2010	Added Contents Added footnote for I _{SB2} parameter in Electrical Characteristics Added Footnote 2 in Switching Characteristics Added footnote related to Chip enable and Byte enables in Truth Table Updated Package Diagram Updated links in Sales, Solutions, and Legal Information
*C	3126445	RAME	01/03/2011	Updated datasheet as per new template Added Acronyms and Units of Measure . Added Ordering Code Definitions Converted all table note to footnote.
*D	3283711	RAME	06/15/2011	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated in new template.
*E	3499186	TAVA	01/17/2012	Updated Product Portfolio Updated Package Diagram
*F	3874351	NILE	01/18/2013	Updated Package Diagram : spec 51-85087 – Changed revision from *D to *E.
*G	4019657	MEMJ	06/04/2013	Updated Functional Description . Updated Electrical Characteristics : Added one more Test Condition "4.5 ≤ V _{CC} ≤ 5.5, I _{OH} = -0.1 mA" for V _{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 8 and referred the same note in maximum value for V _{OH} parameter corresponding to Test Condition "4.5 ≤ V _{CC} ≤ 5.5, I _{OH} = -0.1 mA".

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