CS61584A

Dual T1/E1 Line Interface

Features

- Dual T1/E1 Line Interface
- 3.3 Volt and 5 Volt Versions
- Crystal-less Jitter Attenuator Meets European CTR 12 and ETSI ETS 300 011 Specifications
- Matched Impedance Transmit Drivers
- Transmitter Tri-state Capability
- Common Transmit and ReceiveTransformers for all Modes
- Serial and Parallel Host Mode Operation
- User-customizable Pulse Shapes
- Supports JTAG Boundary Scan
- Compliant with:
  - ITU-T Recommendations: G.703, G.704, G.706, G.732, G.775 and I.431
  - American National Standards (ANSI): T1.102, T1.105, T1.403, T1.408, and T1.231
  - FCC Rules and Regulations: Part 68 and Part 15
  - AT&T Publication 62411
  - ETSI ETS 300 011, 300 233, CTR 12, TBR 13
- TR-NET-00499

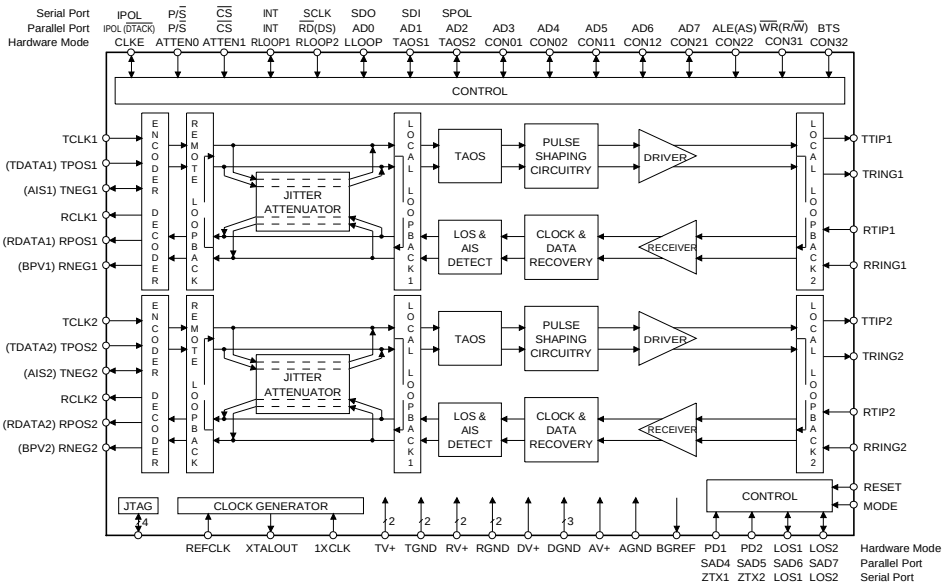
Description

The CS61584A is a dual line interface for T1/E1 applications, designed for high-volume cards where low power and high density are required. The device is optimized for flexible microprocessor control through a serial or parallel Host mode interface. Hardware mode operation is also available.

Matched impedance drivers reduce power consumption and provide substantial transmitter return loss. The transmitter pulse shapes are customizable to allow non-standard line loads. Crystalless jitter attenuation complies with most stringent standards. Support of JTAG boundary scan enhances system testability and reliability.

ORDERING INFORMATION

See page 53.



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1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
DC Supply (TV+1, TV+2, RV+1, RV+2, AV+, DV+) (Note 1)		-	6.0	V
Input Voltage (Any Pin)	V_{in}	RGND - 0.3	(RV+) + 0.3	V
Input Current (Any Pin) (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes: 1. Referenced to RGND1, RGND2, TGND1, TGND2, AGND, DGND at 0 V.

2. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply (TV+1, TV+2, RV+1, RV+2, AV+, DV+) (Note 3)					V
3.3 V		3.135	3.3	3.465	
5.0 V		4.75	5.0	5.25	
Ambient Operating Temperature	T_A	-40	25	85	°C
Power Consumption Per Channel (3.3 V) (Note 4)	P_C				mW
T1 (Note 5)		-	310	-	
T1 (Note 6)		-	190	-	
E1, 75 Ω (Note 5)		-	250	-	
E1, 120 Ω (Note 5)		-	230	-	
Power Consumption Per Channel (5.0 V) (Note 4)	P_C				mW
T1 (Note 5)		-	350	-	
T1 (Note 6)		-	250	-	
E1, 75 Ω (Note 5)		-	320	-	
E1, 120 Ω (Note 5)		-	310	-	
REFCLK Frequency T1 1XCLK = 1		(1.544 - 100 ppm)	1.544	(1.544 + 100 ppm)	MHz
T1 1XCLK = 0		(12.352 - 100 ppm)	12.352	(12.352 + 100 ppm)	MHz
REFCLK Frequency E1 1XCLK = 1		(2.048 - 100 ppm)	2.048	(2.048 + 100 ppm)	MHz
E1 1XCLK = 0		(16.384 - 100 ppm)	16.384	(16.384 + 100 ppm)	MHz

Notes: 3. TV+1, TV+2, AV+, DV+, RV+1, RV+2 should be connected together. TGND1, TGND2, RGND1, GND2, DGND1, DGND2, DGND3 should be connected together.

4. Per channel power consumption while driving line load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

5. Assumes 100% ones density and maximum line length at maximum supply voltage (3.465 V or 5.25 V).

6. Assumes 50% ones density and 300 ft. line length at typical supply voltage (3.3 V or 5.0 V).

Specifications are subject to change without notice

ANALOG CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal.)

Parameter	Symbol	Min	Typ	Max	Unit
Receiver					
RTIP/RRING Differential Input Impedance		-	20	-	kΩ
Sensitivity Below DSX-1 (0 dB = 2.4 V)		-	-13.6	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold T1, DSX-1 (Note 7) (Note 8) T1, FCC Part 68 and E1 (Note 9) (Note 10)		60 55 45 40	65 - 50 -	70 75 55 60	% of Peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance (DSX-1, E1) 10 Hz and below (Note 11) 2 kHz 10 kHz - 100 kHz		 300 6.0 0.4	 - - -	 - - -	UI
Receiver Return Loss (Notes 12, 13, and 14) 51 kHz - 102 kHz 102 kHz - 2.048 MHz 2.048 MHz - 3.072 MHz		 12 18 14	 22 24 22	 - - -	dB
Jitter Attenuator					
Jitter Attenuator Corner Frequency T1 (Notes 12 and 15) E1		 1.25 -	 4.0 1.25	 - -	Hz
Attenuation at 10 kHz Jitter Frequency (Notes 12 and 15)		-	60	-	dB
Attenuator Input Jitter Tolerance (Note 12) (Before Onset of FIFO Overflow or Underflow Protection)		28	43	-	UI_{pk-pk}
Transmitter					
Arbitrary Pulse Amplitude at Transformer Secondary T1, DSX-1 T1, DS1 E1, 75 Ω E1, 120 Ω		 - - - -	 73 52 43 52	 - - - -	mV/LSB

Notes:
7. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
8. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk}, and 4.14 V_{pk} to 5.0 V_{pk}.
9. For input amplitude of 1.07 V_{pk} to 4.14 V_{pk}.
10. For input amplitude of 4.14 V_{pk} to 5.0 V_{pk}.
11. Jitter tolerance increases at lower frequencies. Refer to the Receiver section.
12. Not production tested. Parameters guaranteed by design and characterization.
13. Typical performance using the line interface circuitry recommended in the Applications section.
14. Return loss = 20 $\log_{10}$ ABS(($z_1 + z_0$) / ($z_1 - z_0$)) where z_1 = impedance of the transmitter or receiver, and z_0 = cable impedance.
15. Attenuation measured with sinusoidal input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. Output jitter can increase significantly when more than 28 UI's are input to the attenuator. The jitter attenuator -3 dB knee in T1 mode is selectable for 4.0 Hz or 1.25 Hz. Refer to the Jitter Attenuator section.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter (Continued)					
AMI Output Pulse Amplitudes (Note 16)					V
E1, 75 Ω (Note 17)		2.14	2.37	2.6	
E1, 120 Ω (Note 18)		2.7	3.0	3.3	
T1, DSX-1 (Note 19)		2.4	3.0	3.6	
Recommended Transmitter Output Load (3.3 V) (Note 16)					Ω
T1		-	24.8	-	
E1, 75 Ω		-	18.6	-	
E1, 120 Ω		-	30.0	-	
Recommended Transmitter Output Load (5.0 V) (Note 16)					Ω
T1		-	76.6	-	
E1, 75 Ω		-	57.4	-	
E1, 120 Ω		-	90.6	-	
Jitter Added During Remote Loopback					UI
10 Hz - 8 kHz		-	0.020	-	
8 kHz - 40 kHz		-	0.015	-	
10 Hz - 40 kHz		-	0.015	-	
Broad Band (Note 20)		-	0.045	-	
Power in 2 kHz band about 772 kHz (Notes 12 and 13) (DSX-1 only)		12.6	15	17.9	dBm
Power in 2 kHz band about 1.544 MHz (Note 12 and 13) (referenced to power in 2 kHz band at 772 kHz, DSX-1 only)		-29	-38	-	dB
Positive to Negative Pulse Imbalance (Notes 12 and 13)					
T1, DSX-1		-	0.2	0.5	dB
E1, amplitude at center fo pulse interval		-5	-	5	%
E1, width at 50% of nominal amplitude		-5	-	5	%
Transmitter Return Loss (Notes 12, 13, and 14)					dB
51 kHz - 102 kHz		8	25	-	
102 kHz - 2.048 MHz		14	18	-	
2.048 MHz - 3.072 MHz		10	12	-	
E1 Short Circuit Current 5.0 V (Note 21)		-	-	50	mA_{rms}
3.3 V		-	70	-	mA_{rms}
E1 and DSX-1 Output Pulse Rise/Fall Times (Note 22)		-	50	-	ns
E1 Pulse Width (at 50% of peak amplitude)		-	244	-	ns
E1 Pulse Amplitude for a space E1, 75 Ω		-0.237	-	0.237	V
E1, 120 Ω		-0.3	-	0.3	V

Notes: 16. Using a transformer that meets the specifications in the Applications section.

17. Measured across 75 Ω at the output of the transmit transformer for CON3/2/1/0 = 0/0/0/0.

18. Measured across 120 Ω at the output of the transmit transformer for CON3/2/1/0 = 0/0/0/1.

19. Measured at the DSX-1 Cross-Connect for line length settings CON3/2/1/0 = 0/0/1/0, 0/0/1/1, 0/1/0/0, 0/1/0/1, and 0/1/1/0 after the length of #22 ABAM cable specified in Table 1.

20. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.

21. Transformer secondary shorted with 0.5 Ω resistor during the transmission of 100% ones.

22. At transformer secondary and measured from 10% to 90% of amplitude.

DIGITAL CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal.)

Parameter		Symbol	Min	Max	Unit
High-Level Input Voltage	(Note 23)	V_{IH}	(DV+) - 0.5	-	V
Low-Level Input Voltage	(Note 23)	V_{IL}	-	0.5	V
High-Level Output Voltage (I_{out} = -40 µA)	(Note 24)	V_{OH}	(DV+) - 0.3	-	V
Low-Level Output Voltage (I_{out} = 1.6 mA)	(Note 24)	V_{OL}	-	0.3	V
Input Leakage Current (Digital pins except J-TMS and J-TDI)			-	±10	µA

Notes: 23. Digital inputs are designed for CMOS logic levels.

24. Digital outputs are TTL compatible and drive CMOS levels into a CMOS load.

SWITCHING CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal; Inputs: Logic 0 = 0 V, Logic 1 = DV+.)

Parameter		Symbol	Min	Typ	Max	Unit
T1 Clock/Data						
TCLK Frequency	(Note 25)	f_{tclk}	-	1.544	-	MHz
TCLK Duty Cycle		t_{pwh2}/t_{pw2}	20	50	80	%
RCLK Duty Cycle	(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time (All Digital Outputs)	(Note 27)	t_r	-	-	65	ns
Fall Time (All Digital Outputs)	(Note 27)	t_f	-	-	65	ns
RPOS/RNEG (RDATA) to RCLK Rising Setup Time		t_{su1}	-	274	-	ns
RCLK Rising to RPOS/RNEG (RDATA) Hold Time		t_{h1}	-	274	-	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
E1 Clock/Data						
TCLK Frequency	(Note 25)	f_{tclk}	-	2.048	-	MHz
TCLK Duty Cycle		t_{pwh2}/t_{pw2}	20	50	80	%
RCLK Duty Cycle	(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time (All Digital Outputs)	(Note 27)	t_r	-	-	65	ns
Fall Time (All Digital Outputs)	(Note 27)	t_f	-	-	65	ns
RPOS/RNEG (RDATA) to RCLK Rising Setup Time		t_{su1}	-	194	-	ns
RCLK Rising to RPOS/RNEG (RDATA) Hold Time		t_{h1}	-	194	-	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns

Notes: 25. The maximum burst rate of a gapped TCLK input clock is 8.192 MHz. For the gapped clock to be tolerated by the CS61584A, the jitter attenuator must be switched to the transmit path of the line interface. The maximum gap size that can be tolerated on TCLK is 28 UIp-p.

26. RCLK duty cycle may be outside the specified limits when the jitter attenuator is in the transmit path and when the jitter attenuator is employing the overflow/underflow protection mechanism.

27. At max load of 50 pF.

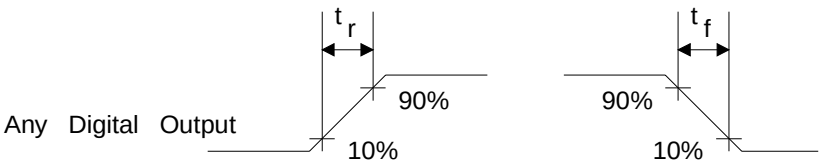


Figure 1. Signal Rise And Fall Characteristics

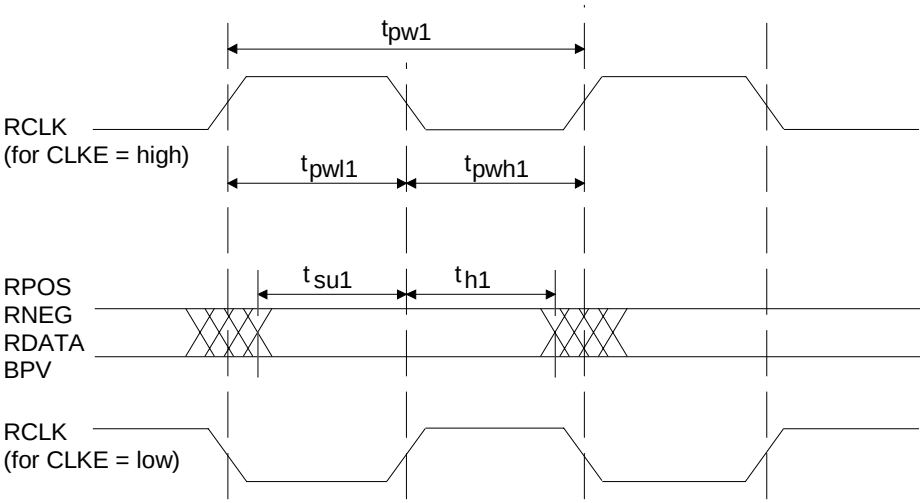


Figure 2. Recovered Clock and Data Switching Characteristics

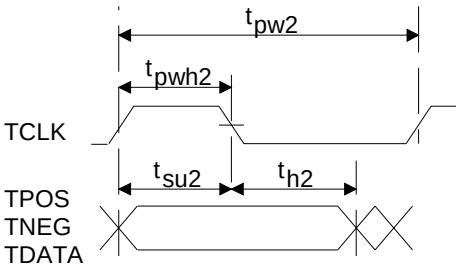


Figure 3. Transmit Clock and Data Switching Characteristics

SWITCHING CHARACTERISTICS - SERIAL PORT (T_A = -40 to 85 °C; DV+, TV+, RV+ = nominal ± 0.3 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Unit
SDI to SCLK Setup Time	t_{dc}	25	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	25	-	-	ns
SCLK Low Time	t_{cl}	50	-	-	ns
SCLK High Time	t_{ch}	50	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	15	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	20	-	-	ns
SCLK to $\overline{CS}$ Hold Time (Note 28)	t_{cch}	20	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	100	-	-	ns
SDO Valid to SCLK (Note 29)	t_{cdv}	-	-	50	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	50	-	ns

Notes: 28. If SPOL = 0, then $\overline{CS}$ should return high no sooner than 20 ns after the 16th rising edge of SCLK during a serial port read.

29. Output load capacitance = 50 pF.

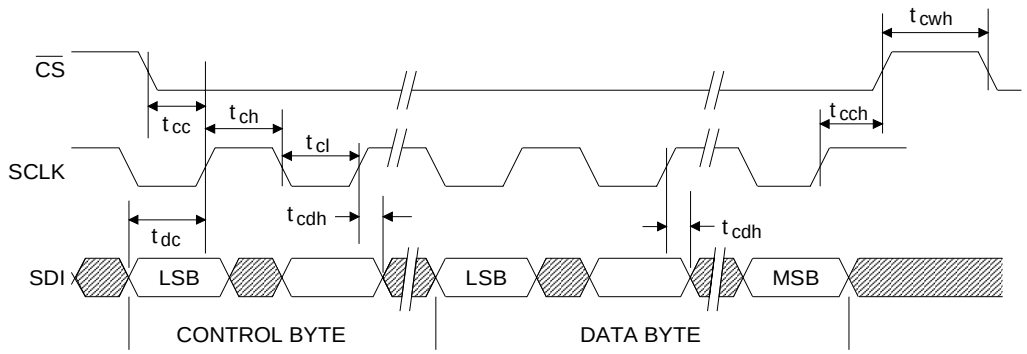


Figure 4. Serial Port Write Timing Diagram

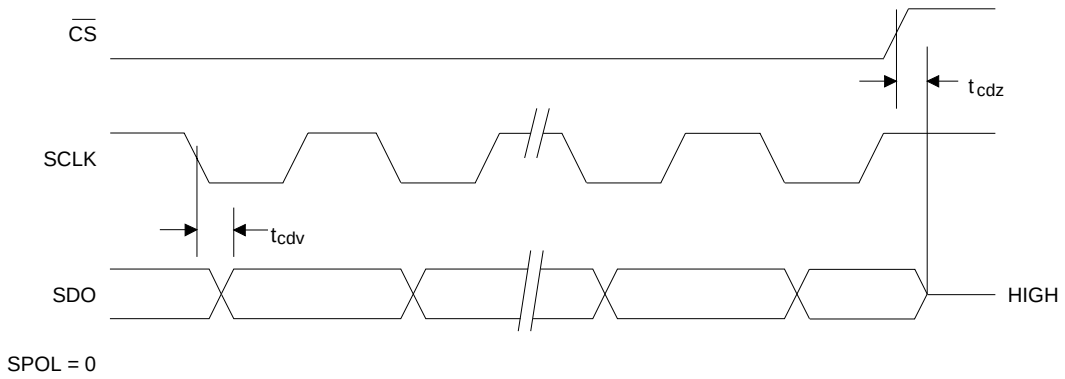


Figure 5. Serial Port Read Timing Diagram

SWITCHING CHARACTERISTICS - PARALLEL PORT (T_A = -40 to 85 °C;

TV+, RV+ = nominal ± 0.3 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+)

Parameter	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	250	-	ns
Pulse Width, DS Low or $\overline{RD}$ High	PW_{el}	150	-	ns
Pulse Width, DS High or $\overline{RD}$ Low	PW_{eh}	150	-	ns
Input Rise/Fall Times	t_r, t_f	-	30	ns
R/$\overline{W}$ Hold Time	t_{rwh}	10	-	ns
R/$\overline{W}$ Setup Time Before DS High	t_{rws}	50	-	ns
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$ Active	t_{cs}	50	-	ns
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$ Active for RAM/ROM	t_{csr}	130	-	ns
$\overline{CS}$ Hold Time	t_{ch}	20	-	ns
Read Data Hold Time	t_{dhr}	10	80	ns
Write Data Hold Time	t_{dhw}	5	-	ns
Muxed Address Valid to AS or ALE Fall	t_{asl}	15	-	ns
Muxed Address Hold Time	t_{ahl}	10	-	ns
Delay Time DS, $\overline{WR}$, or $\overline{RD}$ to AS or ALE Rise	t_{asd}	25	-	ns
Pulse Width AS or ALE High		40	-	ns
Delay Time AS or ALE to DS, $\overline{WR}$, or $\overline{RD}$	t_{ased}	40	-	ns
Output Data Delay Time from DS or $\overline{RD}$	t_{ddr}	20	120	ns
Data Setup Time	t_{dsw}	80	-	ns
$\overline{DTACK}$ Delay	t_{dkd}	5	-	ns
$\overline{DTACK}$ Hold Time	t_{dkh}	5	-	ns
AS/ALE Min Low Interval for RAM/ROM	t_{aamir}	50	-	ns

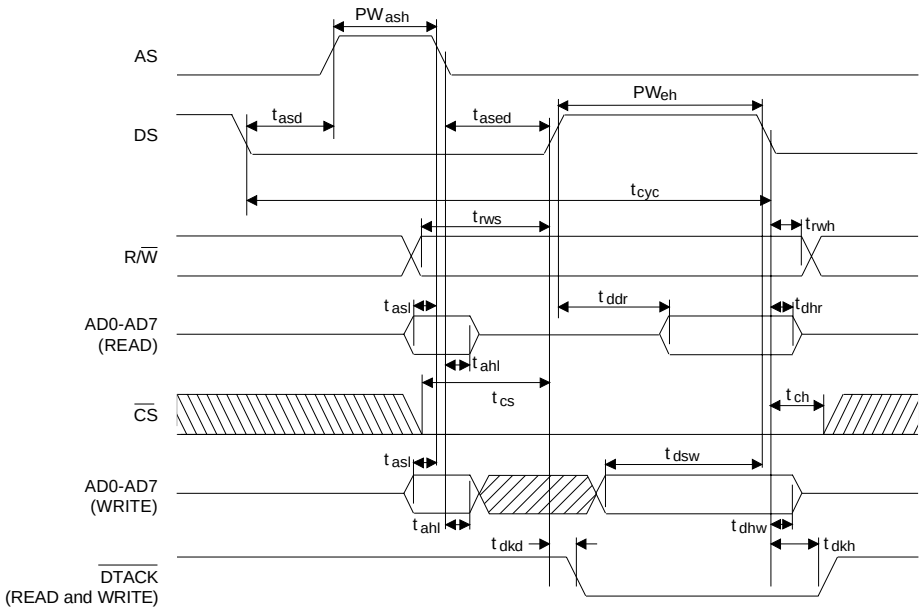


Figure 6. Parallel Port Timing - Motorola Mode

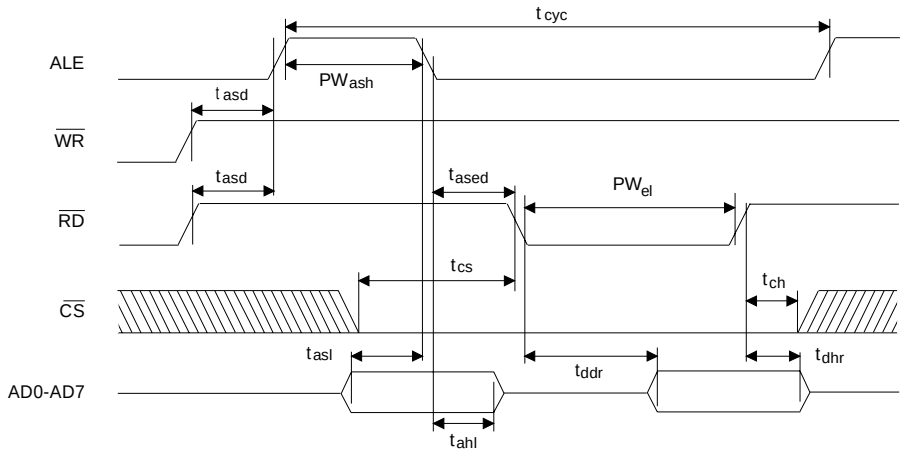


Figure 7. Parallel Port Timing - Intel Read Mode

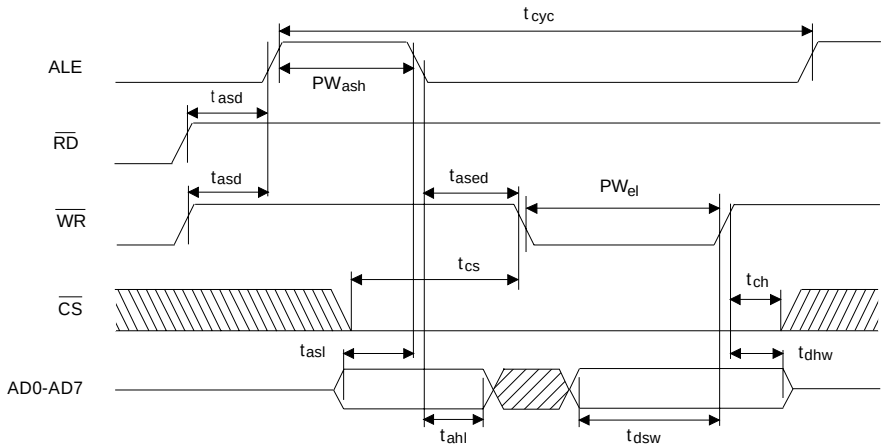


Figure 8. Parallel Port Timing - Intel Write Mode

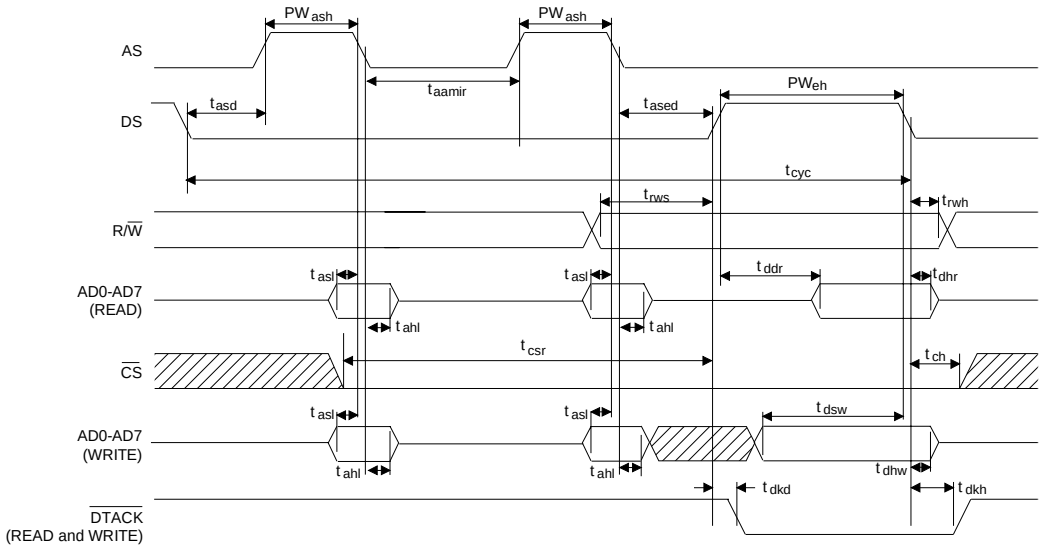


Figure 9. Parallel Port Timing - Motorola Mode to RAM

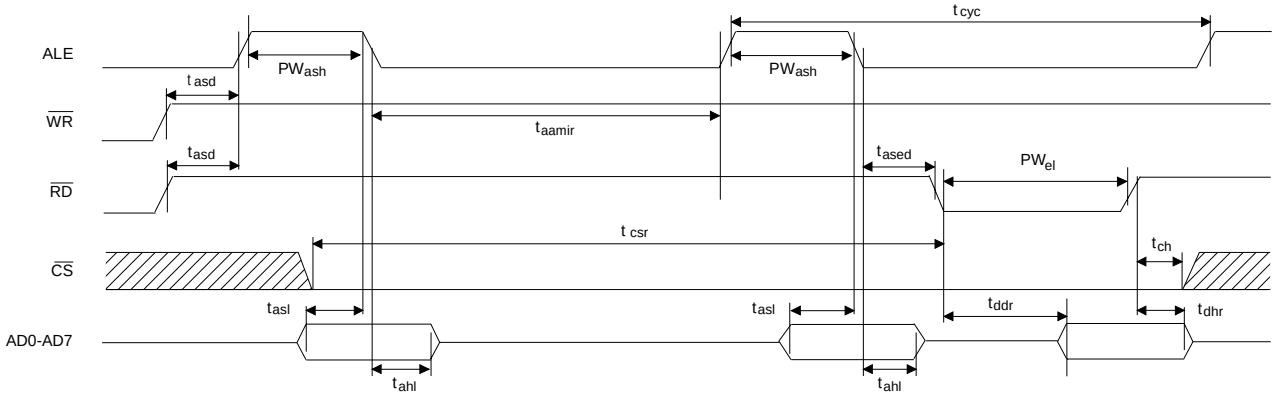


Figure 10. Parallel Port Timing - Intel Read Mode from RAM or ROM

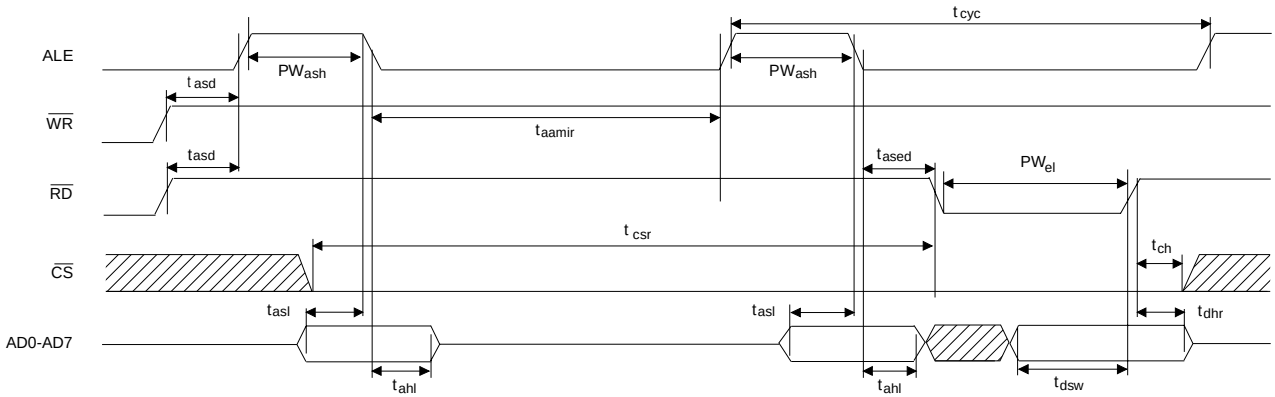


Figure 11. Parallel Port Timing - Intel Write Mode to RAM

SWITCHING CHARACTERISTICS - JTAG (T_A = -40 to 85 °C; TV+, RV+ = nominal ± 0.3 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+)

Parameter	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	200	-	ns
J-TMS/J-TDI to J-TCK Rising Setup Time	t_{su}	50	-	ns
J-TCK Rising to J-TMS/J-TDI Hold Time	t_h	50	-	ns
J-TCK Falling to J-TDO Valid	t_{dv}	-	60	ns

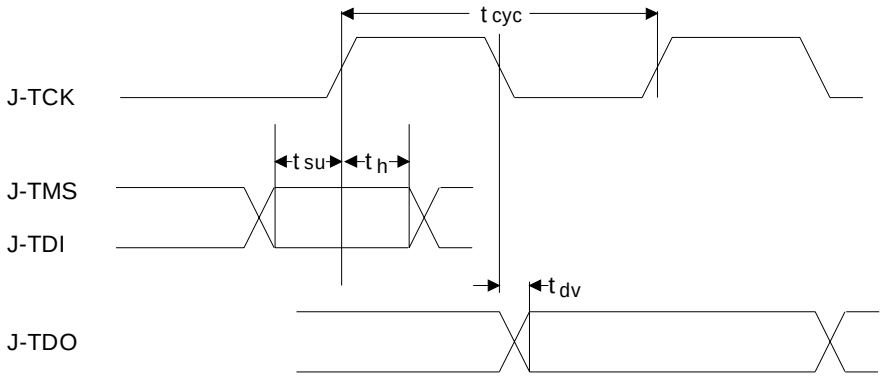


Figure 12. JTAG Switching Characteristics

2. OVERVIEW

The CS61584A is a dual line interface for T1/E1 applications, designed for high-volume cards where low power and high density are required. The device can be operated in either Hardware mode using control pins or in Host mode using an internal register set. One board design can support all T1/E1 short-haul modes by only changing component values in the receive and transmit paths (if REFCLK and TCLK are connected externally). Figure 13 illustrates applications of the CS61584A in various environments.

The line driver generates waveforms compatible with E1 (CCITT G.703), T1 short haul (DSX-1) and T1 FCC Part 68 Option A (DS1). A single transformer turns ratio is used for all waveform types. The driver internally matches the impedance of the load, providing excellent return loss to insure superior T1/E1 pulse quality. An additional benefit of the internal impedance matching is a 50 percent reduction in power consumption compared to implementing return loss using external resistors that causes the transmitter to drive the equivalent of two line loads.

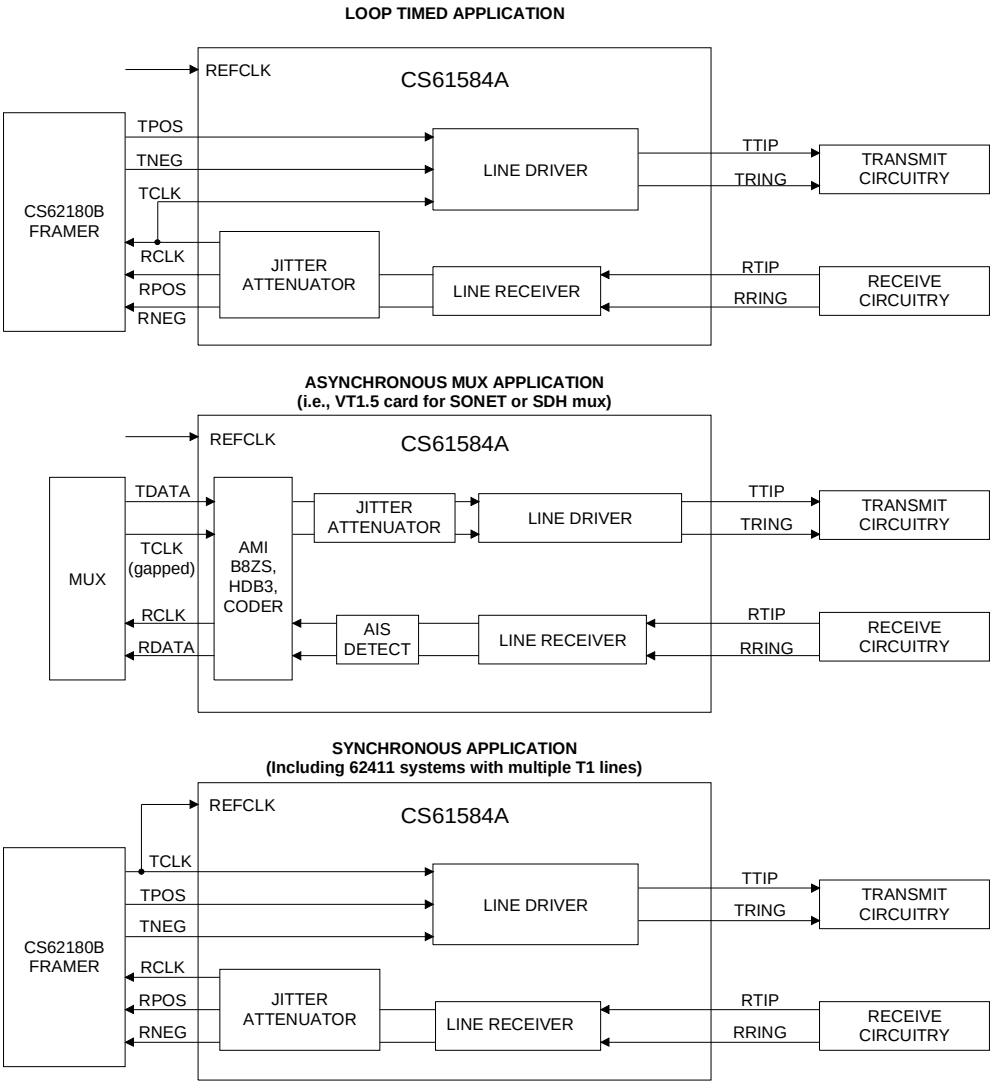


Figure 13. Examples of CS61584A Applications

The line receiver contains all the necessary clock and data recovery circuits.

The jitter attenuator meets AT&T 62411 requirements when using either a 1X or 8X reference clock supplied by either a quartz crystal, crystal oscillator, or external reference at the REFCLK input pin.

2.1 AT&T 62411 Customer Premises Application

The AT&T 62411 specification applies to the T1 interface between the customer premises and the carrier, and must be implemented by the customer premises equipment in order to connect to the AT&T network.

In 62411 applications, the management of jitter is a very important design consideration. Typically, the jitter attenuator is placed in the receive path of the CS61584A to reduce the jitter input to the system synchronizer. The jitter attenuated recovered clock is used as the input to the transmit clock to implement a loop-timed system. A Stratum 4 (±32 ppm) quality clock or better should be input to REFCLK. Note that any jitter present on the reference clock will not be filtered by the jitter attenuator.

2.2 Asynchronous Multiplexer Application

Asynchronous multiplexers accept multiple T1/E1 lines (which are asynchronous to each other), and combine them into a higher speed transmission rate (e.g. M13 muxes and SONET muxes). In these systems, the jitter attenuator is placed in the transmit path of the CS61584A to remove the gapped clock jitter input by the multiplexer to TCLK. Because the transmit clock is jittered, the reference clock to the CS61584A is provided by an external source operating at 1X or 8X the data rate. Because T1/E1 framers are not usually required in asynchronous multiplexers, the B8ZS/AMI/HDB3 coders in the CS61584A are activated to provide data interfaces on TDATA and RDATA.

2.3 Synchronous Application

A typical example of a synchronous application is a T1 card in a central office switch or a 0/1 digital cross-connect system. These systems place the jitter attenuator in the receive path to reduce the jitter presented to the system. A Stratum 3 or better system clock is input to the CS61584A transmit and reference clocks.

3. TRANSMITTER

The transmitter accepts data from a T1 or E1 system and outputs pulses of appropriate shape to the line. The transmit clock (TCLK) and transmit data (TPOS and TNEG, or TDATA) are supplied synchronously. Data is sampled on the falling edge of the TCLK input.

During Hardware mode operation, the configuration pins (CON[3:0]) control transmitted pulse shapes, transmitter source impedance, receiver slicing level, and driver tristate as shown in Table 1. During Host mode operation, the configuration is established by the CON[3:0] bits in the Control B registers. Typical output pulses are shown in Figures 14 and 15. These pulse shapes are fully pre-defined by circuitry in the CS61584A, and are fully compliant with appropriate standards when used with our application guidelines in standard installations. Both channels must be operated at the same line rate (both T1 or both E1).

Host mode operation permits arbitrary transmit pulse shapes to be created and downloaded to the CS61584A. These custom pulse shapes can be used to compensate for waveform degradation caused by non-standard cables, transformers, or protection circuitry (refer to the Arbitrary Waveform Registers section).

Note that the pulse width for Part 68 Option A (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61584A automatically adjusts the pulse width based on the configuration selection.

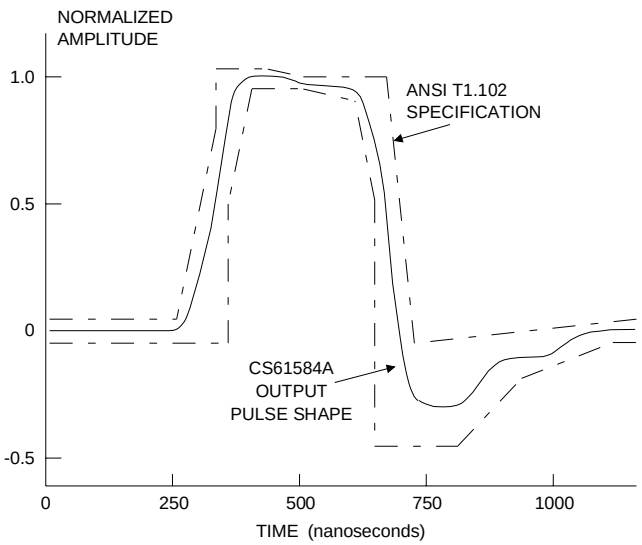


Figure 14. Typical Pulse Shape at DSX-1 Cross Connect

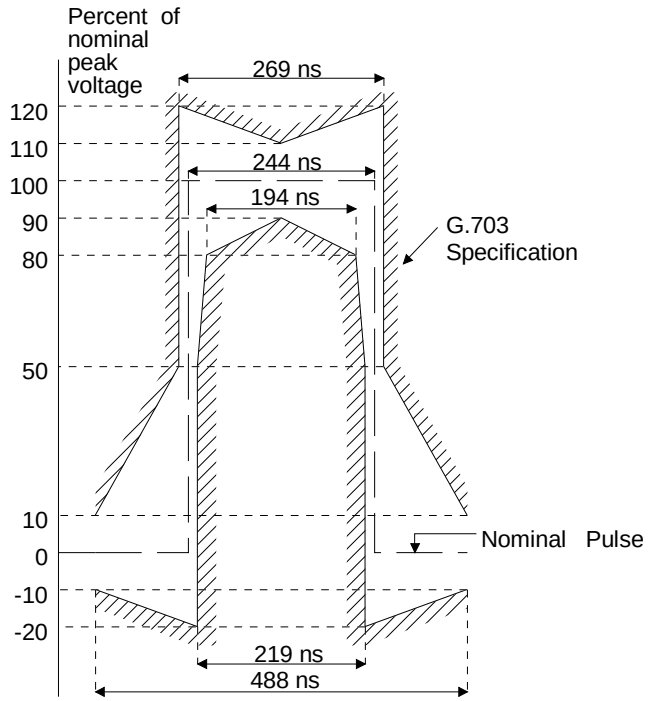


Figure 15. Mask of the Pulse at the 2048 kbps Interface

CON3	CON2	CON1	CON0	Transmit Pulse Width at 50% Amplitude	Transmit Pulse Shape	Receiver Slicing Level	Line Code Encoder / Decoder
0	0	0	0	244 ns (50%)	E1: square, 2.37 V into 75 Ω	50%	AMI/HDB3
1	0	0	0	244 ns (50%)	Arbitrary E1 Wave into 75 Ω	50%	AMI/HDB3
0	0	0	1	244 ns (50%)	E1: square, 2.37 V into 75 Ω	50%	AMI/HDB3
1	0	0	1	244 ns (50%)	Arbitrary E1 Wave into 120 Ω	50%	AMI/HDB3
0	0	1	0	350 ns (54%)	DSX-1: 0-133 ft.	65%	AMI/B8ZS
0	0	1	1	350 ns (54%)	DSX-1: 133-266 ft.	65%	AMI/B8ZS
0	1	0	0	350 ns (54%)	DSX-1: 266-399 ft.	65%	AMI/B8ZS
0	1	0	1	350 ns (54%)	DSX-1: 399-533 ft.	65%	AMI/B8ZS
0	1	1	0	350 ns (54%)	DSX-1: 533-655 ft.	65%	AMI/B8ZS
1	0	1	0	350 ns (54%)	Arbitrary DSX-1 Waveform	65%	AMI/B8ZS
0	1	1	1	324 ns (50%)	DS1: FCC Part 68 Option A with undershoot	65%	AMI/B8ZS
1	1	0	0	324 ns (50%)	DS1: FCC Part 68 Option A (0 dB)	65%	AMI/B8ZS
1	0	1	1	324 ns (50%)	Arbitrary DS1 Waveform	65%	AMI/B8ZS
1	1	0	1	Reserved			
1	1	1	0	Transmit Hi Z	Tristate TTIP/TRING Driver Outputs	50%	AMI/HDB3
1	1	1	1	Transmit Hi Z	Tristate TTIP/TRING Driver Outputs	65%	AMI/B8ZS

Table 1. Line Configuration Selections

The transmitter impedance changes with the line length options in order to match the load impedance (75 Ω for E1 coax, 100 Ω for T1, 120 Ω for E1 shielded twisted pair), providing a minimum of 14 dB return loss for T1 and E1 frequencies during the transmission of both marks and spaces. This improves signal quality by minimizing reflections from the transmitter. Impedance matching also reduces load power consumption by a factor of two when compared to the return loss achieved by using external resistors.

The CS61584A driver will automatically detect an inactive TLCK (i.e., no data clocked to the driver) or REFCLK input. When either of these conditions are detected the driver is forced to the tristate (high-impedance) condition. If the jitter attenuator is in the transmit path, the driver will tristate after 170 to 182 TCLK clock cycles. If the attenuator is not in the transmit path, the driver will tristate after 4 to 12 TCLK clock cycles. During Host mode operation, the CLKLOST bit in the Status register goes high to indicate when the driver is tristated due to the absence of TCLK or REFCLK. The driver exits the tristate condition when four clock cycles are input to TCLK. On power-up or reset, the driver is tristated until REFCLK is present and four clock cycles are input to TCLK. In Host mode the driver will have to be taken out of the tristate condition by writing the CON[3:0]. The driver is not forced to the tristate condition during remote loopback if TCLK is absent.

When the transmit configuration established by CON[3:0], TAOS, or LLOOP changes state, the transmitter stabilizes within 22 TCLK bit periods. The transmitter takes longer to stabilize when RLOOP1 or RLOOP2 is selected because the timing circuitry must adjust to the new frequency from RCLK.

When the transmitter transformer secondaries are shorted through a 0.5 Ω resistor, the transmitter will output a maximum of 50 mA-rms, as required by the European specification BS6450. This spec is met for 5.0 V operation only.

4. RECEIVER

The input signal is connected to the receiver through a step down transformer (1.15:1 for 5 V and 2:1 for 3.3 V). Data and clock are extracted from the T1/E1 signal input to the line interface and to the system. The signal is detected differentially across the receive transformer and can be recovered over the entire range of short haul cable lengths. The transmit and receive transformer specifications are identical and are presented in the Applications section. As shown in Table 1, the receiver slicing level is set at 65% for DS1/DSX-1 short-haul and at 50% for all other applications.

The clock recovery circuit is a second-order phase locked loop that can tolerate up to 0.4 UI of jitter from 10 kHz to 100 kHz without generating errors (Figure 13). The clock and data recovery circuit is tolerant of long strings of consecutive zeros and will successfully recover a 1-in-175 jitter-free line input signal.

Recovered data at RPOS and RNEG (or RDATA) is stable and may be sampled using the recovered clock RCLK. During Hardware mode operation,

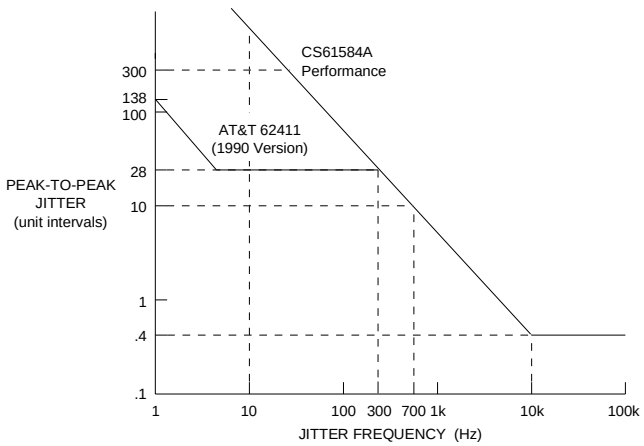


Figure 16. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and jitter Attenuator)

the CLKE pin determines the clock polarity where the output data is stable and valid as shown in Table 2. During Host mode operation, the polarity is established by the CLKE bit in the Control A register. When CLKE is low, RPOS and RNEG (or RDATA) are valid on the rising edge of RCLK. When CLKE is high, RPOS and RNEG (or RDATA) are valid on the falling edge of RCLK

During Host mode operation, the data at RPOS and RNEG (or RDATA) may be forced to output an unframed all-ones pattern by setting both the LLOOP1 and LLOOP2 bits in the Control B register to "1".

CLKE	DATA	CLOCK	Clock edge for valid data
LOW	RPOS, RNEG or RDATA	RCLK RCLK	Rising Rising
HIGH	RPOS, RNEG or RDATA	RCLK RCLK	Falling Falling

Table 2. Recovered Data/Clock Options

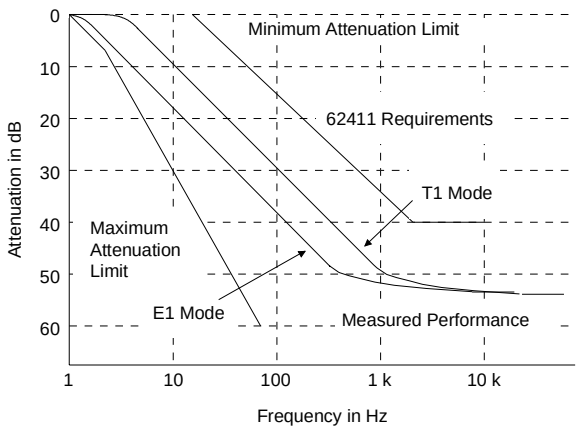


Figure 17. Typical Jitter Transfer Function

5. JITTER ATTENUATOR

The jitter attenuator can be switched into either the receive or transmit paths. Alternatively, it can also be removed from both paths to reduce the propagation delay. Figure 14 illustrates the typical jitter attenuation curves.

During Hardware mode operation, the location of the jitter attenuators for both channels is controlled by the ATTEN0 and ATTEN1 pins. During Host mode operation, the location of the jitter attenuators are independent and are controlled by the ATTEN[1:0] bits in the Control A registers. Table 3 shows how these pins are decoded.

The attenuator consists of a 64-bit FIFO, a narrowband monolithic PLL, and control logic. Signal jitter is absorbed in the FIFO which is designed to neither overflow nor underflow. If overflow or underflow is imminent, the jitter transfer function is altered to ensure that no bit-errors occur. Under this condition, jitter gain may occur and external provisions may be required. The jitter attenuator will typically tolerate 43 UIs before the overflow/underflow mechanism occurs. If the jitter attenuator has not had time to "lock" to the average incoming frequency (e.g. following a device reset) the attenuator will tolerate a minimum of 22 UIs before the overflow/underflow mechanism occurs.

The jitter attenuator -3 dB knee frequency is 4.0 Hz for T1 mode and 1.25 Hz for E1 mode as selected by the CON[3:0] pins or register bits. A 1.25 Hz knee for the E1 mode guarantees jitter attenuation compliance to European specifications CTR 12 and ETSI ETS 300 011. Setting ATTEN[1:0] = 11 will place the jitter attenuator in the receive path with a 1.25 Hz knee for both T1 and E1 modes of operation.

For T1/E1 line cards used in high-speed mutiplexers (e.g., SONET and SDH), the jitter attenuator is typically used in the transmit path. The attenuator can accept a transmit clock with gaps ≤ 28 UIs and a transmit clock burst rate of ≤ 8 MHz.

ATTEN1	ATTEN0	Location of Jitter Attenuator
0	0	Receiver
0	1	Disabled
1	0	Transmitter
1	1	Receiver w/ 1.25 Hz knee

Table 3. Jitter Attenuation Control

6. REFERENCE CLOCK

The CS61584A requires a reference clock with a minimum accuracy of ±100 ppm for T1 and E1 applications. This clock can be either a 1X clock (i.e., 1.544 MHz or 2.048 MHz), or can be a 8X clock (i.e., 12.352 MHz or 16.384 MHz) as selected by the 1XCLK pin. This clock may be supplied from internal system timing or a CMOS crystal oscillator and input to the REFCLK pin. An 8X quartz crystal may be connected across the REFCLK and XTALOUT pins and the 1XCLK pin set low. The quartz crystal and CMOS crystal oscillator specifications and are presented in the Applications section.

In systems with a jittered transmit clock, the reference clock should not be tied to the transmit clock and a separate external quartz crystal or crystal oscillator should drive the reference clock input. Any jitter present on the reference clock will not be filtered by the jitter attenuator.

7. POWER-UP RESET

On power-up, the device is held in a static state until the power supply achieves approximately 60% of the power supply voltage. When this threshold is crossed, the device waits another 10 ms to allow the power supply to reach operating voltage and then calibrates the transmit and receive circuitry. This initial calibration takes less than 20 ms but can occur only if REFCLK and TCLK are present.

Power-up reset initializes the control logic and register set and performs the same functions as the RESET pin. During Host mode operation, a reset event is indicated by the Latched-Reset bit in the Status register.

8. LINE CONTROL AND MONITORING

Line control and monitoring of the CS61584A may be implemented in either Hardware or Host mode. Hardware mode is selected when the MODE pin is set low and allows the device to be configured and monitored using control pins. Host mode is selected when the MODE pin is set high and allows the device to be configured and monitored using an internal register set.

The following controls and indications are available in Hardware mode: line length selection, receive clock edge, jitter attenuator location, loss of signal, transmit all ones, local loopback, remote loopback, and power down. Host mode operation offers several additional control options (refer to the Host Mode section).

Note: Please refer to the Loop Selection Equations in the Applications section.

8.1 Line Code Encoder/Decoder

Hardware mode supports only transparent operation to permit the line code to be encoded and decoded by an external T1/E1 framing device. Recovered data is output on the RNEG and RPOS pins in NRZ format and transmitted data is input on the TNEG and TPOS pins.

Host mode supports transparent, AMI, B8ZS, or HDB3 line encoding and decoding for applications not using an external T1/E1 framer (i.e. multiplexers). The CODER, AMI-T, and AMI-R bits in the Control A registers select the coder mode for a given channel. The selection of the transmit encoder is independent from the selection of the receive decoder. When CODER = 1, the transmit data is input to the encoder on TDATA and the receive data is output from the decoder on RDATA in NRZ format.

8.2 Alarm Indication Signal

During Host mode operation, the alarm indication signal (AIS) is detected by the receiver and reported using the AIS and Latched-AIS bits in the Status registers. The receiver detects the AIS condition on observation of 99.9% ones density in a 5.3 ms period (< 9 zeros in 8192 bits). If CODER = 1 in the Control A registers, the TNEG pin becomes the AIS output pin that is set high on detection of AIS. The AIS condition is exited when ≥ 9 zeros are detected in 8192 bits.

8.3 Bipolar Violation Detection

During Host mode operation, a bipolar violation (BPV) is detected by the receiver and reported using the Latched-BPV bit in the Status registers. If CODER = 1 in the Control A registers, the RNEG pin becomes the BPV output strobe pin that is set high for one bit period on detection of a BPV. Note that B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled (CODER = 1 and AMI-R = 0 in the Control A registers).

8.4 Excessive Zeros Detection

During Host mode operation if CODER = 1 and EXZ = 1 in the Control A register, the BPV output pin is OR'ed with receive excessive zero events. In AMI mode when AMI-Rx = 1, the BPV pin is set high for one bit period when 16 or more consecutive zeros are received. In B8ZS mode when AMI-Rx = 0, the BPV pin is set high for one bit period when 8 or more consecutive zeros are received. This is in accordance with the ANSI T1.231 specification. For E1 operation with HDB3 disabled, the excessive zeros detection is also disabled. For E1 with HDB3 enabled the BPV pin goes high for every set of 4 consecutively received zeros.

8.5 Loss of Signal

During Hardware mode and Host mode operation, the loss of signal (LOS) condition is detected by the receiver and reported when the LOS pin is set high. Loss of signal is indicated when 175 ±15 consecutive zeros are received, or when the receive (RTIP/RRING) signal level drops below the receiver sensitivity of the device. The LOS condition is exited according to the ANSI T1.231-1993 criteria that requires a minimum 12.5% ones density signal over 175 ±75 bit periods with no more than 100 consecutive zeros. During LOS, recovered data is squelched and zeroes are output on RPOS/RNEG (RDATA).

During Host mode operation, LOS is reported using the LOS and Latched-LOS bits in the Status registers. Note that both the LOS pin and register indications are available in Host mode operation. The LOS pin and/or bit is set high when the device is reset, in power-up, or a channel is powered-down and returns low when data is recovered by the receiver.

During LOS condition the RPOS (RDATA), RNEG pins are forced low, except when LLOOP1 (digital loopback) is enabled, or when the AAO (Automatic All Ones) bit is set in the channel 1 mask register. Setting the AAO bit high forces unframed all ones pattern out on the RPOS (RDATA), RNEG pins when LOS condition occurs.

When the jitter attenuator is in the receive path and LOS occurs, the frequency of the last valid recovered signal is held at RCLK. When the jitter attenuator is not in the receive path, the output frequency becomes the frequency of the reference clock.

8.6 Transmit All Ones

During Hardware mode operation, transmit all ones (TAOS) is selected by setting the TAOS pin high. During Host mode, TAOS is controlled using the TAOS bit in the Control B registers.

Selecting TAOS causes continuous ones to be transmitted to the line on TTIP and TRING at the frequency of REFCLK. In this mode, the transmit data inputs TPOS and TNEG (or TDATA) are ignored. A TAOS request overrides the data transmitted to the line interface during local and remote loopbacks. Note that the CLKLOST interrupt is not available for TCLK in the TAOS mode.

8.7 Receive All Ones

During Host mode operation, the data at RPOS and RNEG (or RDATA) may be forced to output an unframed all-ones pattern by setting both the LLOOP1 and LLOOP2 bits in the Control B register to "1". An automatic Receive All Ones (AAO)

response to a Loss of Signal condition for either channel is activated by setting bit 1 of the channel 1 Mask register to 1.

8.8 Local Loopback

Selecting LLOOP causes the TCLK, TPOS, and TNEG (or TDATA) inputs to be looped back through the jitter attenuator (if enabled) to the RCLK, RPOS, and RNEG (or RDATA) outputs. The receive line interface is ignored, but data at TPOS and TNEG (or TDATA) continues to be transmitted to the line interface at TTIP and TRING. During Hardware mode operation, simultaneous local loopback 2 of both channels is selected by setting the LLOOP pin high. During Host mode operation, local loopback 1 on a per channel basis is controlled using the LLOOP1 bit in the Control B registers.

During Hardware mode operation, a per channel local loopback 1 is performed when both the RLOOP and TAOS pins are high. The data at TPOS and TNEG is overridden with an all-ones pattern (TAOS) and the receive input at RTIP and RRING is ignored.

During Host mode operation, local loopback 2 can also be selected using the LLOOP2 bit in the Control B registers. Selecting LLOOP2 causes the TCLK, TPOS, and TNEG (or TDATA) inputs to be looped back to the RCLK, RPOS, and RNEG (or RDATA) outputs. The line driver, line receiver, and jitter attenuator (if enabled) are also included. The receive line interface is ignored, but data at TPOS and TNEG (or TDATA) continues to be transmitted to the line interface at TTIP and TRING.

A TAOS request overrides the data transmitted to the line interface during both local loopbacks. A TAOS request also overrides the data received at RPOS and RNEG (or RDATA) during local loopback 2. Note that simultaneous selection of local and remote loopback modes is not valid.

8.9 Remote Loopback

During Hardware mode operation, remote loopbacks of either channel is selected by setting the RLOOP pin high. During Host mode operation, remote loopback of each channel is controlled using the RLOOP bit in the Control B registers.

Selecting RLOOP causes the data received from the line interface at RTIP and RRING to be looped back through the jitter attenuator (if enabled) and retransmitted on TTIP and TRING. Data input to TPOS and TNEG (or TDATA) is ignored, but data recovered from RTIP and RRING continues to be output on RPOS and RNEG (or RDATA).

Remote loopback is functional if TCLK is absent. A TAOS request overrides the data transmitted to the line interface during a remote loopback. Note that simultaneous selection of local and remote loopback modes is not valid.

8.10 Driver Tristate

The drivers may be independently tristated in all modes of operation. During Hardware mode operation, setting the CON[3:0] pins of a channel to "111X" will tristate the driver. During Host mode serial port operation, the ZTX1 and ZTX2 pins perform the driver tristate function and setting the CON[3:0] bits in the Control B registers to "111X" will also tristate the driver. During Host mode parallel port operation, setting the CON[3:0] bits in the Control B register to "111X" tristates the driver. In host mode, the CS61584A powers up with CON[3:0] set to 1110, which tristates the transmitter.

8.11 Power Down

During Hardware mode operation, channel power down is selected by setting the PD1 or PD2 pin high. During Host mode operation, channel power down is controlled using the PD bit in the Control A registers. Power down places the transmitter, receiver, and jitter attenuator in reset. The RCLK, RPOS, RNEG, RDATA, AIS, BPV, TTIP, and TRING output pins are placed in a high-impedance

state. LOS will go high, and the status register will be reset, but the Control, Mask, and Arbitrary Waveform registers remain unchanged. The channel not in power down and the processor port will still to operate normally.

Simultaneously selecting PD1 and PD2 will place all the above-mentioned pins in high impedance state and power down additional analog circuitry that is shared by both channels. The status registers are reset. In the hardware mode all output pins are tri-stated and internally pulled up to the positive supply rail. After exiting the power down state, the channel will be fully operational in less than 20 ms.

8.12 Reset Pin

The CS61584A is continuously calibrated during operation to insure the performance of the device over power supply and temperature. This continuous calibration function eliminates the need to reset the line interface during operation.

During Hardware and Host modes of operation, a device reset is selected by setting the RESET pin high for a minimum of 200 ns. The reset function initiates on the falling edge of RESET and requires less than 20 ms to complete. The control logic and register set are initialized and the transmit and receive circuitry is calibrated if REFCLK and TCLK are present. During Host mode operation, a reset event is indicated by the Latched-Reset bit in the Status register.

9. HOST MODE

Host mode allows the CS61584A to be configured and monitored using an internal register set. This option is selected when the MODE pin is set high. Using the P/$\overline{S}$ pin, serial or 8-bit parallel interface ports are available in Host mode. During serial port operation, the registers are specified by a 6-bit address in the range of 0x10 to 0x19. During parallel port operation, the registers are specified by an 8-bit address. The four most significant bits of the address selects one of 16 devices on the board, established by the SAD[7:4] pins. The four least significant bits of the address specify the register address in the range of 0x00 to 0x09 for the selected device. Parallel port option is compatible with Motorola and Intel 8-bit, multiplexed address/data bus.

9.1 Register Set

The register set available during Host mode operation is presented in Table 4.

Serial Port Address	Parallel Port Address*	Description
0x10	0xY0	Ch 1 Status
0x11	0xY1	Ch 2 Status
0x12	0xY2	Ch 1 Mask
0x13	0xY3	Ch 2 Mask
0x14	0xY4	Ch 1 Control A
0x15	0xY5	Ch 2 Control A
0x16	0xY6	Ch 1 Control B
0x17	0xY7	Ch 2 Control B
0x18	0xY8	Ch 1 Arbitrary Pulse Shape
0x19	0xY9	Ch 2 Arbitrary Pulse Shape

*Y denotes the SAD[7:4] address of the CS61584A device.

Table 4. CS61584A Register Set

9.1.1 Status Registers

The Status registers are read-only registers and are shown in Table 5. The CS61584A generates an interrupt on the $\overline{INT}$ pin any time an unmasked Status register bit changes. When BTS is low (Intel mode), the IPOL pin determines the polarity of the $\overline{INT}$ pin. When BTS is high (Motorola mode), $\overline{INT}$ polarity is active low (IPOL becomes $\overline{DTACK}$). Reading both Status register clears the interrupt and deactivates the $\overline{INT}$ pin.

LOS: Set high while the loss of signal condition is detected. Reading the Status register does not clear the LOS bit. A LOS interrupt is generated only on the falling edge of the LOS alarm condition. The Latched-LOS bit generates an interrupt on the rising edge of LOS. Refer to the timing diagram in Figure 18.

Latched-LOS: Set high on the rising edge of the loss of signal condition. Reading the Status register clears the Latched-LOS bit and deactivates the $\overline{INT}$ pin. Refer to the timing diagram in Figure 18.

AIS: Set high while the alarm indication signal is detected. Reading the Status register does not clear the AIS bit. An AIS interrupt is generated only on the falling edge of the AIS alarm condition. The Latched-AIS bit generates an interrupt on the rising edge of AIS. Refer to the timing diagram in Figure 18.

Status Register (Channel 1) Serial Port Address: 0x10; Parallel Port Address: 0xY0				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	LOS1	LOS currently detected	no LOS	1
6	Latched-LOS1	LOS event since last read	no LOS	1
5	AIS1	AIS currently detected	no AIS	0
4	Latched-AIS1	AIS event since last read	no AIS	0
3	Latched-BPV1	BPV event since last read	no BPV	0
2	Latched-Overflow1	Pulse overflow since last read	no overflow	0
1	Latched-Reset	Reset event since last read	no reset	1
0	Interrupt1	Interrupt event since last read	no interrupt	1

Status Register (Channel 2) Serial Port Address: 0x11; Parallel Port Address: 0xY1				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	LOS2	LOS currently detected	no LOS	1
6	Latched-LOS2	LOS event since last read	no LOS	1
5	AIS2	AIS currently detected	no AIS	0
4	Latched-AIS2	AIS event since last read	no AIS	0
3	Latched-BPV2	BPV event since last read	no BPV	0
2	Latched-Overflow2	Pulse overflow since last read	no overflow	0
1	Latched-CLKLOST	TCLK or REFCLK absent	TCLK and REFCLK present	0
0	Interrupt2	Interrupt event since last read	no interrupt	1

Table 5. Status Registers

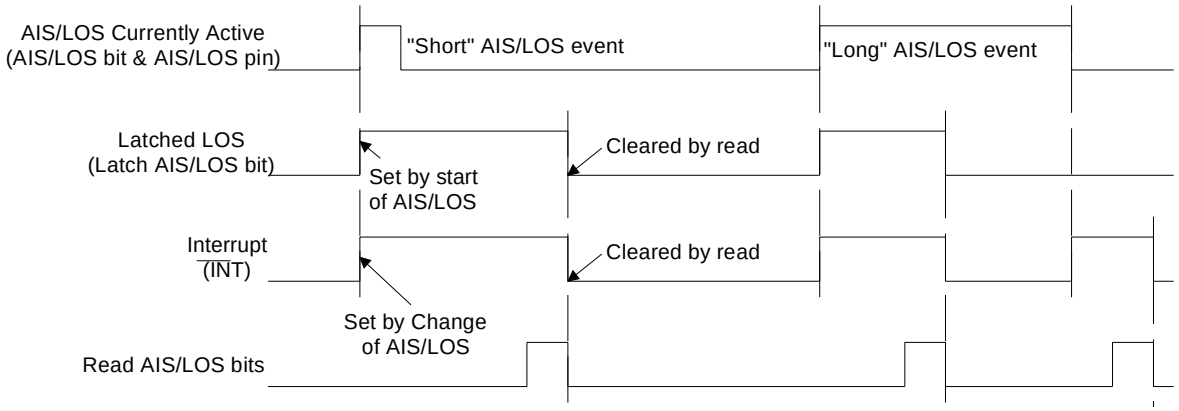


Figure 18. Alarm Indication Event Relationships

Latched-AIS: Set high on the rising edge of the alarm indication signal condition. Reading the Status register clears the Latched-AIS bit and deactivates the $\overline{INT}$ pin. Refer to the timing diagram in Figure 18.

Latched-BPV: Indicates a bipolar violation has been received since the last read of the Status register. Reading the Status register clears the Latched-BPV bit and deactivates the $\overline{INT}$ pin. This bit is set only when the line code decoder is enabled in the Control A register.

Latched-Overflow: Indicates a waveform generated using the Arbitrary Waveform register has exceeded full scale since the last read of the Status register. Reading the Status register clears the Latched-Overflow bit and deactivates the $\overline{INT}$ pin.

Latched-Reset: Indicates a reset event (power-up or RESET pin) has occurred since the last read of the Status register. Reading the Status register clears the Latched-Reset bit and deactivates the $\overline{INT}$ pin. This bit is not maskable.

Latched-CLKLOST: Set high when TCLK or REFCLK are absent. Reading the Status register clears the Latched-CLKLOST bit and deactivates the $\overline{INT}$ pin.

Interrupt: Indicates a change in the Status register since the last read. Reading the Status register clears the Interrupt bit and deactivates the $\overline{INT}$ pin.

9.1.2 Mask Registers

The Mask registers are read-write registers and are shown in Table 6. The Mask registers disables the interrupts in the corresponding Status register on a per-bit basis. Masking a Status register bit forces it to remain at zero and prevents the $\overline{INT}$ pin from activating on the condition.

Mask Register (Channel 1) Serial Port Address: 0x12; Parallel Port Address: 0xY2				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	Mask LOS1	Mask Interrupt	Enable Interrupt	0
6	Mask Latched-LOS1	Mask Interrupt	Enable Interrupt	0
5	Mask AIS1	Mask Interrupt	Enable Interrupt	0
4	Mask Latched-AIS1	Mask Interrupt	Enable Interrupt	0
3	Mask Latched-BPV1	Mask Interrupt	Enable Interrupt	0
2	Mask Latched-Overflow1	Mask Interrupt	Enable Interrupt	0
1	Automatic All Ones, AAO	Ones at RPOS/NEG on LOS	Zeros at RPOS/NEG on LOS	0
0	Mask Interrupt1	Mask Interrupt	Enable Interrupt	0

Mask Register (Channel 2) Serial Port Address: 0x13; Parallel Port Address: 0xY3				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	Mask LOS2	Mask Interrupt	Enable Interrupt	0
6	Mask Latched-LOS2	Mask Interrupt	Enable Interrupt	0
5	Mask AIS2	Mask Interrupt	Enable Interrupt	0
4	Mask Latched-AIS2	Mask Interrupt	Enable Interrupt	0
3	Mask Latched-BPV2	Mask Interrupt	Enable Interrupt	0
2	Mask Latched-Overflow2	Mask Interrupt	Enable Interrupt	0
1	Mask Latched-CLKLOST	Mask Interrupt	Enable Interrupt	0
0	Mask Interrupt2	Mask Interrupt	Enable Interrupt	0

Table 6. Mask Registers

AAO: The Automatic All-Ones (AAO) bit in the Mask Register (Channel 1, bit 1) causes an unframed all-ones pattern to be output at the RPOS and RNEG (or RDATA) pins when the receiver is in a loss of signal (LOS) condition.

9.1.3 Control A Registers

The Control A registers are read-write registers and are shown in Table 7. The Control A registers select device configuration and power down control.

CLKE: Establishes the edge of the of RCLK that RPOS and RNEG (or RDATA) are valid.

PD: Controls per channel power down.

ATTEN0 and ATTEN1: Controls the jitter attenuator location and -3 dB knee frequency (See Jitter Attenuator section).

CODER: Controls the coder mode function. The TPOS, TNEG, RPOS, and RNEG pins are active when the transparent mode is enabled. The TDATA, RDATA, AIS, and BPV pins are active when the coder mode is enabled.

AMI-T: Controls the line encoder in the transmit direction. The selection of B8ZS or HDB3 is determined by the CON[3:0] bits (See the Transmitter section).

AMI-R: Controls the line decoder in the receive direction. The selection of B8ZS or HDB3 is determined by the CON[3:0] bits (See the Transmitter section).

EXZ: Controls the automatic detection of excessive zeros on the BPV pin according to ANSI T1.231 when coder mode is enabled (CODERx = 1).

Control A Register (Channel 1) Serial Port Address: 0x14; Parallel Port Address: 0xY4				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	CLKE	RPOS/RNEG (or RDATA) valid on falling edge of RCLK	RPOS/RNEG (or RDATA) valid on rising edge of RCLK	0
6	PD1	Power down channel	Power up channel	0
5	ATTEN01	Jitter attenuator location (See Jitter Attenuator section)		0
4	ATTEN11			0
3	CODER1	Coder mode enabled	Transparent mode enabled	0
2	AMI-T1	AMI encoder enabled	B8ZS/HDB3 encoder enabled	0
1	AMI-R1	AMI decoder enabled	B8ZS/HDB3 decoder enabled	0
0	Factory Test	Test	Normal operation	0

Control A Register (Channel 2) Serial Port Address: 0x15; Parallel Port Address: 0xY5				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	EXZ	Excessive zeros detection for both channels enabled	Excessive zeros detection for both channels disabled	0
6	PD2	Power down channel	Power up channel	0
5	ATTEN02	Jitter attenuator location (See Jitter Attenuator section)		0
4	ATTEN12			0
3	CODER2	Coder mode enabled	Transparent mode enabled	0
2	AMI-T2	AMI encoder enabled	B8ZS/HDB3 encoder enabled	0
1	AMI-R2	AMI decoder enabled	B8ZS/HDB3 decoder enabled	0
0	Factory Test	Test	Normal operation	0

Table 7. Control A Registers

Factory Test: Must be cleared for normal device operation.

9.1.4 Control B Registers

The Control B registers are read-write registers and are shown in Table 8. The Control B registers select device configuration and loopback control.

TAOS: Controls the transmission of all ones to the line interface. A TAOS request overrides the data transmitted to the line interface during local and remote loopbacks.

RLOOP: Controls the remote loopback function for the channel.

LLOOP1: Controls the local loopback #1 function for the channel. Includes the jitter attenuator, if enabled. In host mode, selecting LLOOP1 and LLOOP2 simultaneously causes all ones to be output from RPOS/RNEG (RDATA).

LLOOP2: Controls the local loopback #2 function for the channel. Includes the line driver, line receiver, and jitter attenuator, if enabled. See LLOOP1, above, for receive all ones function.

CON[3:0]: Controls the configuration of the line driver, line receiver, coder, and driver tristate as shown in the Transmitter section. Both channels must be configured to operate at the same rate (both T1 or both E1).

9.1.5 Arbitrary Waveform Registers

In addition to the predefined T1 and E1 pulse shapes, arbitrary pulse shapes may be created during Host mode operation using the registers shown in Table 9. This flexibility can be used to compen-

Control B Register (Channel 1) Serial Port Address: 0x16; Parallel Port Address: 0xY6				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	TAOS1	Enable transmit all ones	Disable transmit all ones	0
6	RLOOP1	Enable remote loopback	Disable remote loopback	0
5	LLOOP11	Enable local loopback #1	Disable local loopback #1	0
4	LLOOP21	Enable local loopback #2	Disable local loopback #2	0
3	CON31	Line configuration selections (See Transmitter section)		1
2	CON21			1
1	CON11			1
0	CON01			0

Control B Register (Channel 2) Serial Port Address: 0x17; Parallel Port Address: 0xY7				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	TAOS2	Enable transmit all ones	Disable transmit all ones	0
6	RLOOP2	Enable remote loopback	Disable remote loopback	0
5	LLOOP12	Enable local loopback #1	Disable local loopback #1	0
4	LLOOP22	Enable local loopback #2	Disable local loopback #2	0
3	CON32	Line configuration selections (See Transmitter section)		1
2	CON22			1
1	CON12			1
0	CON02			0

Table 8. Control B Registers

sate for waveform degradation that may result from non-standard cables, transformers, or protection circuitry.

Arbitrary waveform generation is enabled when the CON[3:0] line configuration selection in the Control B register is set to one of four arbitrary waveform modes (See the Transmitter section). The arbitrary pulse shape of mark (a transmitted "1") is specified by describing the pulse shape across three Unit Intervals (UIs). One UI in DS1 applications is 648 ns (1.544 MHz period) and one UI in E1 applications is 488 ns (2.048 MHz period). For example, arbitrary waveform generation allows the DSX-1 return-to-zero "tail" to extend further into the next UI or allows T1 long-haul waveforms to be defined across all three UIs. The amplitude of a space (a transmitted "0") is fixed at zero volts.

All three UIs are divided into 14 equal phases for a total of 42 phase segments. The shape of the pulse is then defined by writing the amplitude of each phase segment to the Arbitrary Waveform register 42 times in sequence from UI1/phase1 to UI3/phase14. The custom pulse shape must be defined using the Arbitrary Waveform register before setting the CON[3:0] configuration selection to one of the arbitrary generation settings (i.e., 1001, 1010, or 1011).

For DS1 applications, the CS61584A divides the 648 ns UI into 14 equal phases of 46.3 ns. For DSX-1 applications, the 648 ns UI is divided into 13 equal phases of 49.8 ns. The phase amplitude information written for phase 14 of each UI is ignored. For E1 applications, the 488 ns UI is divided into 12 equal phases of 40.7 ns. The phase ampli-

Arbitrary Waveform Register (Channel 1) Serial Port Address: 0x18; Parallel Port Address: 0xY8				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	0	Arbitrary pulse shape definitions		undefined
6	MSB			
5				
4				
3				
2				
1				
0	LSB			

Arbitrary Waveform Register (Channel 2) Serial Port Address: 0x19; Parallel Port Address: 0xY9				
Bit	**Description**	**Definition**		**Reset Value**
		1	**0**	
7	0	Arbitrary pulse shape definitions		undefined
6	MSB			
5				
4				
3				
2				
1				
0	LSB			

Table 9. Arbitrary Waveform Registers

tude information written for phases 13 and 14 of each UI is ignored. Examples of arbitrary waveforms are illustrated in Figure 19.

The amplitude of each phase segment is described by a 7-bit, 2's complement number (bit 8 is ignored). A positive value describes pulse amplitude and a negative value describes pulse undershoot. For DSX-1 applications with CON[3:0] = 1010, the typical output voltage step is 73 mV/LSB across the secondary (line side) of the transformer. For DS1 applications with CON[3:0] = 1011, the typical output voltage step is 52 mV/LSB across the transformer secondary. For E1 75 Ω coaxial applications with CON[3:0] = 1000, the typical output voltage step is 43 mV/LSB. For E1 120 Ω twisted-pair applications with CON[3:0] = 1001, the typical output voltage step is 52 mV/LSB.

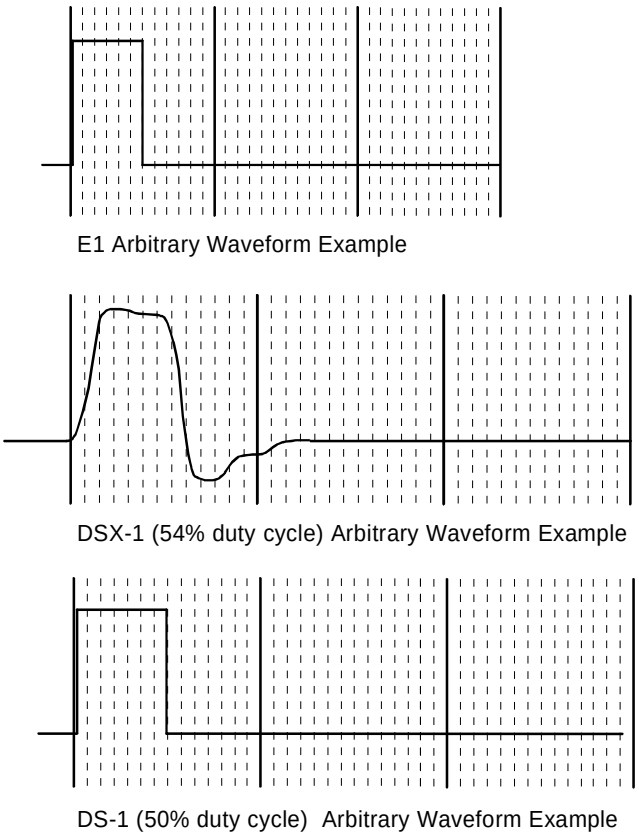


Figure 19. Phase Definition of Arbitrary Waveforms

The full scale positive value is 0x3F and the full scale negative value is 0x40. It is recommended that the output voltage across the secondary of the transformer (line interface side) be limited to 4.4 Vpk. At higher output voltages, the transmitter may not be able to drive the requested voltage based on the current operating conditions.

Because the transmitter drives either a mark or a space to the line interface every UI, the phase amplitude information defined in UI2 and UI3 is added to the symbols transmitted at TTIP and TRING in those intervals. Therefore, a mark defined only for UI1 will be output exactly as programmed if another mark is transmitted in the next two UI. However, a mark defined over UI1 and UI2 with an extended return-to-zero "tail" will cause the leading edge of a mark transmitted in the next UI to rise or fall more quickly. This is illustrated in Figure 20. If the hexadecimal sum of the phase amplitudes exceeds the full scale values, the sum is replaced by the full scale value and the Latched-Overflow bit is set in the Status register.

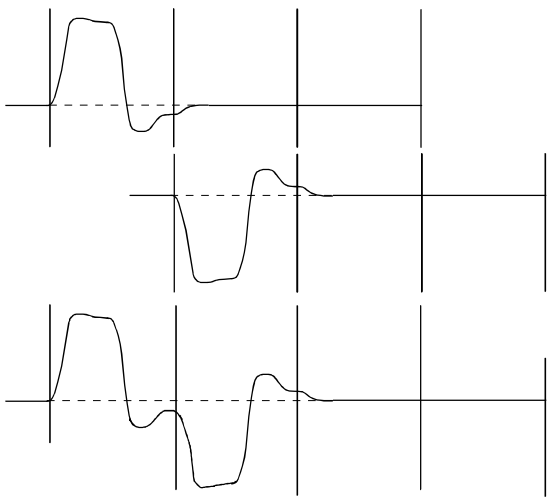


Figure 20. Example of Summing of Waveforms

9.2 Serial Port Operation

Serial port operation in Host mode is selected when the MODE pin is set high and the P/$\overline{S}$ pin is set low. In this mode, the CS61584A register set is accessed by setting the chip select ($\overline{CS}$) pin low and communicating over the SDI, SDO, and SCLK pins. Timing over the serial port is independent of the transmit and receive system timing. Figure 21 illustrates the format of serial port data transfers.

A read or write is initiated by writing an address/command byte (ACB) to SDI. During a read cycle, the register data addressed by the ACB is output on SDO on the next eight SCLK clock cycles. During a write cycle, the data byte immediately follows the ACB. A second address byte is required when reading or writing the Arbitrary Waveform registers (see below).

Data is written to and read from the serial port in LSB first format. When writing to the port, SDI input data is sampled by the device on the rising edge of SCLK. The polarity of the data output on SDO is controlled by the SPOL pin. When the SPOL pin is low, data on SDO is valid on the rising edge of SCLK. When the SPOL pin is high, data on SDO is valid on the falling edge of SCLK. The SDO pin is high impedance when not transmitting data. If the host processor has a bi-directional I/O port, SDI and SDO may be tied together.

As illustrated in Figure 22, the ACB consists of a R/$\overline{W}$ bit, address field, and two reserved bits. The R/$\overline{W}$ bit specifies if the current register access is a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$ = 0) operation. The address field specifies the register address from 0x10 to 0x19. The reserved bit must be cleared for normal operation of serial mode.

During register addressing, the first eight registers are addressed as 0x10 to 0x17 in the address field of the ACB. Because Arbitrary Waveform registers 0x18 and 0x19 access multiple bytes of RAM, reading or writing these registers requires an Address Command Byte followed by a RAM address byte for each data transfer. The ACB specifies either 0x18 or 0x19 in the address field to access the channel 1 or channel 2 Arbitrary Waveform register set. The RAM address is an 8-bit, unsigned binary number in the range of 0x00 to 0x29 to identify one of 42 RAM locations. The data byte containing the 7-bit, 2's complement number specifying the phase amplitude completes the 24 SCLK write cycle.

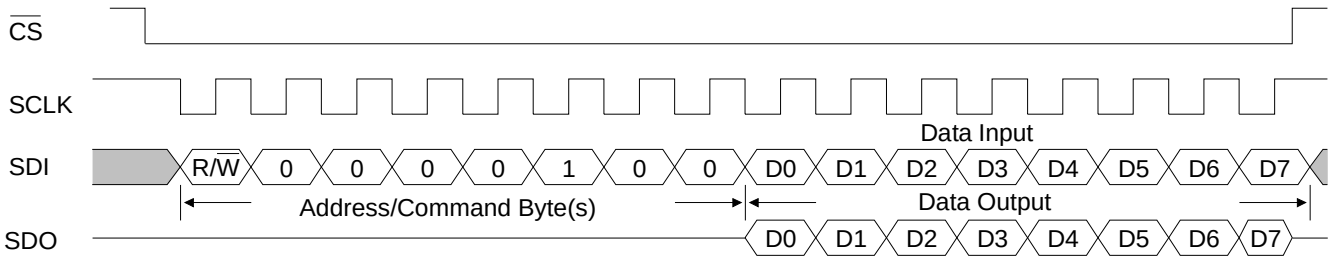


Figure 21. Serial Read/Write Format (SPOL = 0)

B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
Reserved	Reserved	ADR4	ADR3	ADR2	ADR1	ADR0	R/W
0	0	MSB	Address Field			LSB	0 = Write 1 = Read

Figure 22. Address Command byte

9.3 Parallel Port Operation

Parallel port operation in Host mode is selected when the MODE and P/$\overline{S}$ pins are set high. In this mode, the CS61584A register set is accessed using an 8-bit, multiplexed bi-directional address/data bus AD[7:0]. Timing over the serial port is independent of the transmit and receive system timing.

The device is compatible with both Intel and Motorola bus formats. The Intel bus format is selected when the BTS pin is low and the Motorola bus format is selected when the BTS pin is high. A read or write is initiated by writing an address byte to AD[7:0]. The device latches the address on the falling edge of ALE(AS). During a read cycle, the register data is output during the later portion of the $\overline{RD}$ or DS pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high in Intel timing or DS transitions low in Motorola timing. During a write cycle, valid write data must be present and held stable during the later portion of the $\overline{WR}$ or DS pulses. A second address byte is required when reading or writing the Arbitrary Waveform registers (see below).

A read or write over the parallel port is initiated by writing an address byte to AD[7:0]. The address byte consists of two nibbles. The four most significant bits AD[7:4] select one of 16 CS61584A devices in the application. This device address value is established by the SAD[7:4] pins. The four least significant bits AD[3:0] are the register address for the selected device, ranging from 0x00 to 0x09.

The first eight device registers are addressed from 0x00 to 0x07 in the four least significant bits of the address. Because Arbitrary Waveform registers 0x08 and 0x09 access multiple bytes of RAM, reading or writing these registers requires an additional RAM address byte for each data transfer. The RAM address is an 8-bit, unsigned binary number in the range of 0x00 to 0x29 to identify one of 42 RAM locations. The data byte containing the 7-bit, 2's complement number specifying the phase amplitude completes a write cycle. The sequence for writing to RAM is: first ALE(AS) addresses the device, a second ALE(AS) addresses the RAM, then a $\overline{RD}$ or $\overline{WR}$ (R/$\overline{W}$) accesses the RAM data.

10. JTAG BOUNDARY SCAN

Board testing is supported through JTAG boundary scan. Using boundary scan, the integrity of the digital paths between devices on a circuit board can be verified. This verification is supported by the ability to externally set the signals on the digital output pins of the CS61584A, and to externally read the signals present on the input pins of the CS61584A. Additionally, the manufacturer ID, part number and revision of the device can be read during board test using JTAG boundary scan.

As shown in Figure 23, the JTAG hardware consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is achieved through signals applied to the Test Mode Select (J-TMS) and Test Clock (J-TCK) input pins. Data is shifted into the registers via the Test Data Input (J-TDI) pin, and shifted out of the registers via the Test Data Output (J-TDO) pin. Both J-TDI and J-TDO are clocked at a rate determined by J-TCK. The Instruction register defines which data register is accessed in the shift operation. Note that if J-TDI is floating, an internal pull-up resistor forces the pin high.

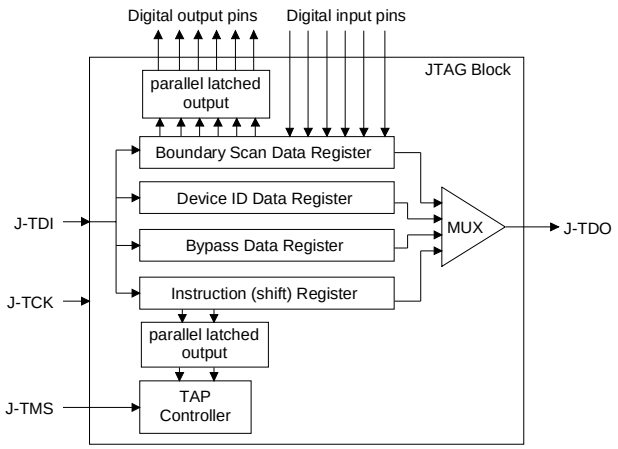


Figure 23. JTAG Circuitry Block Diagram

10.1 JTAG Data Registers (DR)

The test data registers are the Boundary-Scan Register (BSR), the Device Identification Register (DIR), and the Bypass Register (BR).

Boundary Scan Register: The BSR is connected in parallel to all the digital I/O pins, and provides the mechanism for applying/reading test patterns to/from the board traces. The BSR is 62 bits long and is initialized and read using the instruction SAMPLE/PRELOAD. The bit ordering for the BSR is the same as the top-view package pin out, beginning with the LOS1 pin and moving counter-clockwise to end with the PD1 pin as shown in Table 10. Note that the analog, oscillator, power, ground, CLKE/IPOL, and MODE pins are not included as part of the boundary-scan register.

The input pins require one bit in the BSR and only one J-TCK cycle is required to load test data for each input pin.

The output pins have two bits in the BSR to define output high, output low, or high impedance. The first bit (shifted in first) selects between an output-enabled state (bit set to 1) or high-impedance state (bit set to 0). The second bit shifted in contains the test data that may be output on the pin. Therefore, two J-TCK cycles are required to load test data for each output pin.

The bi-directional pins have three bits in the BSR to define input, output high, output low, or high impedance. The first bit shifted into the BSR configures the output driver as high-impedance (bit set to 0) or active (bit set to 1). The second bit shifted into the BSR sets the output value when the first bit is 1. The third bit captures the value of the pin. This pin may have its value set externally as an input (if the first bit is 0) or set internally as an output (if the first bit is 1). To configure a pad as an input, the J-TDI pattern is 0X0. To configure a pad as an output, the J-TDI pattern is 1X1. Therefore, three J-TCK cycles are required to load test data for each bi-directional pin.

When JTAG testing is conducted in Host mode, the polarity of the $\overline{\text{INT}}$ pin is determined by the state of the IPOL pin. The JTAG BSR should configure the $\overline{\text{INT}}$ pin as an input in Hardware mode and as an output in Host mode.

Device Identification Register: The DIR provides the manufacturer, part number, and version of the CS61584A. This information can be used to verify that the proper version or revision number has been used in the system under test. The DIR is 32 bits long and is partitioned as shown in Table 11. Data from the DIR is shifted out to J-TDO LSB first.

BSR Bits	Pin Name	Pad Type
0 - 2	LOS1, SAD6	bi-directional
3 - 5	TNEG1, AIS1	bi-directional
6	TPOS1, TDATA1	input
7	TCLK1	input
8 - 9	RNEG1, BPV1	output
10 - 11	RPOS1, RDATA1	output
12 - 13	RCLK1	output
14	ATTEN1, $\overline{\text{CS}}$	input
15 - 17	RLOOP1, $\overline{\text{INT}}$	bi-directional
18	RLOOP2, SCLK, $\overline{\text{RD}}$(DS)	input
19 - 21	LLOOP, SDO, AD0	bi-directional
22 - 24	TAOS1, SDI, AD1	bi-directional
25 - 27	TAOS2, SPOL, AD2	bi-directional
28 - 30	CON01, AD3	bi-directional
31 - 33	CON02, AD4	bi-directional
34 - 36	CON11, AD5	bi-directional
37 - 39	CON12, AD6	bi-directional
40 - 42	CON21, AD7	bi-directional
43	CON22, ALE(AS)	input
44	CON31, $\overline{\text{WR}}$(R/W)	input
45 - 46	RCLK2	output
47 - 48	RPOS2, RDATA2	output
49 - 50	RNEG2, BPV2	output
51	TCLK2	input
52	TPOS2, TDATA2	input
53 - 55	TNEG2, AIS2	bi-directional
56 - 58	LOS2, SAD7	bi-directional
59	CON32, BTS	input
60	PD2, SAD5	input
61	PD1, SAD4	input

Table 10. Boundary Scan Register

MSB 31 28	27 12	11 1	LSB 0
0 0 0 0	0 1 1 0 0 1 1 0 1 1 1 0 0 0 0 1	0 0 0 0 1 1 0 0 1 0 0	1
4 bits	16 bits	11 bits	

BIT #(s)	Function	Total Bits
31-28	Version Number	4
27-14	Part Number	14
13-12	Derivative Code	2
11-1	Manufacturer Number	11
0	Constant Logic ‘1’	1

Table 11. Device Identification Register

Bypass Register: The Bypass register consists of a single bit, and provides a serial path between J-TDI and J-TDO, bypassing the BSR. This allows bypassing specific devices during certain board-level tests. This also reduces test access times by reducing the total number of shifts required from J-TDI to J-TDO.

10.2 JTAG Instructions and Instruction Register (IR)

The instruction register (2 bits) allows the instruction to be shifted into the JTAG circuit. The instruction selects the test to be performed or the data register to be accessed or both. The valid instructions are shifted in LSB first and are listed in Table 12:

IR CODE	INSTRUCTION
00	EXTEST
01	SAMPLE/PRELOAD
10	IDCODE
11	BYPASS

Table 12.

EXTEST Instruction: The EXTEST instruction allows testing of off-chip circuitry and board-level interconnect. EXTEST connects the BSR to the J-TDI and J-TDO pins. The normal path between the CS61584A logic and I/O pins is broken. The signals on the output pins are loaded from the BSR and the signals on the input pins are loaded into the BSR.

SAMPLE/PRELOAD Instruction: The SAMPLE/PRELOAD instructions allows scanning of the boundary-scan register without interfering with the operation of the CS61584A. This instruction connects the BSR to the J-TDI and J-TDO pins. The normal path between the CS61584A logic and its I/O pins is maintained. The signals on the I/O pins are loaded into the BSR. Additionally, this instruction can be used to latch values into the digital output pins.

IDCODE Instruction: The IDCODE instruction connects the device identification register to the J-TDO pin. The IDCODE instruction is forced into the instruction register during the Test-Logic-Reset controller state.The default instruction is IDCODE after a device reset.

BYPASS Instruction: The BYPASS instruction connects the minimum length bypass register between the J-TDI and J-TDO pins and allows data to be shifted in the Shift-DR controller state.

10.3 JTAG TAP Controller

Figure 24 shows the state diagram for the TAP state machine. A description of each state follows. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure is the value present at J-TMS at each rising edge of J-TCK.

10.4 Test-Logic-Reset State

In this state, the test logic is disabled to continue normal operation of the device. During initialization, the CS61584A initializes the instruction register with the IDCODE instruction.

Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the J-TMS input is held high for at least five rising edges of J-TCK. The controller remains in this state while J-TMS is high. The CS61584A processor automatically enters this state at power-up.

10.5 Run-Test/Idle State

This is a controller state between scan operations. Once in this state, the controller remains in the state as long as J-TMS is held low. The instruction register and all test data registers retain their previous state. When J-TMS is high and a rising edge is applied to J-TCK, the controller moves to the Select-DR state.

10.6 Select-DR-Scan State

This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If J-TMS is held low and a rising edge is applied to J-TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If J-TMS is held high and a rising edge applied to J-TCK, the controller moves to the Select-IR-Scan state.

10.7 Capture-DR State

In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other test data registers, which do not have parallel input, are not changed. When the TAP controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-DR state if J-TMS is high or the Shift-DR state if J-TMS is low.

10.8 Shift-DR State

In this controller state, the test data register connected between J-TDI and J-TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of J-TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-DR state if J-TMS is high or remains in the Shift-DR state if J-TMS is low.

10.9 Exit1-DR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.

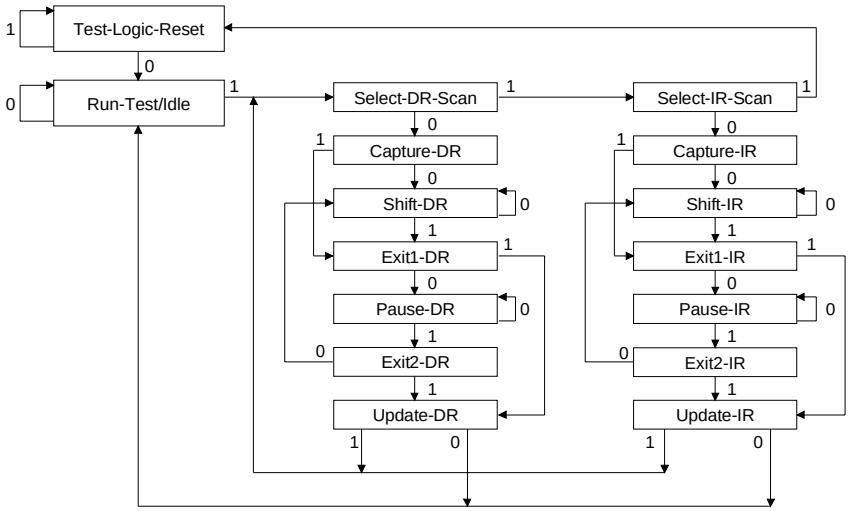


Figure 24. TAP Controller State Diagram

10.10 Pause-DR State

The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between J-TDI and J-TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as J-TMS is low. When J-TMS goes high and a rising edge is applied to J-TCK, the controller moves to the Exit2-DR state.

10.11 Exit2-DR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Shift-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.

10.12 Update-DR State

The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of J-TCK. The data held at the latched parallel output changes only in this state.

All shift-register stages in the test data register selected by the current instruction retain their previous value and the instruction does not change during this state.

10.13 Select-IR-Scan State

This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If J-TMS is held low and a rising edge is applied to J-TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If J-TMS is held high and a rising edge is applied to J-TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.

10.14 Capture-IR State

In this controller state, the shift register contained in the instruction register loads a fixed value of "01" on the rising edge of J-TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-IR state if J-TMS is held high, or the Shift-IR state if J-TMS is held low.

10.15 Shift-IR State

In this state, the shift register contained in the instruction register is connected between J-TDI and J-TDO and shifts data one stage towards its serial output on each rising edge of J-TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-IR state if J-TMS is held high, or remains in the Shift-IR state if J-TMS is held low.

10.16 Exit1-IR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.

10.17 Pause-IR State

The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as J-TMS is low. When J-TMS goes high and a rising edge is applied to J-TCK, the controller moves to the Exit2-IR state.

10.18 Exit2-IR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Shift-IR state.

The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.

10.19 Update-IR State

The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of J-TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.

10.20 JTAG Application Examples

Figures 25 and 26 illustrate examples of updating the instruction and data registers during JTAG operation.

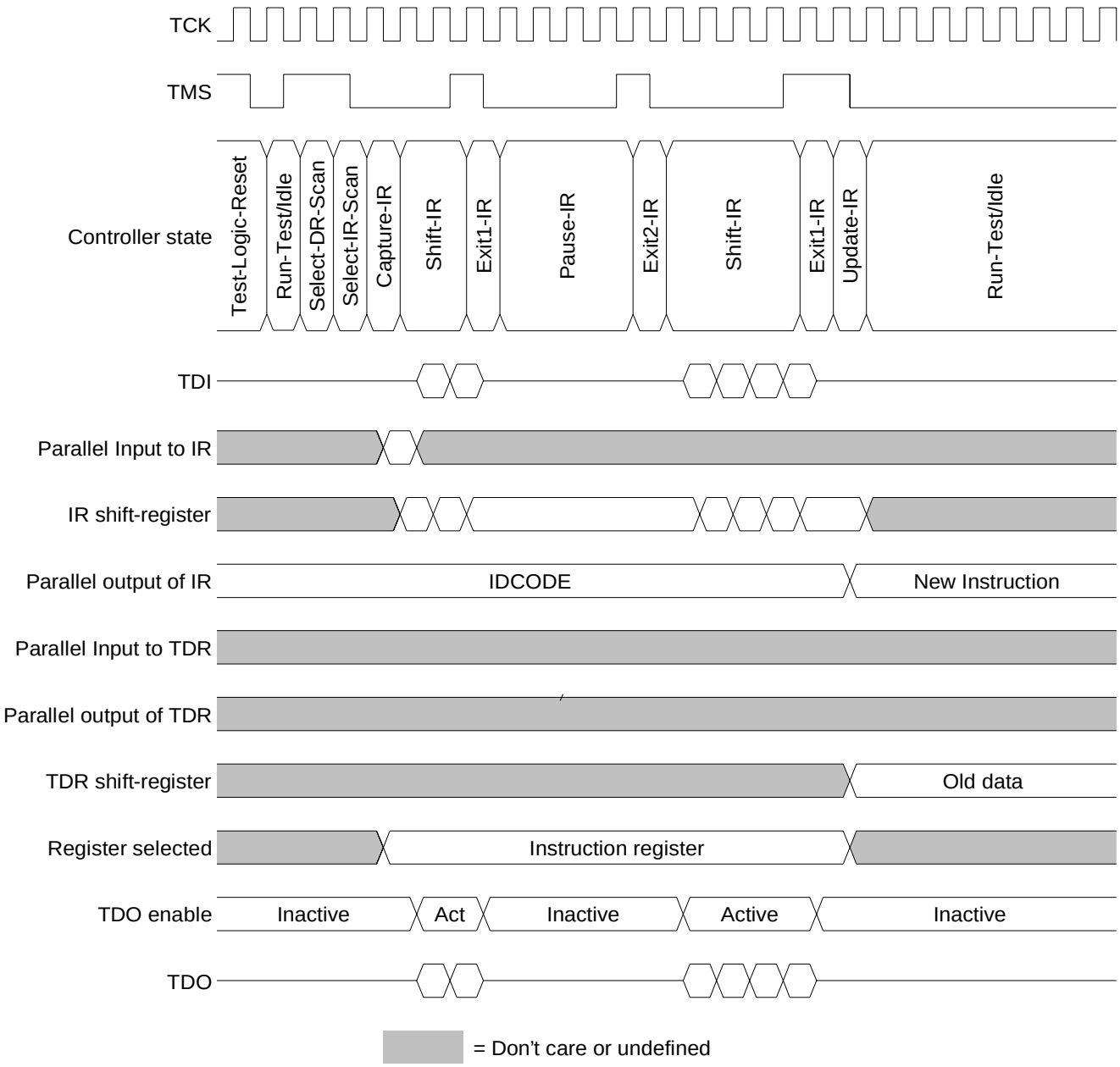


Figure 25. JTAG Instruction Register update

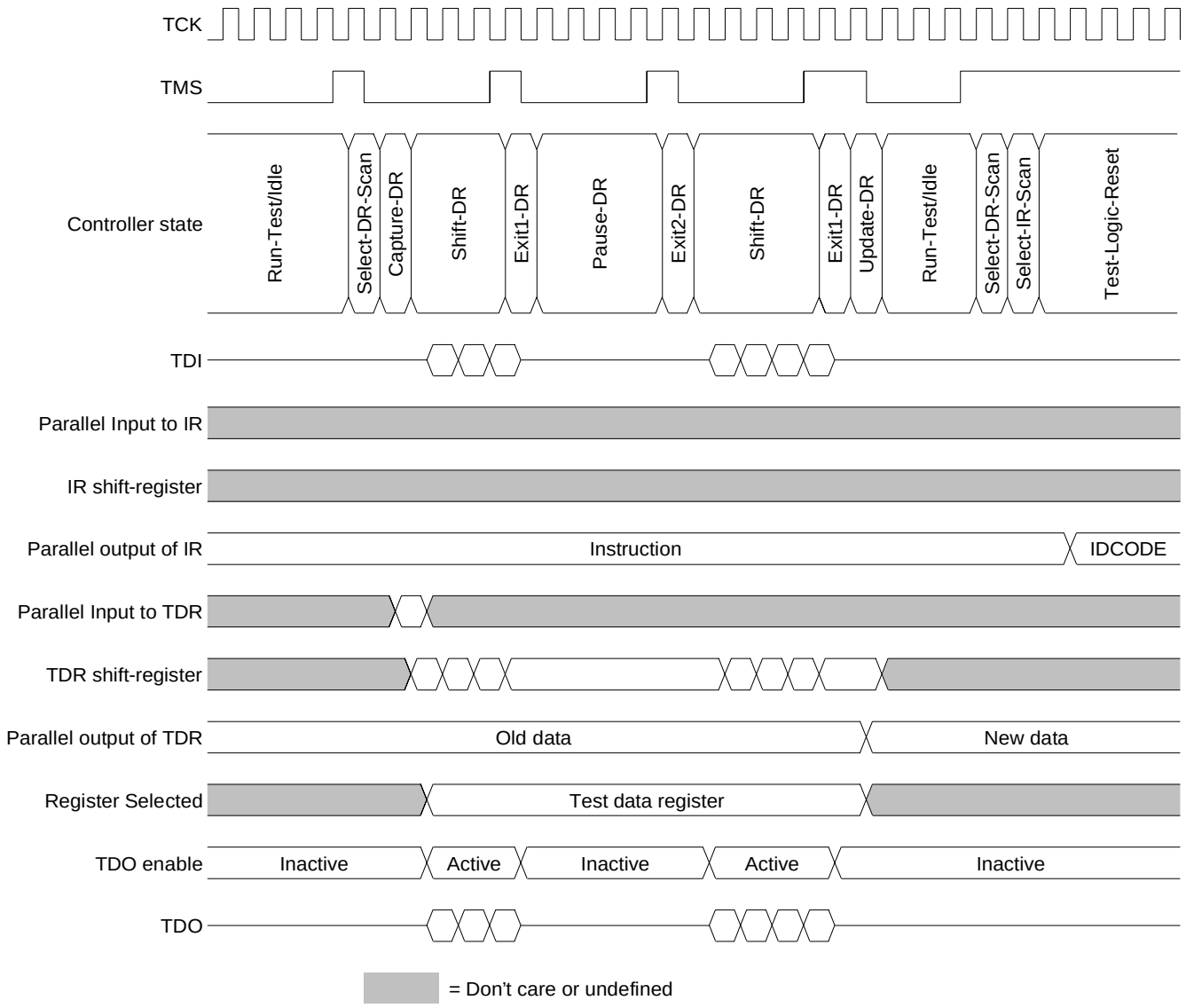
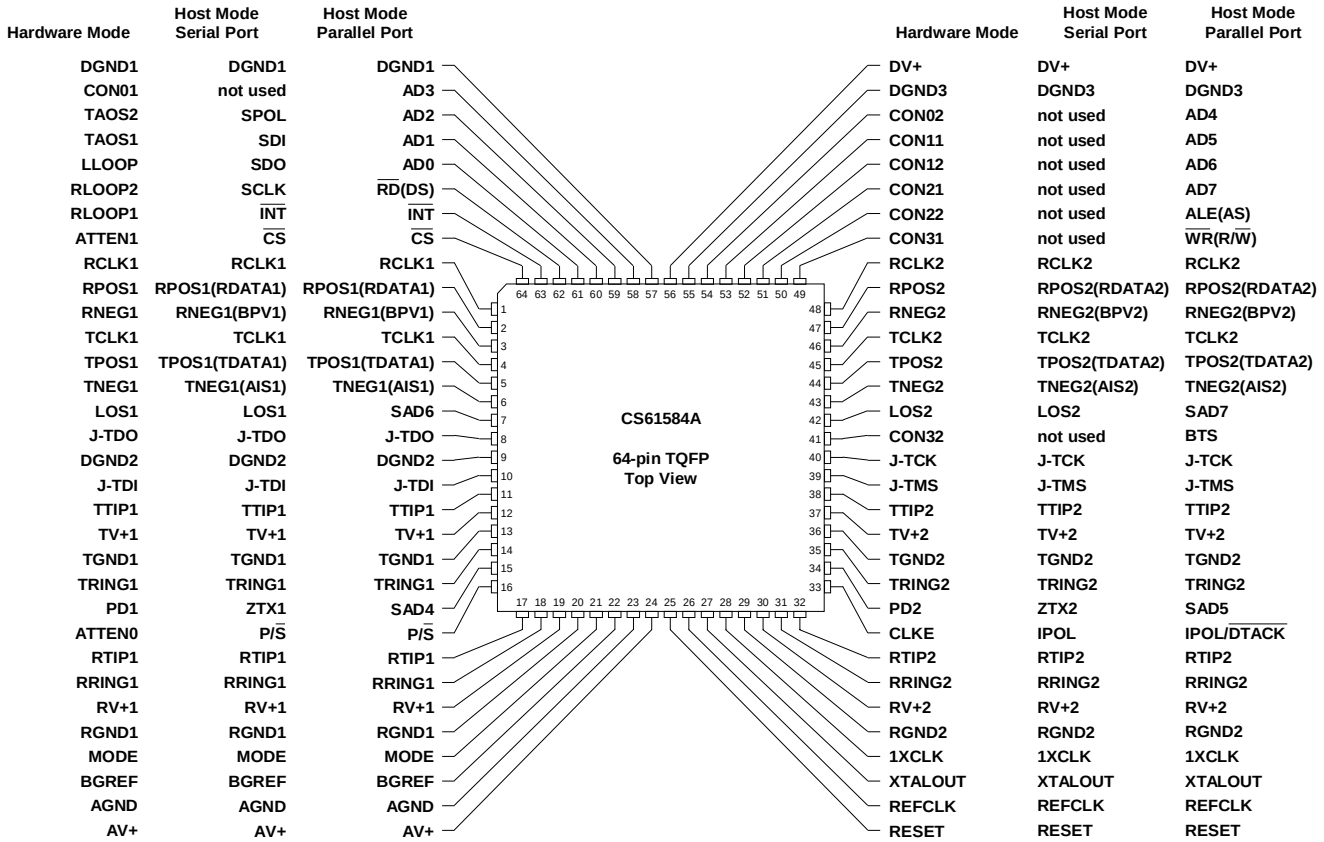


Figure 26. JTAG Data Register update

11. PIN DESCRIPTIONS



Pins labeled as “not used” should be tied to ground.

Power Supplies

AGND - Analog Ground (PLCC pin 33; TQFP pin 23)

Analog supply ground pin.

AV+ - Analog Power Supply (PLCC pin 34; TQFP pin 24)

Analog supply pin for internal bandgap reference, oscillator, and timing generation circuits.

BGREF - Bandgap Reference (PLCC pin 32; TQFP pin 22)

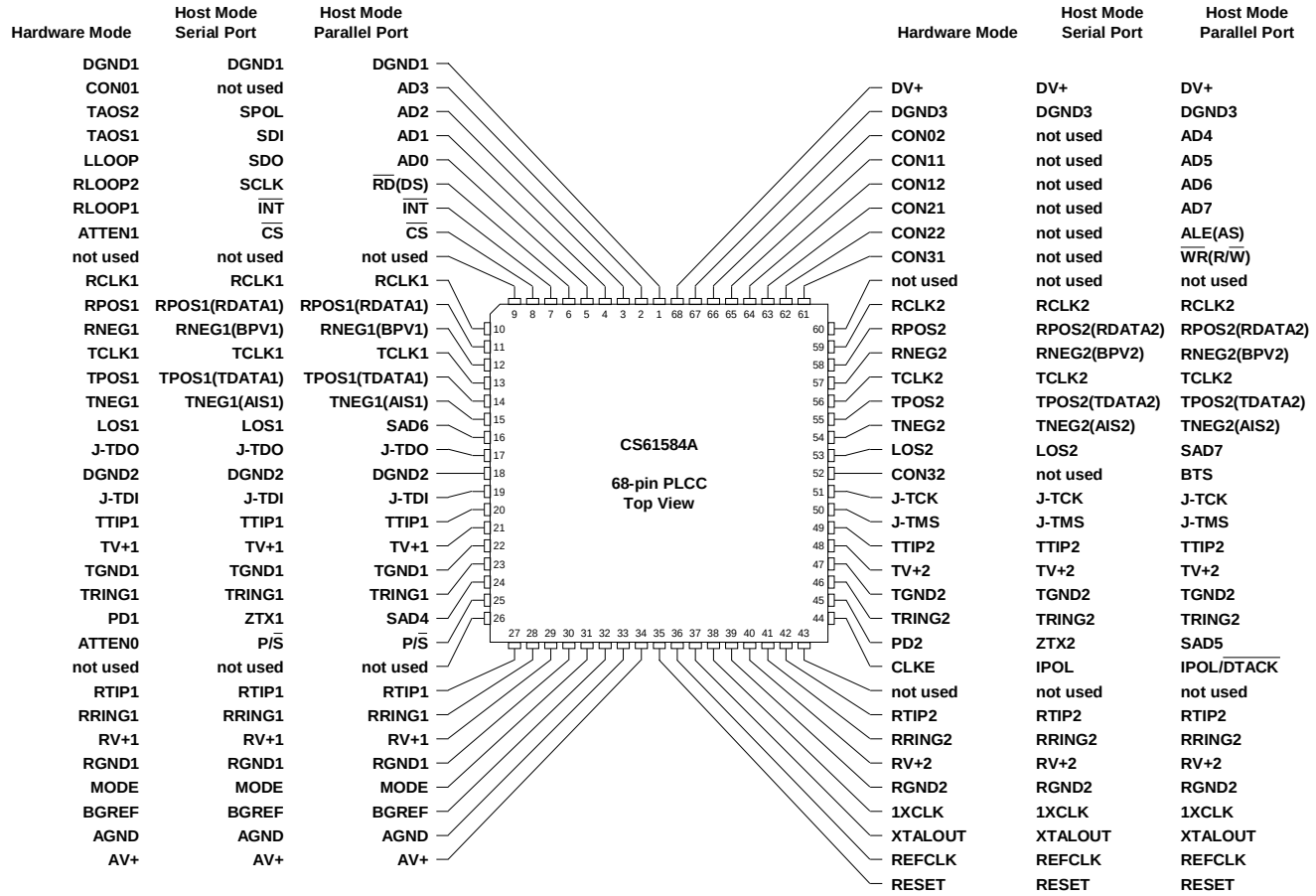
This pin is used by the internal bandgap reference and must be connected to ground by a 4.99 kΩ ±1% resistor to provide an internal current reference.

DGND1, DGND2, DGND3 - Digital Ground (PLCC pins 1, 18, 67; TQFP pins 57, 9, 55)

Power supply ground pins for the digital circuitry of both channels.

DV+ - Digital Power Supply (PLCC pin 68; TQFP pin 56)

Power supply pin for the digital circuitry of both channels.



Pins labeled as “not used” should be tied to ground.

RGND1, RGND2 - Receiver Ground (PLCC pins 30, 39; TQFP pins 20, 29)

Power supply ground pins for the receiver circuitry.

RV+1, RV+2 - Receiver Power Supply (PLCC pins 29, 40; TQFP pins 19, 30)

Power supply pins for the analog receiver circuitry.

TGND1, TGND2 - Transmit Ground (PLCC pins 22, 47; TQFP pins 13, 36)

Power supply ground pins for the transmitter circuitry.

TV+1, TV+2 - Transmit Power Supply (PLCC pins 21, 48; TQFP pins 12, 37)

Power supply pins for the analog transmitter circuitry.

T1/E1 Data Inputs and Outputs

RCLK1, RCLK2 - Receive Clock (PLCC pins 10, 59; TQFP pins 1, 48)
RPOS1, RPOS2 - Receive Positive Data (PLCC pins 11, 58; TQFP pins 2, 47)
RNEG1, RNEG2 - Receive Negative Data (PLCC pins 12, 57; TQFP pins 3, 46)

The receiver recovered clock and NRZ digital data from RTIP and RRING is output on these pins. During Hardware mode operation, the CLKE pin determines the clock edge on which RPOS and RNEG are stable and valid. During Host mode operation, the CLKE bit in the Control A register determines the clock edge on which RPOS and RNEG are stable and valid. A positive pulse (with respect to ground) received on RTIP generates a logic 1 on RPOS, and a positive pulse received on RRING generates a logic 1 on RNEG.

RDATA1, RDATA2 - Receive Data [Host mode] (PLCC pins 11, 58; TQFP pins 2, 47)

During Host mode operation with the coders enabled, the decoded digital data stream from RTIP and RRING is output on RDATA in NRZ format. The CLKE bit in the Control A register determines the clock edge on which RDATA is stable and valid.

RTIP1, RTIP2 - Receive Tip (PLCC pins 27, 42; TQFP pins 17, 32)
RRING1, RRING2 - Receive Ring (PLCC pins 28, 41; TQFP pins 18, 31)

The receive AMI signal from the line interface is input on these pins. The recovered clock and data are output on RCLK, RPOS, and RNEG (or RDATA).

TCLK1, TCLK2 - Transmit Clock (PLCC pins 13, 56; TQFP pins 4, 45)
TPOS1, TPOS2 - Transmit Positive Data (PLCC pins 14, 55; TQFP pins 5, 44)
TNEG1, TNEG2 - Transmit Negative Data (PLCC pins 15, 54; TQFP pins 6, 43)

The transmit clock and data are input to these pins. The signal is driven to the line interface at TTIP and TRING. Data on TPOS and TNEG are sampled on the falling edge of TCLK. An input on TPOS causes a positive pulse to be transmitted at TTIP and TRING, while an input on TNEG causes a negative pulse to be transmitted at TTIP and TRING.

TDATA1, TDATA2 - Transmit Data [Host mode] (PLCC pins 14, 55; TQFP pins 5, 44)

During Host mode operation with the coders enabled, the un-encoded digital data stream is input on TDATA in NRZ format. Data at TDATA is sampled on the falling edge of TCLK.

TTIP1, TTIP2 - Transmit Tip (PLCC pins 20,49; TQFP pins 11, 38)
TRING1, TRING2 - Transmit Ring (PLCC pins 23, 46; TQFP pins 14, 35)

The transmit AMI signal to the line interface is output on these pins. The transmit clock and data are input on TCLK, TPOS, and TNEG (or TDATA).

Oscillator

1XCLK - One-times Clock Frequency Select (PLCC pin 38; TQFP pin 28)

When 1XCLK is high, REFCLK must be a 1X clock (i.e., 1.544 MHz for T1 applications or 2.048 MHz for E1 applications). When 1XCLK is low, REFCLK must be an 8X clock (i.e., 12.352 MHz for T1 applications or 16.384 MHz for E1 applications).

REFCLK - External Reference Clock Input (PLCC pin 36; TQFP pin 26)

Input reference clock for the receive and jitter attenuator circuits. When 1XCLK is high, REFCLK must be a 1X clock (i.e., 1.544 MHz ±100 ppm for T1 applications or 2.048 MHz ±100 ppm for E1 applications). When 1XCLK is set low, REFCLK must be an 8X clock (i.e., 12.352 MHz ±100 ppm for T1 applications or 16.384 MHz ±100 ppm for E1 applications). The REFCLK input also determines the transmission rate when TAOS is asserted.

XTALOUT - Crystal Oscillator Output (PLCC pin 37; TQFP pin 27)

A quartz crystal with a resonant frequency of 12.352 MHz for T1 applications or 16.384 MHz for E1 applications may be connected across the XTALOUT and REFCLK pins instead of using a CMOS compatible clock source. The 1XCLK pin must be set low to select 8X clock operation. This pin must remain unconnected if a quartz crystal is not used.

Control

ATTEN0, ATTEN1 - Attenuator Select [Hardware Mode] (PLCC pins 25, 8; TQFP pins 16, 64)

Selects the jitter attenuator path and -3 dB knee point for both channels (transmit/receive/neither). See Table 3.

CLKE - Clock Edge [Hardware mode] (PLCC pin 44; TQFP pin 33)

Controls the polarity of the recovered clock RCLK. When CLKE is high, RPOS and RNEG (or RDATA) are valid on the falling edge of RCLK. When CLKE is low, RPOS and RNEG (or RDATA) are valid on the rising edge of RCLK.

CON01, CON11 - Configuration Selection for Channel 1 [Hardware Mode]
CON21, CON31 - (PLCC pins 2, 65, 63, 61; TQFP pins 58, 53, 51, 49)
CON02, CON12 - Configuration Selection for Channel 2 [Hardware Mode]
CON22, CON32 - (PLCC pins 66, 64, 62, 52; TQFP pins 54, 52, 50, 41)

These pins configure the transmitter (pulse shape, pulse width, pulse amplitude, and driver impedance), receiver (slicing level), coder (HDB3 vs B8ZS), and driver tristate. The CONx1 pins control channel 1 and the CONx2 pins control channel 2. Both channels must be configured to operate at the same data rate on the line interface (both T1 or both E1). The arbitrary waveform options are not available during Hardware mode operation. See Table 1.

LLOOP - Local Loopback [Hardware Mode] (PLCC pin 5; TQFP pin 61)

A local loopback #2 of both channels is enabled when LLOOP is high. Selecting LLOOP causes the TCLK, TPOS/TNEG (TDATA) inputs to be looped back through the transmitter, receiver and jitter attenuator (if enabled) to the RCLK, RPOS/RNEG (RDATA) outputs. The data at TPOS/TNEG (TDATA) continues to be transmitted to the line interface unless overridden by a TAOS request. The input on RTIP and RRING is ignored.

When the RLOOP and TAOS pins are both high, the TCLK, TPOS/TNEG (TDATA) inputs are looped back (local loopback #1) through the jitter attenuator (if enabled) to the RCLK, RPOS/RNEG (RDATA) outputs for the selected channel. The data at TPOS/TNEG (TDATA) is also overridden with an all-ones pattern (TAOS). The receive input at RTIP and RRING is ignored.

MODE - Mode Select (PLCC pin 31; TQFP pin 21)

Hardware mode operation is selected when MODE is low, enabling the device to be configured and monitored using control pins. Host mode operation is selected when MODE is high, enabling the device to be configured and monitored over a microprocessor interface using the internal register set.

PD1, PD2 - Power Down [Hardware mode] (PLCC pins 24, 45; TQFP pins 15, 34)

Setting PD high places the channel in a low power, inactive state. Power down forces the transmitter, receiver, and jitter attenuator to the reset state. All device outputs are forced to a high impedance state to facilitate circuit board testing.

ZTX1 - Driver Tristate [Host mode - serial port]
ZTX2 - (PLCC pins 24, 45; TQFP pins 15, 34)

Setting ZTX high causes the driver at TTIP and TRING to be placed in a tristate (high-impedance) condition.

RESET - Reset (PLCC pin 35; TQFP pin 25)

A device reset is selected by setting the RESET pin high for a minimum of 200 ns. The reset function requires less than 20 ms to complete. The control logic and register set are initialized and LOS is set high. The RESET pin should be set low for normal operation.

RLOOP1, RLOOP2 - Remote Loopback [Hardware Mode] (PLCC pins 7, 6; TQFP pin 63, 62)

A remote loopback of the channel is selected when RLOOP is high. The data received from the line interface at RTIP and RRING is looped back through the jitter attenuator (if enabled) and retransmitted on TTIP and TRING. Data recovered from RTIP and RRING continues to be output on RPOS/RNEG (RDATA). Data input on TPOS/TNEG (TDATA) is ignored.

When the RLOOP and TAOS pins are both high, local loopback #1 is invoked along with transmit all ones for the selected channel. The receive input at RTIP and RRING is ignored.

TAOS1 - Transmit All Ones Select [Hardware Mode]
TAOS2 - (PLCC pins 4, 3; TQFP pins 60, 59)

Setting TAOS high causes continuous ones to be transmitted on the line interface at the frequency determined by REFCLK.

When the RLOOP and TAOS pins are both high, local loopback #1 is invoked along with transmit all ones for the selected channel. The receive input at RTIP and RRING is ignored.

Interface

AD7, AD6, AD5, AD4 - Address/Data Bus [Host mode - parallel port]
AD3, AD2, AD1, AD0 - (PLCC pins 63-66, 2-5; TQFP pins 51-54, 58-61)

The 8-bit, multiplexed address/data bus.

ALE (AS) - Address Latch Enable (Address Strobe) [Host mode - parallel port] (PLCC pin 62; TQFP pin 50)

The address present on the address/data bus is latched on the falling edge of this signal.

BTS - Bus Type Select [Host mode - parallel port] (PLCC pin 52; TQFP pin 41)

This pin controls the function of the $\overline{RD}$(DS), ALE(AS), and $\overline{WR}$(R/$\overline{W}$) pins. Intel bus timing is selected when BTS is low. Motorola bus timing is selected when BTS is high and the pin function is listed in parenthesis "( )".

$\overline{CS}$ - Chip Select [Host mode] (PLCC pin 8; TQFP pin 64)

This pin must be low in order to access the serial or parallel port of the device.

$\overline{\text{INT}}$ - Receive Alarm Interrupt [Host mode] (PLCC pin 7; TQFP pin 63)

An interrupt is generated to flag the host processor when a Status register changes state. The interrupt is cleared by reading the Status register. The logic level for an active interrupt alarm is controlled by the IPOL pin. The $\overline{\text{INT}}$ pin is an open drain output and must be tied to the appropriate supply through a resistor.

IPOL - Interrupt Polarity [Host mode, BTS = 0] (PLCC pin 44; TQFP pin 33)

When BTS is low (Intel bus timing), the active polarity of the $\overline{\text{INT}}$ pin is controlled by IPOL. An active high interrupt is generated when IPOL is high. An active low interrupt is generated when IPOL is low. When the BTS pin is high, this pin becomes $\overline{\text{DTACK}}$ and $\overline{\text{INT}}$ is active low.

$\overline{\text{DTACK}}$ - Data Acknowledge [Host mode - parallel port, BTS = 1] (PLCC pin 44; TQFP pin 33)

When the BTS pin is high (Motorola bus timing), a low pulse on $\overline{\text{DTACK}}$ indicates when the CS61584A has latched the data during a microprocessor write cycle or when the CS61584A has output data to the bus during a microprocessor read cycle. The polarity of the $\overline{\text{INT}}$ pin is fixed to active low when the BTS pin is high (Motorola bus timing).

P/$\overline{\text{S}}$ - Parallel/Serial Port Selection [Host modes] (PLCC pin 25; TQFP pin 16)

Selects the method of communication to the internal register set during Host mode operation. Serial port communication over the SDI, SDO, and SCK pins is selected when P/$\overline{\text{S}}$ is low. Parallel port communication over an 8-bit, multiplexed address/data bus is selected when P/$\overline{\text{S}}$ is high.

$\overline{\text{RD}}$(DS) - Read Input (Data Strobe) [Host mode - parallel port] (PLCC pin 6; TQFP pin 62)

When the BTS pin is low (Intel bus timing), a low pulse on $\overline{\text{RD}}$ selects a read operation when the $\overline{\text{CS}}$ pin is low. When the BTS pin is high (Motorola bus timing), a high pulse on DS performs a read/write operation when the $\overline{\text{CS}}$ pin is low.

SAD4, SAD5 - Set Chip Address [Host mode - parallel port]
SAD6, SAD7 - (PLCC pins 24, 45, 16, 53; TQFP pins 15, 34, 7, 42)

These pins are hard-wired to establish one of 16 possible device addresses to permit a shared parallel bus system architecture. The value is compared with the upper nibble of the address byte AD[7:4] as part of the address decode procedure.

SCLK - Serial Clock [Host mode - serial port] (PLCC pin 6; TQFP pin 62)

Serial clock used to access the register set. A high or low level can be present on SCLK when the device is selected using the $\overline{\text{CS}}$ pin.

SDI - Serial Data Input [Host mode - serial port] (PLCC pin 4; TQFP pin 60)

Serial data input to the register set. Sampled by the device on the rising edge of SCLK.

SDO - Serial Data Output [Host mode - serial port] (PLCC pin 5; TQFP pin 61)

Serial data output from the register set. If SPOL is low, SDO is valid on the rising edge of SCLK. If SPOL is high, SDO is valid on the falling edge of SCLK. The SDO pin goes to a high-impedance state while the serial port is being written or after bit D7 is output on SDO during a read.

SPOL - SDO Polarity Control [Host mode - serial port] (PLCC pin 3; TQFP pin 59)

Controls the polarity of the serial data output SDO. If SPOL is low, SDO is valid on the rising edge of SCLK. If SPOL is high, SDO is valid on the falling edge of SCLK.

$\overline{\text{WR}}$(R/$\overline{\text{W}}$) - Write Input (Read/Write) [Host mode - parallel port] (PLCC pin 61; TQFP pin 49)

When the BTS pin is low (Intel bus timing), a low pulse on $\overline{\text{WR}}$ selects a write operation when the $\overline{\text{CS}}$ pin is low. When the BTS pin is high (Motorola bus timing), a high pulse on R/$\overline{\text{W}}$ selects a read operation and a low pulse on R/$\overline{\text{W}}$ selects a write operation when the $\overline{\text{CS}}$ pin is low.

Status

AIS1, AIS2 - Alarm Indication Signal [Host mode] (PLCC pins 15, 54; TQFP pins 6, 43)

The AIS indication goes high when the receiver detects 99.9% ones density in a 5.3 ms period (< 9 zeros in 8192 bits). The AIS indication returns low when the receiver detects ≥ 9 zeros in 8192 bits.

BPV1, BPV2 - Bipolar Violation [Host mode] (PLCC pins 12, 57; TQFP pins 3, 46)

The BPV indication goes high for one RCLK bit period when a bipolar violation is detected in the received signal. Bipolar violations caused by B8ZS (or HDB3) zero substitutions are not flagged by the BPV pin if the coder mode is enabled.

The BPV pin also goes high for one RCLK bit period on excessive zero events if EXZ = 1 (Control A register, channel 2). In AMI mode, the BPV pin goes high when 16 or more zeros are received. In B8ZS mode, the BPV pin goes high when 8 or more zeros are received. This functionality is disabled when the device is configured for E1 operation.

LOS1 - Loss of Signal [Hardware mode and Host mode - serial port]
LOS2 - (PLCC pins 16, 53; TQFP pins 7, 42)

The LOS indication goes high when 175 ±15 consecutive zeros are received on the line interface, or when the receive (RTIP/RRING) signal level drop below the receiver sensitivity of the device. The LOS indication returns low when a minimum 12.5% ones density signal over 175 ±75 bit periods with no more than 100 consecutive zeros is received.

Test

J-TCK - JTAG Test Clock (PLCC pin 51; TQFP pin 40)

Data on pins J-TDI and J-TDO is valid on the rising edge of J-TCK. When J-TCK is stopped low, all JTAG registers remain unchanged.

J-TMS - JTAG Test Mode Select (PLCC pin 50; TQFP pin 39)

An active high signal on J-TMS enables the JTAG serial port. This pin has an internal pull-up resistor and may be unconnected to float high or tied low while the JTAG interface is not active.

J-TDI - JTAG Test Data In (PLCC pin 19; TQFP pin 10)

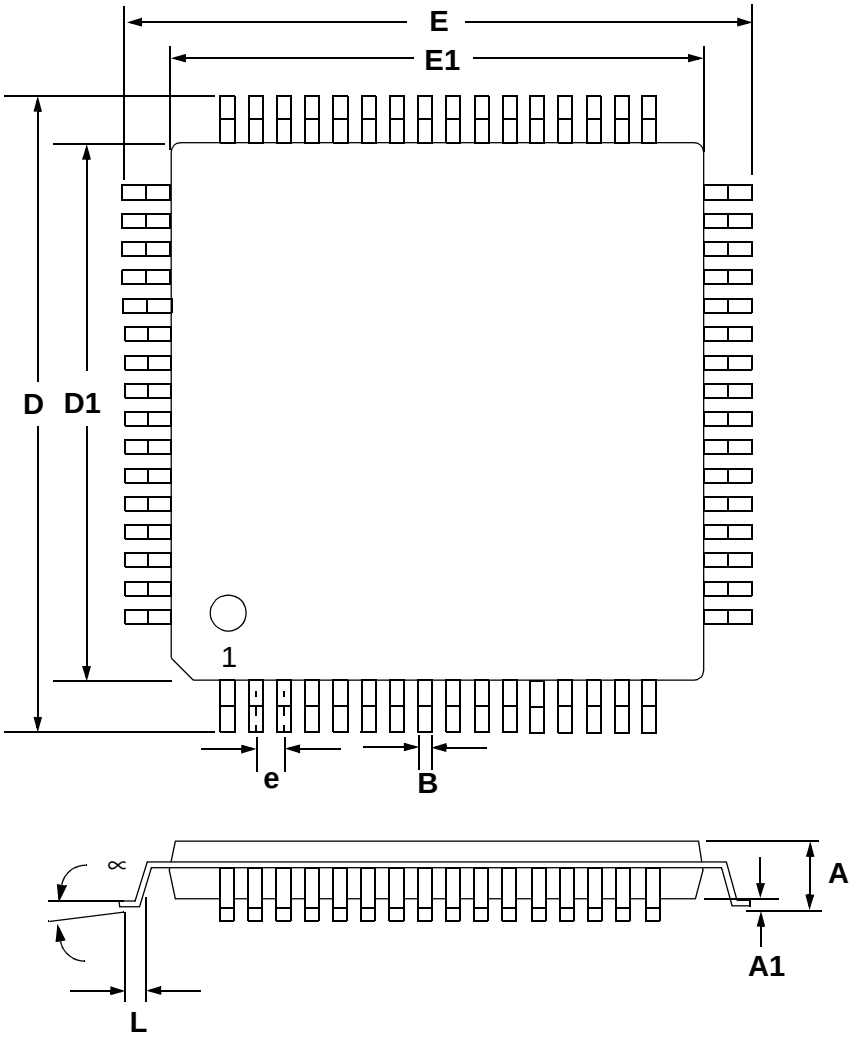
JTAG data is shifted into the device on this pin. This pin has an internal pull-up resistor. Data must be stable on the rising edge of J-TCK.

J-TDO - JTAG Test Data Out (PLCC pin 17; TQFP pin 8)

JTAG data is shifted out of the device on this pin. This pin is active only when JTAG testing is in progress. J-TDO will be updated on the falling edge of J-TCK.

12. PACKAGE DIMENSIONS

64L LQFP PACKAGE DRAWING

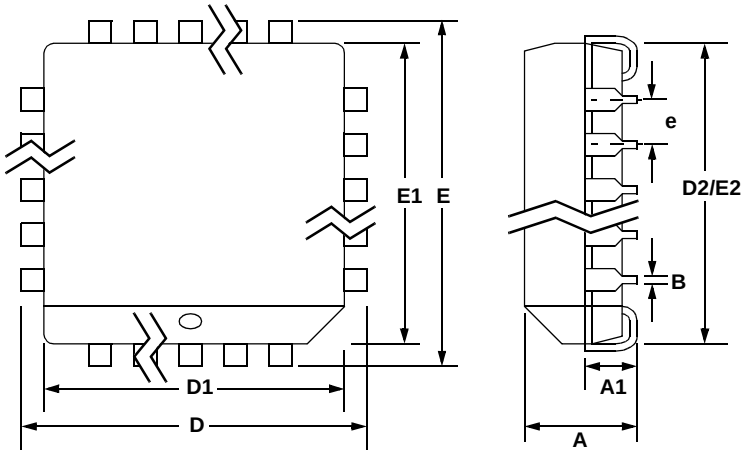


	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.55	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.008	0.011	0.17	0.20	0.27
D	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
D1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
E	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
E1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
e*	0.016	0.020 BSC	0.024	0.40	0.50 BSC	0.60
L	0.018	0.024	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS022

68L PLCC PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.165	0.1825	0.200	4.191	4.6355	5.08
A1	0.090	0.105	0.130	2.286	2.667	3.302
B	0.013	0.017	0.021	0.3302	0.4318	0.533
D	0.985	0.990	0.995	25.019	25.146	25.273
D1	0.950	0.953	0.958	24.13	24.206	24.333
D2	0.890	0.910	0.930	22.606	23.114	23.622
E	0.985	0.990	0.995	25.019	25.146	25.273
E1	0.950	0.953	0.958	24.13	24.206	24.333
E2	0.890	0.910	0.930	22.606	23.114	23.622
e	0.040	0.050	0.060	1.016	1.270	1.524

JEDEC #: MS-047

13. APPLICATIONS

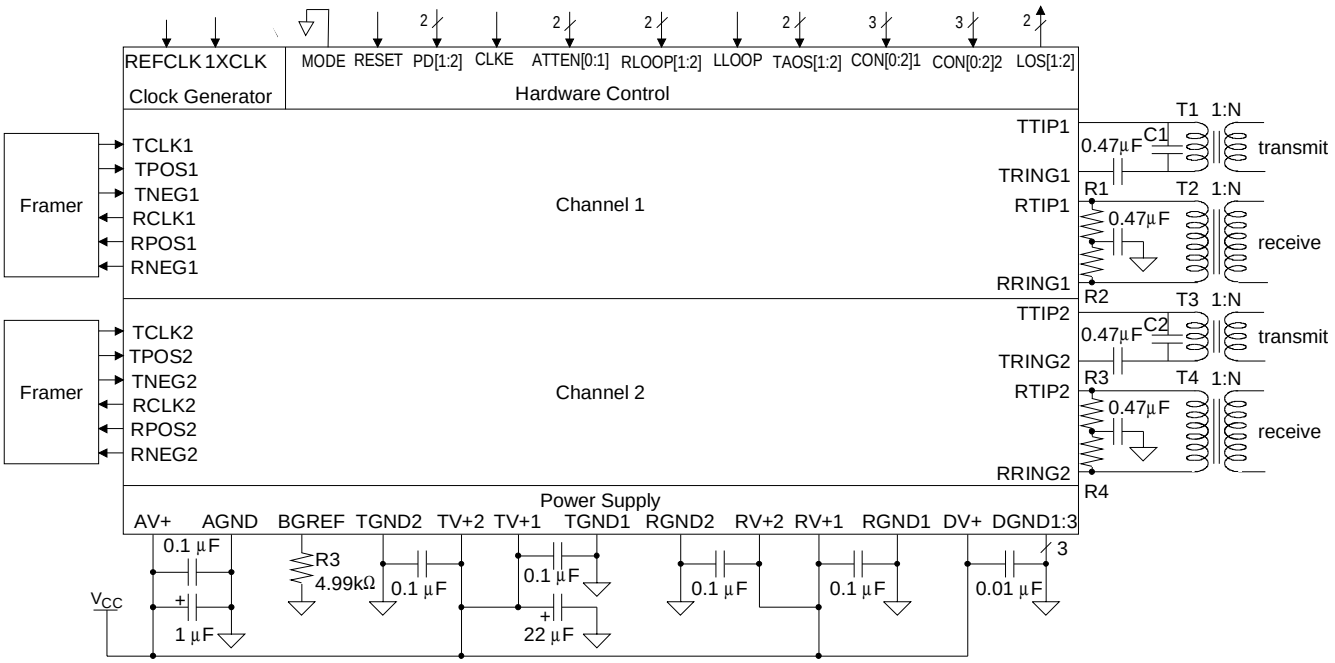


Figure 27. Hardware Mode Configuration

Device Suffix	Data Rate (MHz)	REFCLK Frequency (MHz)		Transformer Turns Ratio	Cable (Ω)	R1-R4 (Ω)	C1-C2 (pF)
		1XCLK = 1	1XCLK = 0				
-IL3 and -IQ3 (3.3 Volts)	1.544	1.544	12.352	1:2	100	12.4	560
	2.048	2.048	16.384		75	9.31	2200
					120	15.0	560
-IL5 and -IQ5 (5.0 Volts)	1.544	1.544	12.352	1:1.15	100	38.3	220
	2.048	2.048	16.384		75	28.7	470
					120	45.3	220

Table 13. CS61584A External Components

13.1 Line Interface

Figures 27-29 illustrate typical connection diagram for T1 and E1 line interface circuits in Hardware, Host serial port, and Host parallel port modes. Table 13 lists the external components that are required in T1 and E1 applications for both the 5.0 and 3.3 Volt devices.

In the transmit line interface circuitry, capacitors C1 and C2 provide transmitter return loss. The 0.47 µF capacitor in series with the transformer primary prevents output stage imbalances from producing a DC current through the transformer that might saturate the transformer and result in an output level offset.

In the receive line interface circuitry, resistors R1-R4 provide receive impedance matching and receiver return loss. The 0.47 µF capacitor to ground provides the necessary differential input voltage reference for the receiver.

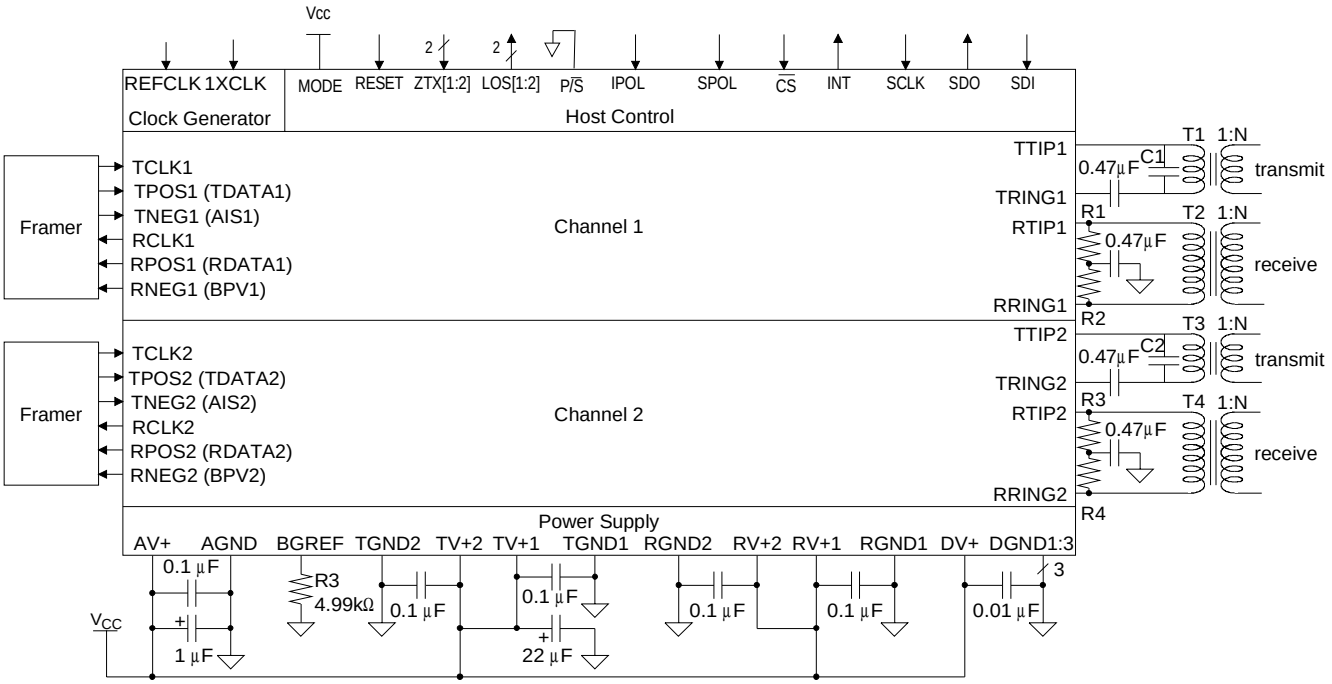


Figure 28. Host Mode Serial Port Configuration

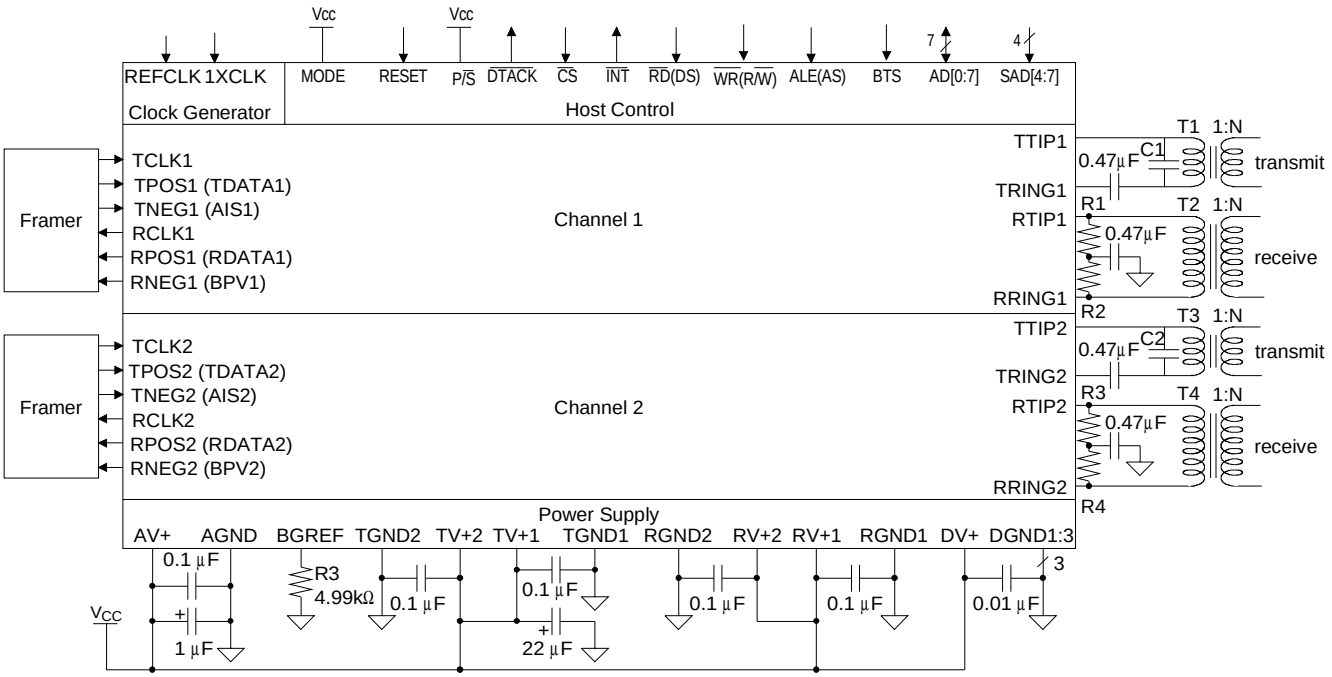


Figure 29. Host Mode Parallel Port Configuration

13.2 Power Supply

As shown in Figure 27, the CS61584A operates from a 3.3 Volt or 5.0 Volt supply. Separate power and ground pins provide internal isolation. The best way to configure the power supplies is to connect all of the supply pins together at the device. The various ground pins must not be more negative than AGND. A 4.99 kΩ ±1% resistor must be connected from BGREF to ground to provide an internal current reference.

De-coupling and filtering of the power supplies is crucial for the proper operation of the analog circuits. A capacitor should be connected between each supply and its respective ground. For capacitors smaller than 1 µF, use mylar or ceramic capacitors and place them as close as possible to their respective power supply pins. Wire-wrap bread boarding of the line interface is not recommended because lead resistance and inductance defeat the function of the de-coupling capacitors.

13.3 Quartz Crystal Specifications

When a reference clock signal is not available, a quartz crystal operating at the 8X rate can be connected across the REFCLK and XTALOUT pins. The crystal must be AT-cut and fundamental mode. The minimum specifications are shown in Table 14. Based on these specifications, quartz crystals suggested for use with the CS61584A are shown in Table 15.

13.4 Crystal Oscillator Specifications

When a reference clock signal is not available, a CMOS crystal oscillator operating at either the 1X or 8X rate can be connected at the REFCLK pin. The oscillator must have a minimum symmetry of 40-60% and minimum stability of ±100 ppm for T1 and E1 applications. Based on these specifications, crystal oscillators suggested for use with the

Parameter	Min	Typ	Max	Unit
T1 parallel resonant frequency	-	12.352	-	MHz
E1 parallel resonant frequency	-	16.384	-	MHz
Resonant frequency error (C_L = 20 pF)	-50	-	+50	ppm
Temperature drift (over system limits)	-100	-	+100	ppm
Drive level	-	-	500	µW
Series resistance	-	-	50	Ω
Shunt capacitance	-	-	7	pF
Aging	-5	-	+5	ppm/yr

Table 14. Quartz Crystal Specifications

Manufacturer	Part Number	Package Type
M-tron	397-316	ATS-49 through-hole
	522-372	ATSM-49 surface mount
SaRonix	SRX5769 SRX5772	HC-49S through-hole
	SRX5770 SRX5773	49SMLB surface mount

NOTE: Frequency tolerances are ±32 ppm with a -40 to +85 °C operating temperature range.

Table 15. Suggested Quartz Crystals

Manufacturer	Part Number	Contact Number
Comclok	CT31CH	(800)333-9825
CTS	CXO-65HG-5-I	(815)786-8411
M-tron	MH26TAD	(800)762-8800
SaRonix	NTH250A	(800)227-8974

NOTE: Frequency tolerances are ±32 ppm with a -40 to +85 °C operating temperature range.

All are 8-pin DIP packages and can be tristated.

Table 16. Suggested Crystal Oscillators

13.5 Transformers

Recommended transformer specifications are shown in Table 17. Based on these specifications, the transformers recommended for use with the CS61584A are listed in Table 18.

Turns ratio (-IL3 and IQ3)	1:2 step-up transmit 1:2 step-down receive
Turns ratio (-IL5 and IQ5)	1:1.15 step-up transmit 1:1.15 step-down receive
Primary inductance	1.5 mH min at 772 kHz
Primary leakage inductance	0.3 µH max at 772 kHz with secondary shorted
Secondary leakage inductance	0.4 µH max at 772 kHz
Interwinding capacitance	18 pF max, primary to secondary
ET-constant	16 V-µs min

Table 17. Transformer Specifications

13.6 Designing for AT&T 62411

For additional information on the requirements of AT&T 62411 and the design of an appropriate system synchronizer, refer to the Crystal Semiconductor Application Notes "AT&T 62411 Design Considerations - Jitter and Synchronization" and "Jitter Testing Procedures for Compliance with AT&T 62411."

13.7 Line Protection

Secondary protection components can be added to the line interface circuitry to provide lightning surge and AC power-cross immunity. For additional information on the different electrical safety standards and specific application circuit recommendations, refer to the Crystal Semiconductor Application Note "Secondary Line Protection for T1 and E1 Line Cards."

13.8 Loop Selection Equations

The following equations indicate the different states that various inputs have to assume to invoke the various loopback functions available in the device.

$$RLOOP1 = \overline{TAOS1}.\overline{LLOOP}.RLOOP1$$

$$RLOOP2 = \overline{TAOS2}.\overline{LLOOP}.RLOOP2$$

$$LLOOP11 = LLOOP2.RLOOP2.\overline{RLOOP1} + TAOS1.RLOOP1$$

$$LLOOP12 = LLOOP2.RLOOP2.\overline{RLOOP1} + TAOS2.RLOOP2$$

$$LLOOP21 = \overline{TAOS1}.LLOOP2.(RLOOP1 + \overline{RLOOP2})$$

$$LLOOP22 = \overline{TAOS2}.LLOOP2.(RLOOP1 + \overline{RLOOP2})$$

Turns Ratio	Manufacturer	Part Number	Package Type
1:2 (-IL3 and -IQ3)	Halo	TD08-1205A	1.5 kV through-hole, single
		TG26-1205N1	2 kV surface mount, dual
	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		PE-65771	1.5 kV through-hole, single extended temperature
		PE-65835	3.0 kV through-hole, single extended temperature
		PE-65761	1.5 kV surface mount, dual
		PE-65821	1.5 kV surface mount, dual extended temperature
		PE-65861	1.5 kV surface mount, dual
		T1016	1.5 kV surface mount, quad
		T1073	1.5 kV surface mount, octal
	Schott	67129300	1.5 kV through-hole, single extended temperature
		67115090	1.5 kV through-hole, dual extended temperature
	Valor	ST5095	1.5 kV surface mount, dual
		ST5175T	1.5 kV surface mount, quad
1:1.15 (-IL5 and -IQ5)	Halo	TD38-1505A	1.5 kV through-hole, single
	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		PE-65770	1.5 kV through-hole, single extended temperature
		PE-65838	3.0 kV through-hole, single extended temperature
		PE-68674	1.5 kV surface mount, dual extended temperature
		PE-65870	1.5 kV surface mount, dual
		T1016	1.5 kV surface mount, quad
		T1072	1.5 kV surface mount, octal
	Schott	67124840	1.5 kV through-hole, single extended temperature
	Valor	ST5112	2.0 kV surface mount, dual
		ST5171T	1.5 kV surface mount, quad

Table 18. Recommended Transformers

ORDERING INFORMATION

Model	Operating Voltage	Package	Temperature
CS61584A-IL3	3.3 V	68-pin PLCC	-40 to +85 °C
CS61584A-IL5	5.0 V		
CS61584A-IQ3	3.3 V	64-pin LQFP	
CS61584A-IQ3Z (Lead Free)			
CS61584A-IQ5	5.0 V		
CS61584A-IQ5Z (Lead Free)			

ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS61584A-IL3	225 °C	3	7 Days
CS61584A-IL5			
CS61584A-IQ3	240 °C		
CS61584A-IQ3Z (Lead Free)	250 °C		
CS61584A-IQ5	240 °C		
CS61584A-IQ5Z (Lead Free)	250 °C		

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

REVISION HISTORY

Revision	Date	Changes
PP5	JAN 2001	Preliminary Release
F1	SEP 2005	Updated device ordering info. Updated legal notice. Added MSL data..

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

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