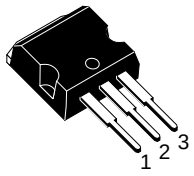
# STB12NK80Z-S

## N-CHANNEL 800V - 0.65Ω - 10.5A I²SPAK
## Zener-Protected SuperMESH™Power MOSFET

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ | Pw |
|---|---|---|---|---|
| STB12NK80Z-S | 800 V | < 0.75 Ω | 10.5 A | 190 W |

- TYPICAL $R_{DS}$(on) = 0.65 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY




**I²SPAK**

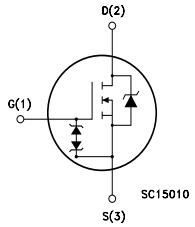
### DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

### APPLICATIONS

- IDEAL FOR HIGH DENSITY LOW PROFILE ADAPTERS

### INTERNAL SCHEMATIC DIAGRAM




### ORDERING INFORMATION

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|---|---|---|---|
| STB12NK80Z-S | B12NK80Z | I²SPAK | TUBE |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 800 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 800 | V |
| $V_{GS}$ | Gate- source Voltage | ± 30 | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°C | 10.5 | A |
| $I_D$ | Drain Current (continuous) at $T_C$ = 100°C | 6.6 | A |
| $I_{DM}$ (•) | Drain Current (pulsed) | 42 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 190 | W |
| | Derating Factor | 1.51 | W/°C |
| $V_{ESD(G-S)}$ | Gate source ESD(HBM-C=100pF, R=1.5KΩ) | 6000 | V |
| dv/dt (1) | Peak Diode Recovery voltage slope | 4.5 | V/ns |
| $T_j$<br>$T_{stg}$ | Operating Junction Temperature<br>Storage Temperature | -55 to 150 | °C |

(•) Pulse width limited by safe operating area
(1) $I_{SD}$ ≤10.5A, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$
(*) Limited only by maximum temperature allowed

## THERMAL DATA

| | | | |
|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 0.66 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 62.5 | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | 300 | °C |

## AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max) | 10.5 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 50 V) | 400 | mJ |

## GATE-SOURCE ZENER DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{GSO}$ | Gate-Source Breakdown Voltage | Igs=± 1mA (Open Drain) | 30 | | | V |

## PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ($T_{CASE}$ =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 800 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 1<br>50 | µA<br>µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 100 µA | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10V, $I_D$ = 5.25 A | | 0.65 | 0.75 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$ = 5.25 A | | 12 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input Capacitance<br>Output Capacitance<br>Reverse Transfer Capacitance | $V_{DS}$ = 25V, f = 1 MHz, $V_{GS}$ = 0 | | 2620<br>250<br>53 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (3) | Equivalent Output Capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 640V | | 100 | | pF |

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on Delay Time<br>Rise Time | $V_{DD}$ = 400 V, $I_D$ = 5.25 A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10 V<br>(Resistive Load see, Figure 3) | | 30<br>18 | | ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge | $V_{DD}$ = 640V, $I_D$ = 10.5 A,<br>$V_{GS}$ = 10V | | 87<br>14<br>44 | | nC<br>nC<br>nC |

SWITCHING OFF

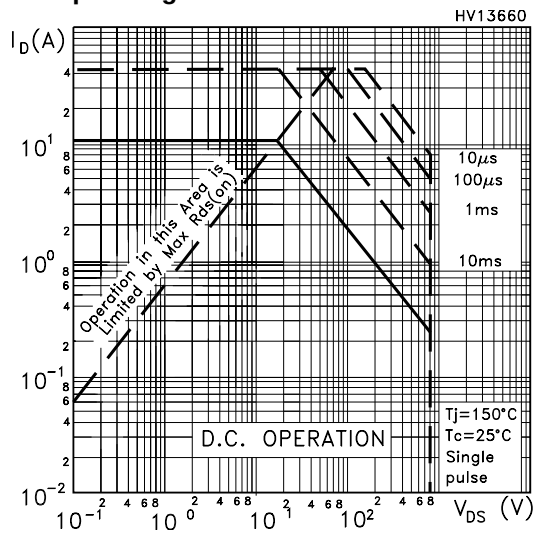
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(off)}$<br>$t_f$ | Turn-off Delay Time<br>Fall Time | $V_{DD}$ = 400 V, $I_D$ = 5.25 A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10 V<br>(Resistive Load see, Figure 3) | | 70<br>20 | | ns<br>ns |
| $t_{r(Voff)}$<br>$t_f$<br>$t_c$ | Off-voltage Rise Time<br>Fall Time<br>Cross-over Time | $V_{DD}$ = 640 V, $I_D$ = 10.5 A,<br>$R_G$ = 4.7Ω, $V_{GS}$ = 10V<br>(Inductive Load see, Figure 5) | | 16<br>15<br>28 | | ns<br>ns<br>ns |

SOURCE DRAIN DIODE

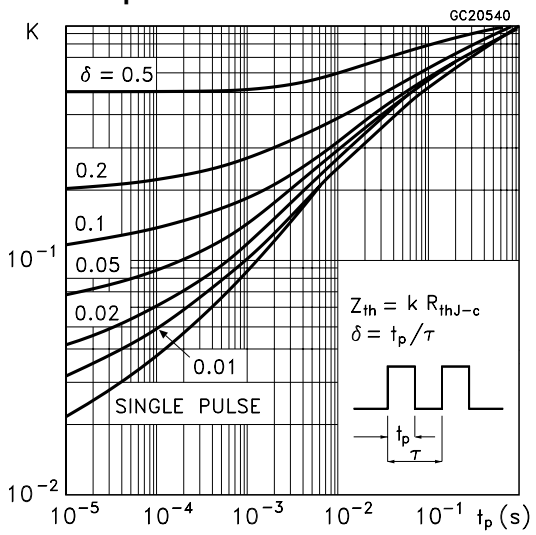
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (2) | Source-drain Current<br>Source-drain Current (pulsed) | | | | 10.5<br>42 | A<br>A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 10.5 A, $V_{GS}$ = 0 | | | 1.6 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 10.5 A, di/dt = 100A/µs<br>$V_{DD}$ = 100 V, $T_j$ = 150°C<br>(see test circuit, Figure 5) | | 635<br>5.9<br>18.5 | | ns<br>µC<br>A |

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.

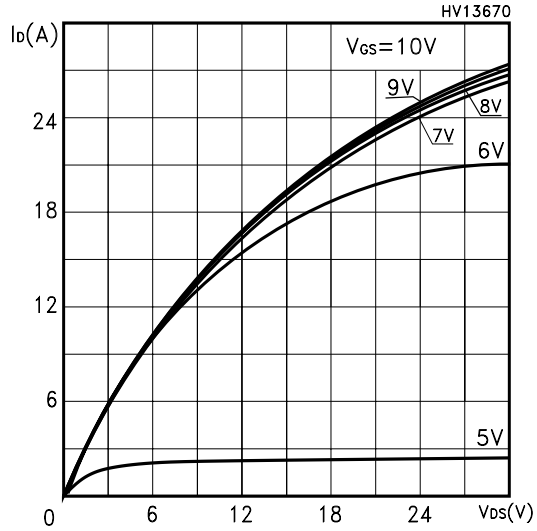
### Safe Operating Area



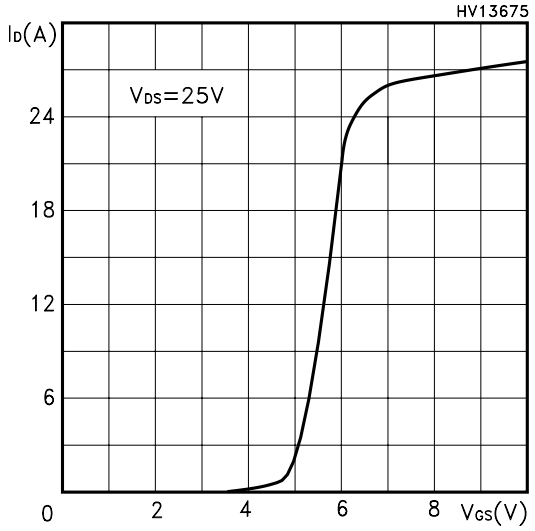

### Thermal Impedance



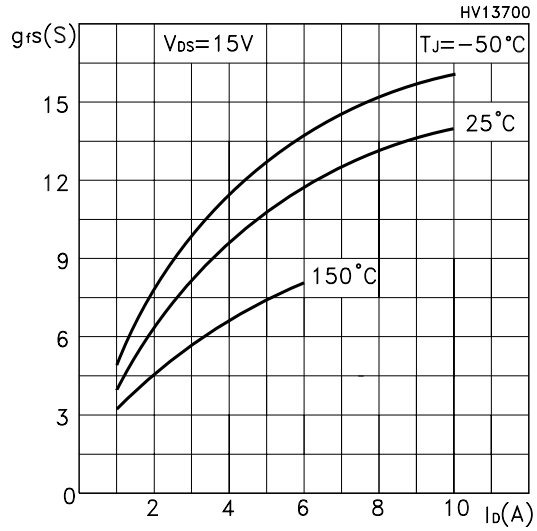

### Output Characteristics



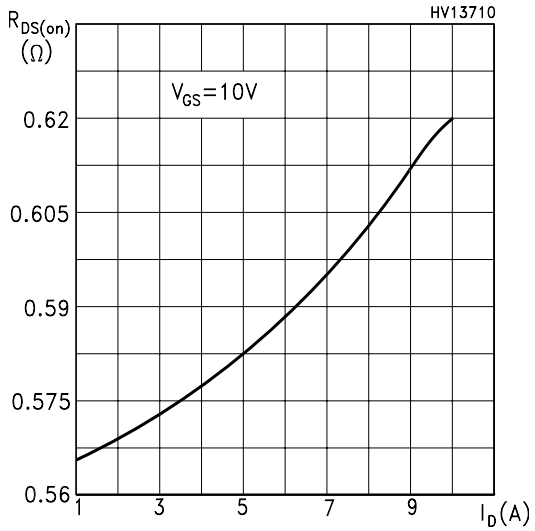

### Transfer Characteristics



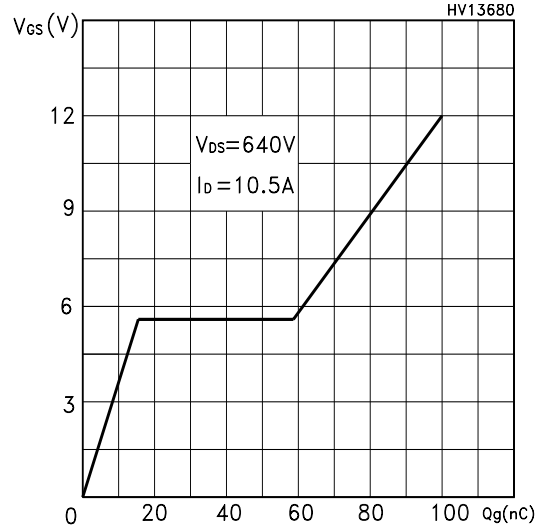

### Transconductance



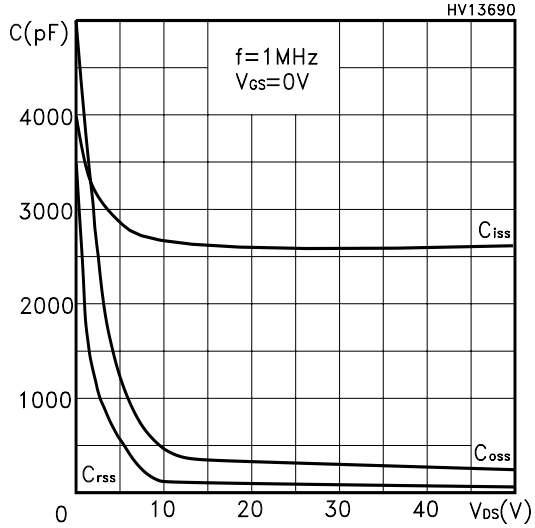

### Static Drain-source On Resistance



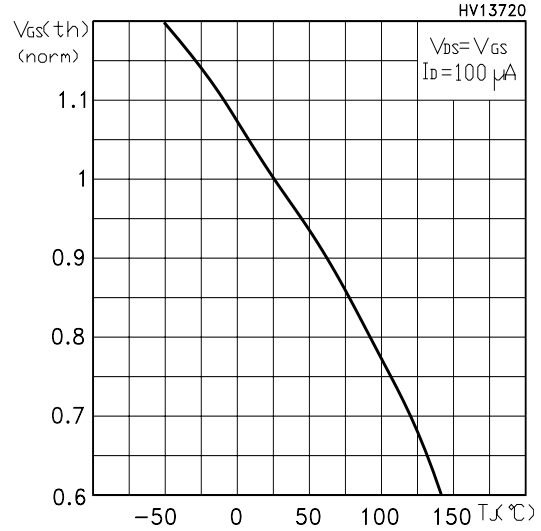
**Gate Charge vs Gate-source Voltage**



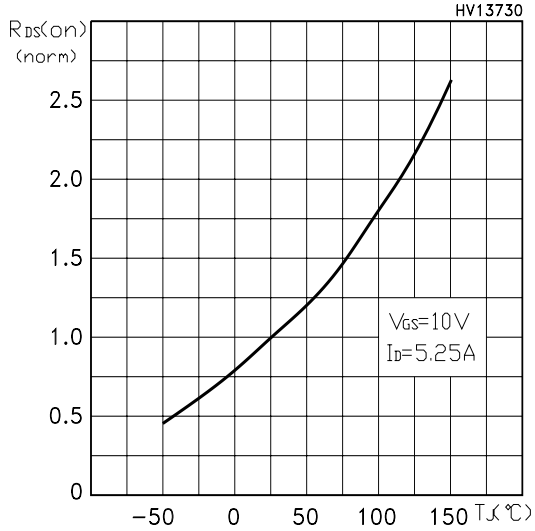

**Capacitance Variations**



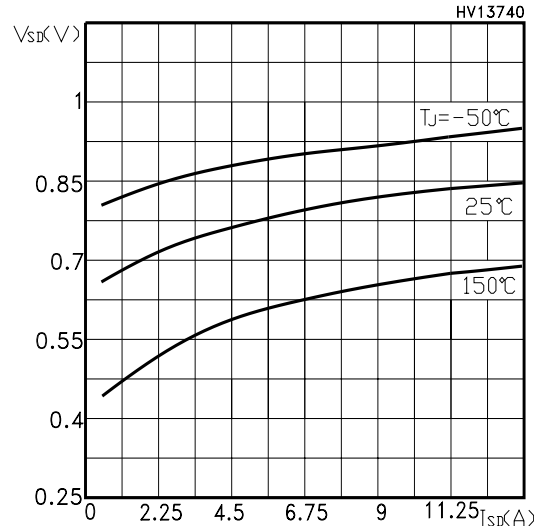

**Normalized Gate Threshold Voltage vs Temp.**



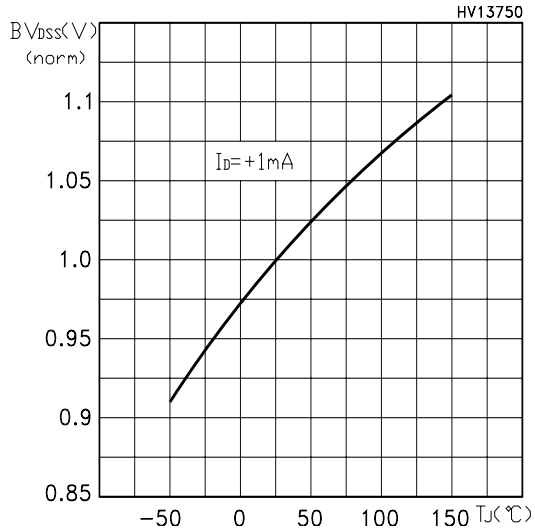

**Normalized On Resistance vs Temperature**




**Source-drain Diode Forward Characteristics**




**Normalized BVDSS vs Temperature**



### Maximum Avalanche Energy vs Temperature

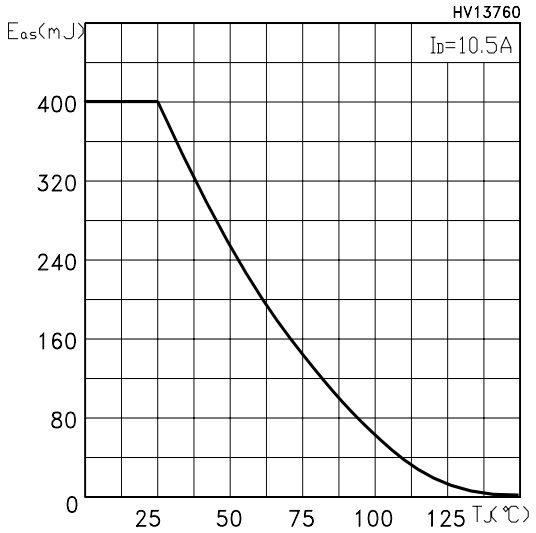


**Fig. 1:** Unclamped Inductive Load Test Circuit

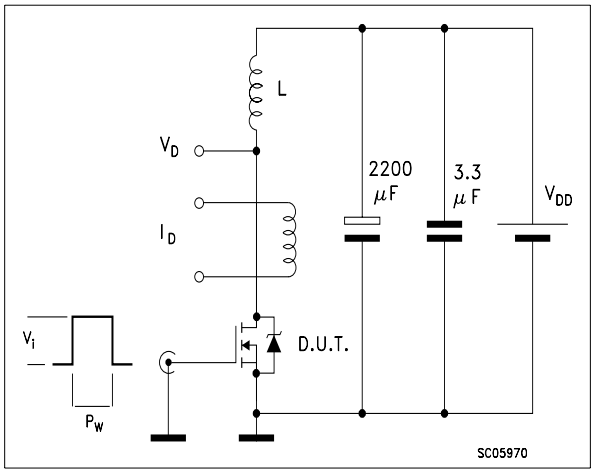



**Fig. 2:** Unclamped Inductive Waveform

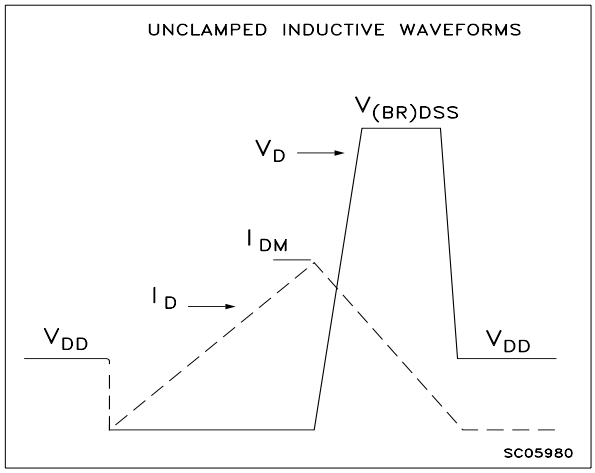



**Fig. 3:** Switching Times Test Circuit For Resistive Load

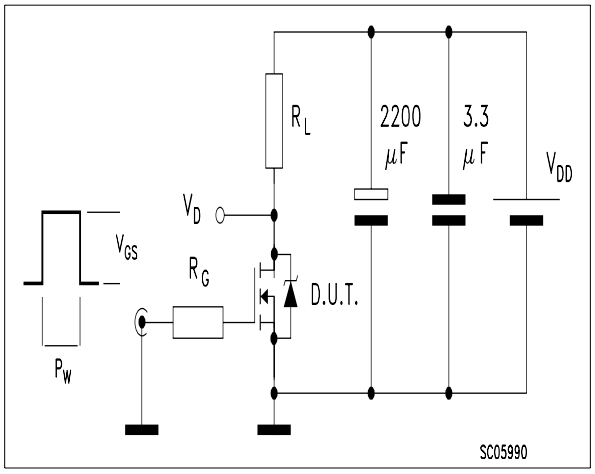



**Fig. 4:** Gate Charge test Circuit

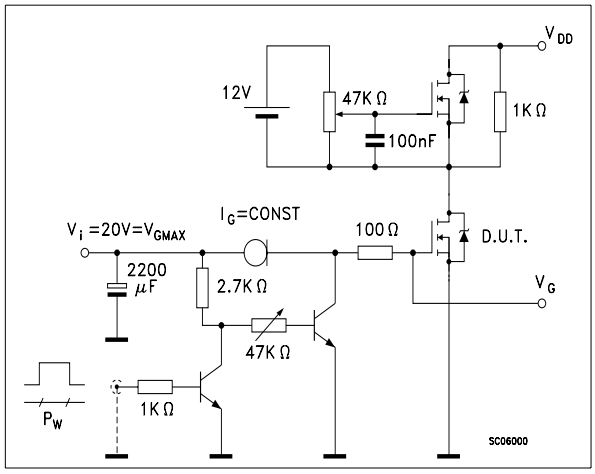
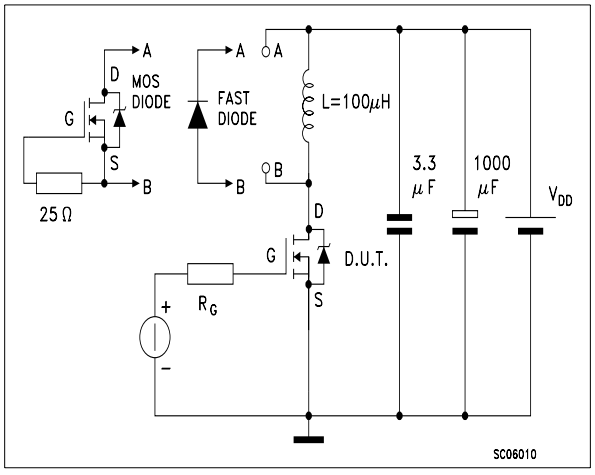
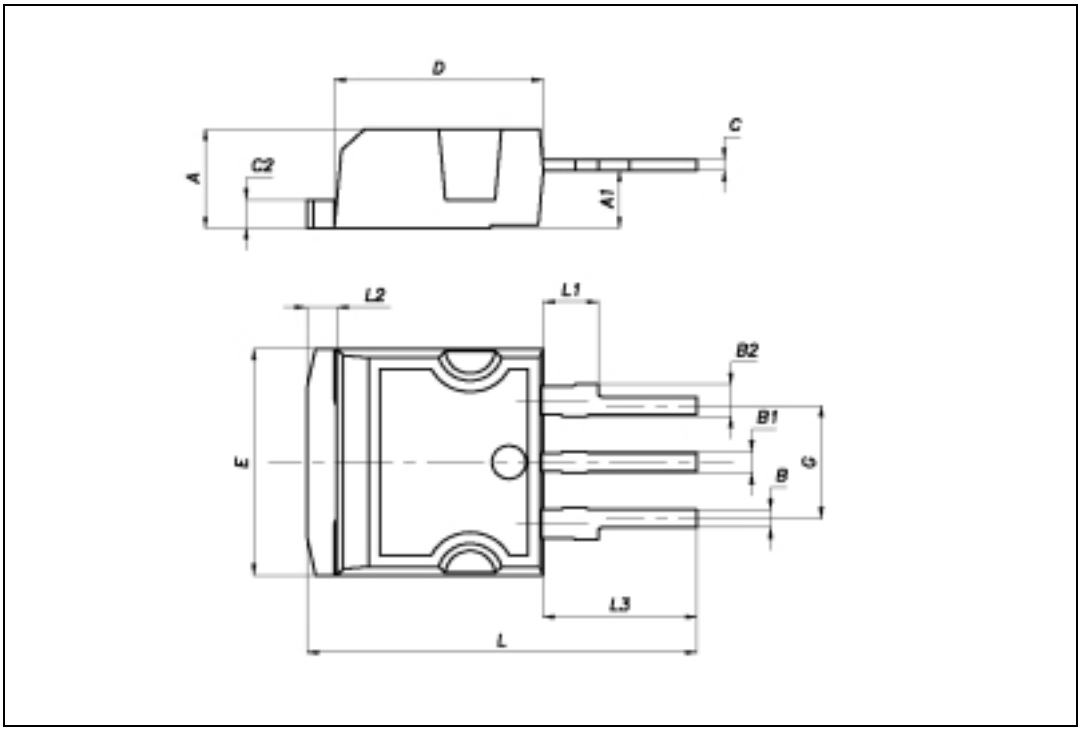



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## I²SPAK MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.40 | | 4.50 | 0.173 | | 0.177 |
| A1 | 2.50 | | 5.70 | 0.098 | | 0.106 |
| B | 0.75 | | 0.90 | 0.029 | | 0.035 |
| B1 | | | 1.10 | | | 0.043 |
| B2 | | | 1.60 | | | 0.063 |
| C | 0.45 | | 0.60 | 0.017 | | 0.023 |
| C2 | 1.25 | | 1.35 | 0.049 | | 0.053 |
| D | 9.00 | | 9.30 | 0.354 | | 0.366 |
| E | 10.00 | | 10.40 | 0.393 | | 0.409 |
| G | 4.90 | | 5.30 | 0.192 | | 0.208 |
| L | 16.80 | | 17.50 | 0.661 | | 0.689 |
| L1 | 3.60 | | 3.90 | 0.141 | | 0.153 |
| L2 | 1.22 | | 1.42 | 0.048 | | 0.056 |
| L3 | 6.50 | | 6.80 | 0.256 | | 0.267 |



**Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.**

**The ST logo is a registered trademark of STMicroelectronics**

**All other names are the property of their respective owners**

**© 2004 STMicroelectronics - All Rights Reserved**

**STMicroelectronics GROUP OF COMPANIES**

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

**http://www.st.com**