2.95 V to 6 V Input, 2 A Output, 2MHz, Synchronous Step Down Switcher With Integrated FETs (SWIFT™)

Check for Samples: TPS54218

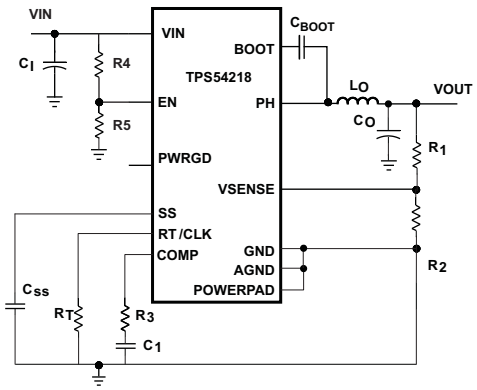
FEATURES

- **Two 30 mΩ (typical) MOSFETs for High Efficiency at 2 A loads**
- **200kHz to 2MHz Switching Frequency**
- **0.8 V ± 1% Voltage Reference Over Temperature**
- **Synchronizes to External Clock**
- **Adjustable Slow Start/Sequencing**
- **UV and OV Power Good Output**
- **Low Operating and Shutdown Quiescent Current**
- **Safe Start-up into Pre-Biased Output**
- **Cycle by Cycle Current Limit, Thermal and Frequency Fold Back Protection**
- **–40°C to 150°C Operating Junction Temperature Range**
- **Thermally Enhanced 3mm × 3mm 16-pin QFN**

APPLICATIONS

- **Low-Voltage, High-Density Power Systems**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**

SIMPLIFIED SCHEMATIC



DESCRIPTION

The TPS54218 device is a full featured 6 V, 2 A, synchronous step down current mode converter with two integrated MOSFETs.

The TPS54218 enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2 MHz switching frequency, and minimizing the IC footprint with a small 3mm x 3mm thermally enhanced QFN package.

The TPS54218 provides accurate regulation for a variety of loads with an accurate ±1% Voltage Reference (V_{ref}) over temperature.

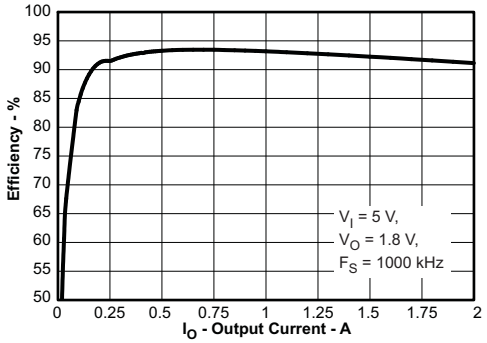
Efficiency is maximized through the integrated 30mΩ MOSFETs and 350µA typical supply current. Using the enable pin, shutdown supply current is reduced to 2 µA by entering a shutdown mode.

Undervoltage lockout is internally set at 2.6 V, but can be increased by programming the threshold with a resistor network on the enable pin. The output voltage startup ramp is controlled by the slow start pin. An open drain power good signal indicates the output is within 93% to 107% of its nominal voltage.

Frequency fold back and thermal shutdown protects the device during an overcurrent condition.

The TPS54218 is supported in the SwitcherPro™ Software Tool at www.ti.com/switcherpro.

For more SWIFT™ documentation, see the TI website at www.ti.com/swift.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGE	PART NUMBER(1)
–40°C to 150°C	3 × 3 mm QFN	TPS54218RTET
		TPS54218RTER

(1) The RTE package is only available taped and reeled. To order, add the suffix “R” to the end of the part number for a reel of 3000, or add the suffix “T” to the end of the part number for a reel of 250 (e.g., TPS54218RTER).

ABSOLUTE MAXIMUM RATINGS

		VALUE	UNIT
Input voltage	VIN	–0.3 to 7	V
	EN	–0.3 to 7	
	BOOT	PH + 8	
	VSENSE	–0.3 to 3	
	COMP	–0.3 to 3	
	PWRGD	–0.3 to 7	
	SS	–0.3 to 3	
	RT/CLK	–0.3 to 6	
Output voltage	BOOT-PH	8	V
	PH	–0.6 to 7	
	PH 10 ns Transient	–2 to 7	
Source current	EN	100	µA
	RT/CLK	100	µA
Sink current	COMP	100	µA
	PWRGD	10	mA
	SS	100	µA
Electrostatic discharge (HBM)		2	kV
Electrostatic discharge (CDM)		500	V
Operating Junction temperature, T_j		–40 to 150	°C
Storage temperature, T_{stg}		–65 to 150	°C

PACKAGE DISSIPATION RATINGS(1) (2) (3)

over operating free-air temperature range (unless otherwise noted)

PACKAGE	THERMAL IMPEDANCE JUNCTION TO AMBIENT	φ_{JT} THERMAL CHARACTERISTIC JUNCTION TO TOP
RTE	37°C/W	1°C/W

(1) Maximum power dissipation may be limited by overcurrent protection
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 150°C for best performance and long-term reliability. See power dissipation estimate in application section of this data sheet for more information.
(3) Test boards conditions:
(a) 2 inches x 2 inches, 4 layers, thickness: 0.062 inch
(b) 2 oz. copper traces located on the top of the PCB
(c) 2 oz. copper ground planes on the 2 internal layers and bottom layer
(d) 4 thermal vias (10mil) located under the device package

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ELECTRICAL CHARACTERISTICS

T_J = –40°C to 150°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		2.95		6	V
Internal under voltage lockout threshold	No voltage hysteresis, rising and falling		2.6	2.8	V
Shutdown supply current	EN = 0 V, 25°C, 2.95 V ≤ VIN ≤ 6 V		2	5	µA
Quiescent Current - I_q	VSENSE = 0.9 V, VIN = 5 V, 25°C, R_T = 400 kΩ		350	500	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising	1.16	1.25	1.37	V
	Falling		1.18		
Input current	Enable rising threshold + 50 mV		-3.2		µA
	Enable falling threshold – 50 mV		-0.65		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage Reference	2.95 V ≤ VIN ≤ 6 V, –40°C <T_J < 150°C	0.795	0.803	0.811	V
MOSFET					
High side switch resistance	BOOT-PH = 5 V		30	60	mΩ
	BOOT-PH = 2.95 V		44	70	
Low side switch resistance	VIN = 5 V		30	60	mΩ
	VIN = 2.95 V		44	70	
ERROR AMPLIFIER					
Input current			7		nA
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		225		µmhos
Error amplifier transconductance (gm) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, VSENSE = 0.4 V		70		µmhos
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±20		µA
COMP to Iswitch gm			13		A/V
CURRENT LIMIT					
Current limit threshold	Instantaneous peak current	2.9	3.6		A
THERMAL SHUTDOWN					
Thermal Shutdown			175		°C
Hysteresis			15		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching frequency range using RT mode		200		2000	kHz
Switching frequency	R_T = 400 kΩ	400	500	600	kHz
Switching frequency range using CLK mode		300		2000	kHz
Minimum CLK pulse width		75			ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 400kΩ		0.5		V
RT/CLK high threshold			1.6	2.2	V
RT/CLK low threshold		0.4	0.6		V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with R_T resistor in series		90		ns
PLL lock in time	Measure at 500 kHz		14		µs
PH (PH PIN)					
Minimum On time	Measured at 50% points on PH, I_{OUT} = 2 A		60		ns
	Measured at 50% points on PH, VIN = 5 V, I_{OUT} = 0 A		110		
Minimum Off time	Prior to skipping off pulses, BOOT-PH = 2.95 V, I_{OUT} = 2 A		60		ns
Rise/Fall Time	VIN = 5 V		1.5		V/ns

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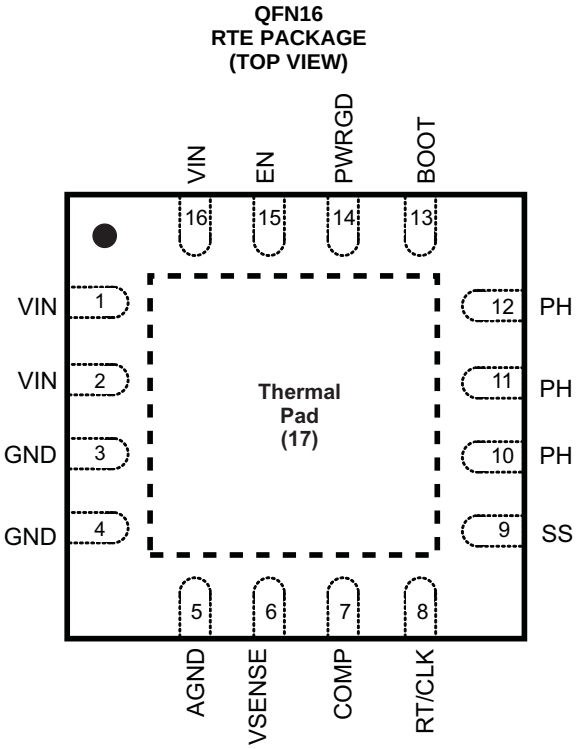
ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 150°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BOOT (BOOT PIN)					
BOOT Charge Resistance	VIN = 5 V		16		Ω
BOOT-PH UVLO	VIN = 2.95 V		2.1		V
SLOW START (SS PIN)					
Charge Current	$V_{(SS)}$ = 0.4 V		1.8		µA
SS to reference crossover	98% nominal		0.9		V
SS discharge voltage (overload)	VSENSE = 0 V		20		µA
SS discharge current (UVLO, EN, Thermal Fault)	VIN = 5 V, $V_{(SS)}$ = 0.5 V		1.25		mA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91		% Vref
	VSENSE rising (Good)		93		% Vref
	VSENSE rising (Fault)		107		% Vref
	VSENSE falling (Good)		105		% Vref
Hysteresis	VSENSE falling		2		% Vref
Output high leakage	VSENSE = VREF, $V_{(PWRGD)}$ = 5.5 V		2		nA
On resistance			100		Ω
Output low	$I_{(PWRGD)}$ = 3.5 mA		0.3		V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		1.2	1.6	V

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PIN CONFIGURATION

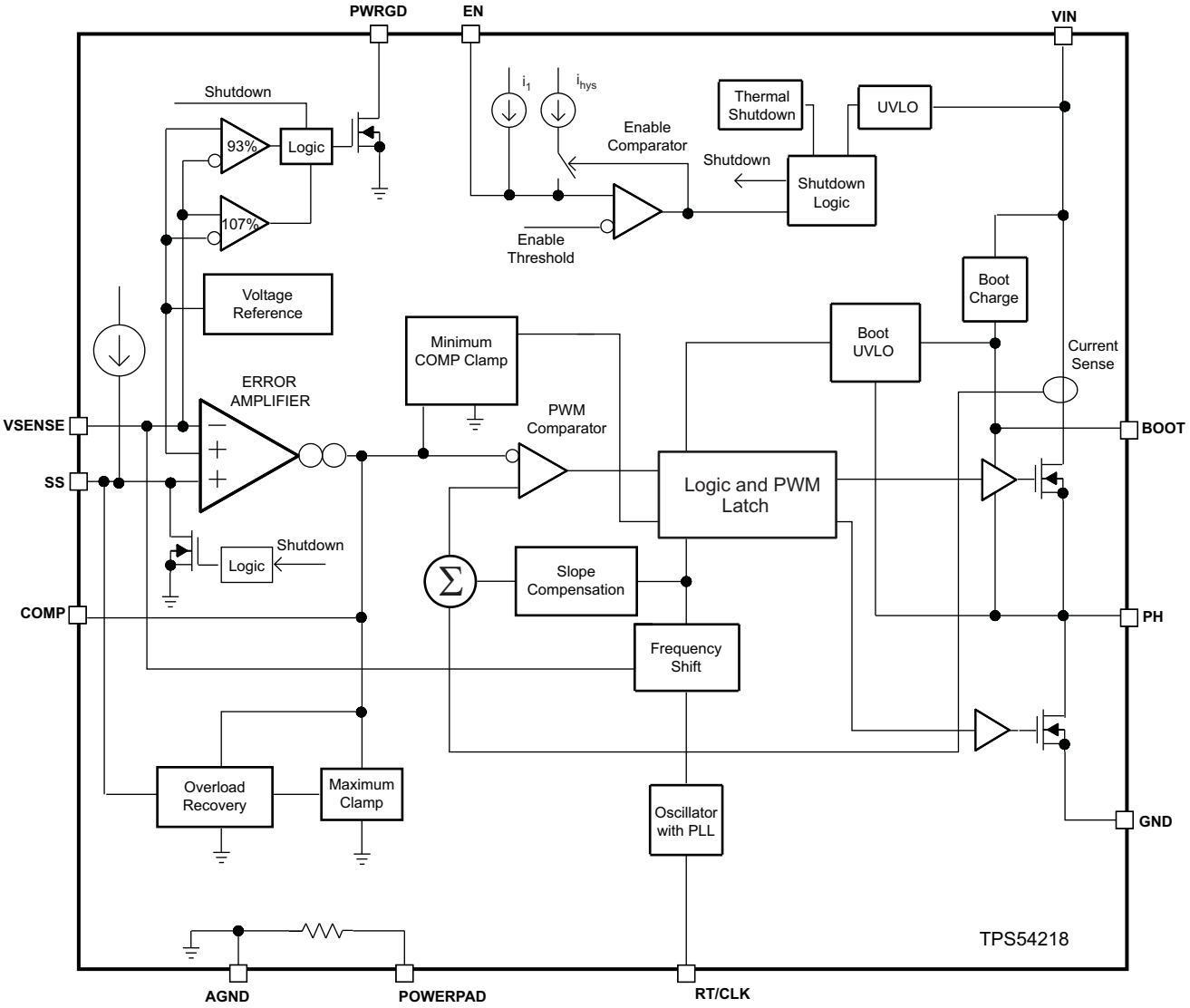


PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
AGND	5	Analog Ground should be electrically connected to GND close to the device.
BOOT	13	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
COMP	7	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	Enable pin, internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
GND	3, 4	Power Ground. This pin should be electrically connected directly to the power pad under the IC.
PH	10, 11, 12	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous) rectifier MOSFET.
PowerPAD	17	GND pin should be connected to the exposed power pad for proper operation. This power pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.
PWRGD	14	An open drain output, asserts low if output voltage is low due to thermal shutdown, overcurrent, over/under-voltage or EN shut down.
RT/CLK	8	Resistor Timing or External Clock input pin.
SS	9	Slow-start. An external capacitor connected to this pin sets the output voltage rise time.
VIN	1, 2, 16	Input supply voltage, 2.95 V to 6 V.
VSENSE	6	Inverting node of the transconductance (gm) error amplifier.

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FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS CURVES

HIGH SIDE AND LOW SIDE $R_{DS\ (on)}$ vs TEMPERATURE

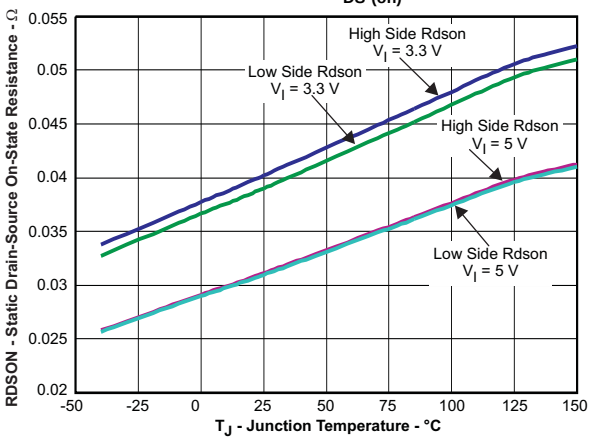


Figure 1.

FREQUENCY vs TEMPERATURE

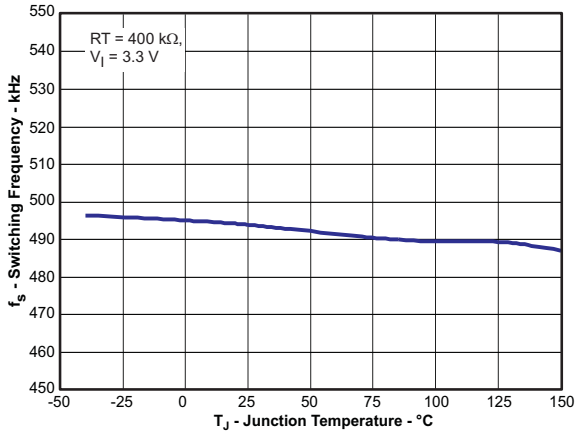


Figure 2.

HIGH SIDE CURRENT LIMIT vs TEMPERATURE

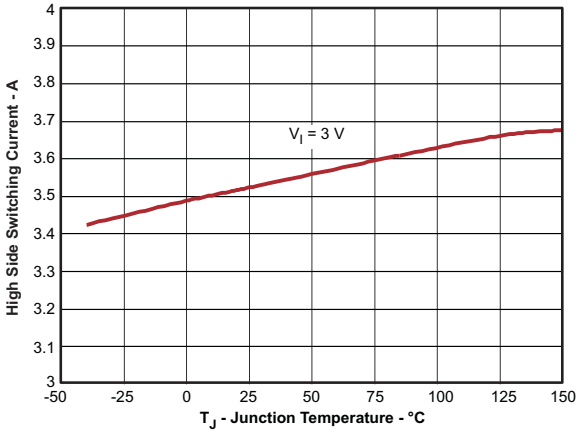


Figure 3.

VOLTAGE REFERENCE vs TEMPERATURE

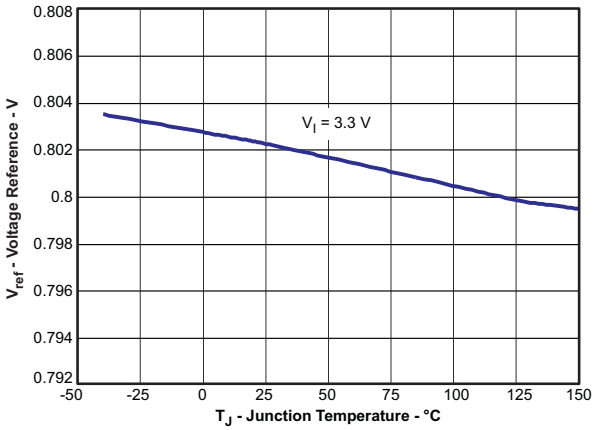


Figure 4.

SWITCHING FREQUENCY vs RT RESISTANCE LOW FREQUENCY RANGE

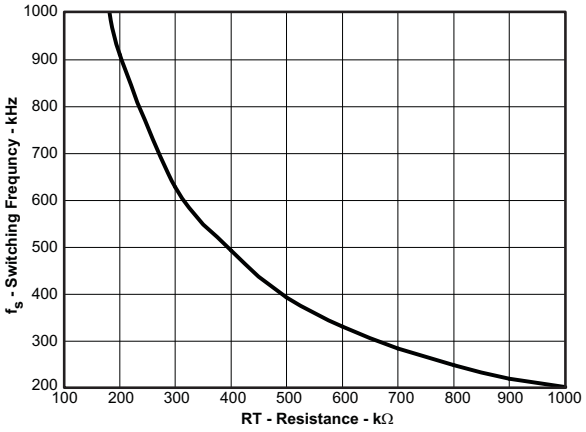


Figure 5.

SWITCHING FREQUENCY vs RT RESISTANCE HIGH FREQUENCY RANGE

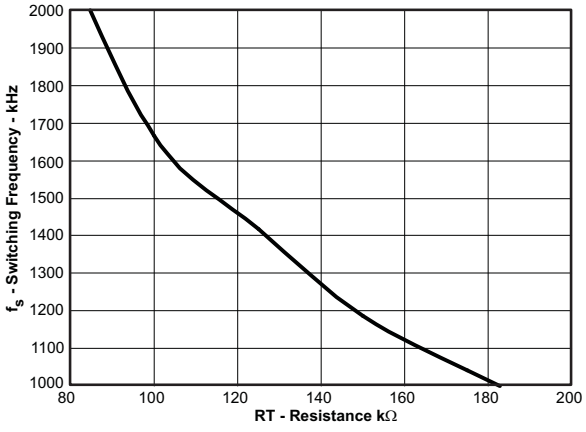


Figure 6.

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TYPICAL CHARACTERISTICS CURVES (continued)

SWITCHING FREQUENCY vs VSENSE

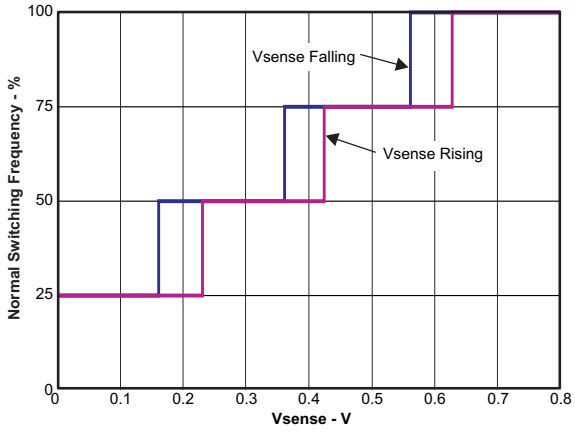


Figure 7.

TRANSCONDUCTANCE vs TEMPERATURE

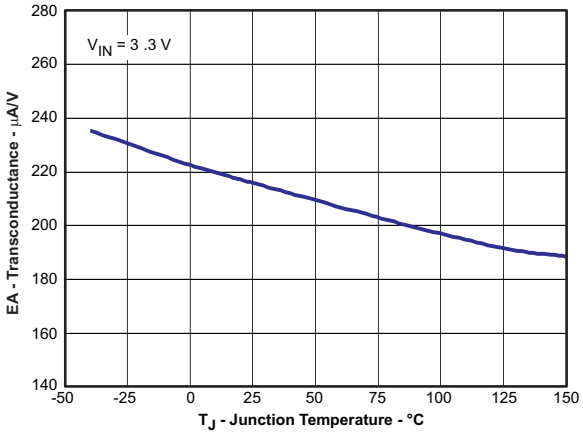


Figure 8.

TRANSCONDUCTANCE (SLOW START) vs JUNCTION TEMPERATURE

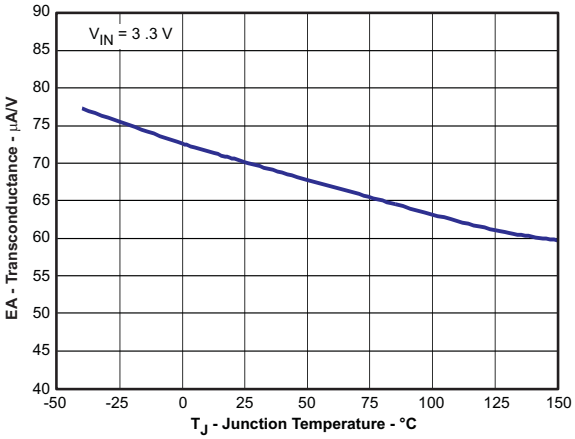


Figure 9.

ENABLE PIN VOLTAGE vs TEMPERATURE

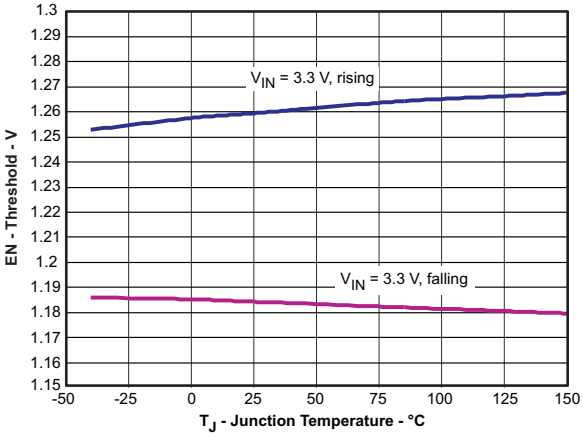


Figure 10.

PIN CURRENT vs TEMPERATURE

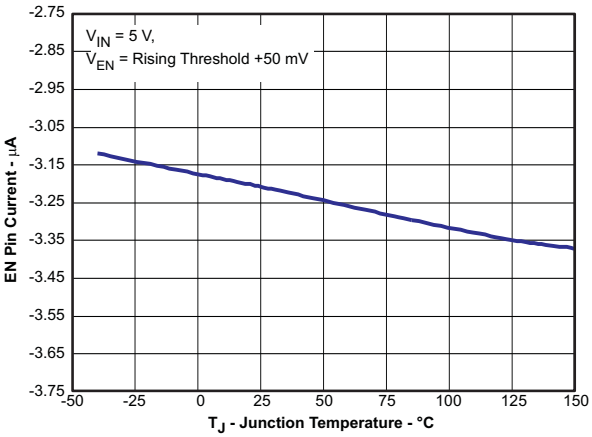


Figure 11.

PIN CURRENT vs TEMPERATURE

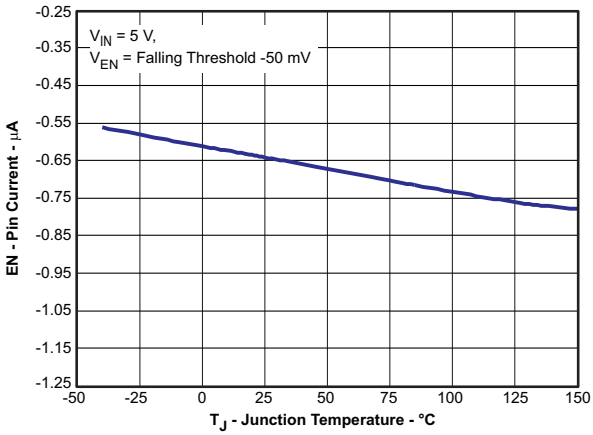


Figure 12.

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TYPICAL CHARACTERISTICS CURVES (continued)

CHARGE CURRENT vs TEMPERATURE

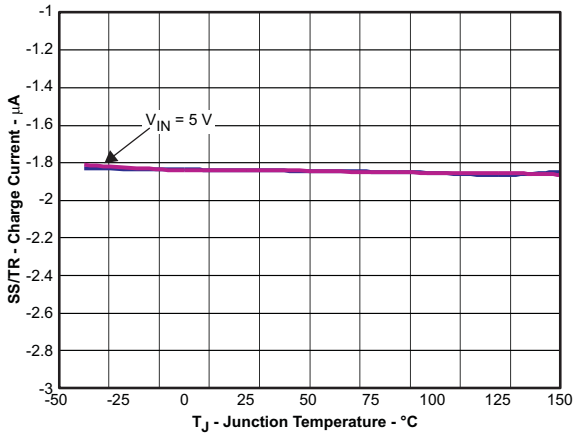


Figure 13.

DISCHARGE CURRENT vs TEMPERATURE

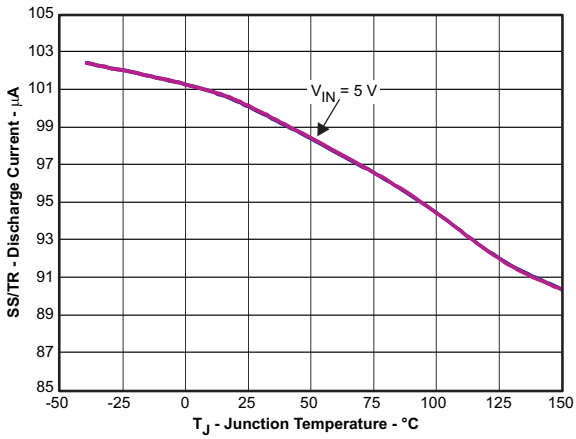


Figure 14.

INPUT VOLTAGE vs TEMPERATURE

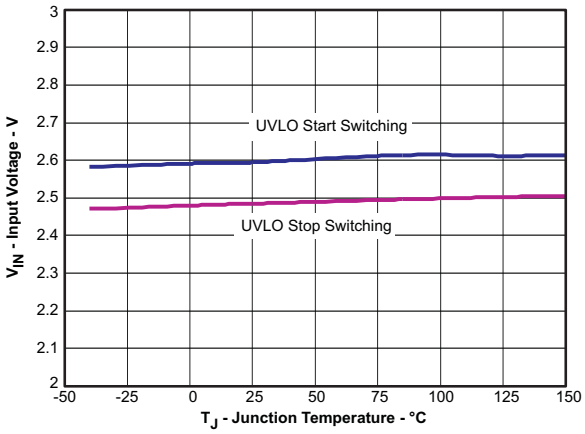


Figure 15.

SHUTDOWN SUPPLY CURRENT vs TEMPERATURE

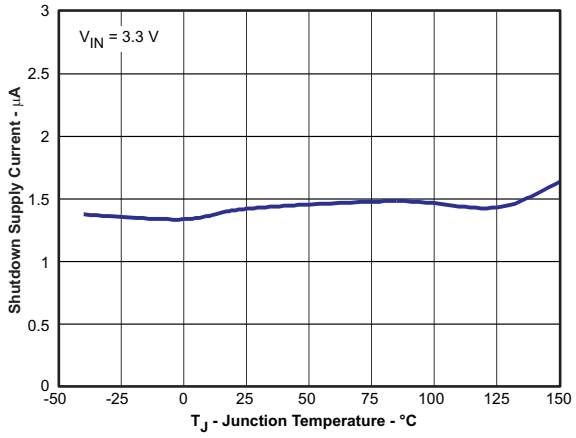


Figure 16.

SHUTDOWN SUPPLY CURRENT vs INPUT VOLTAGE

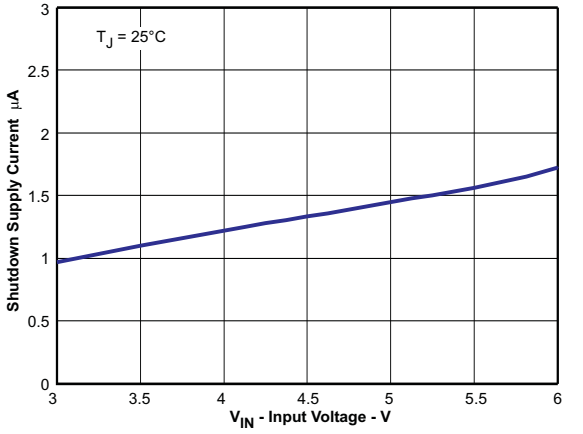


Figure 17.

SUPPLY CURRENT vs TEMPERATURE

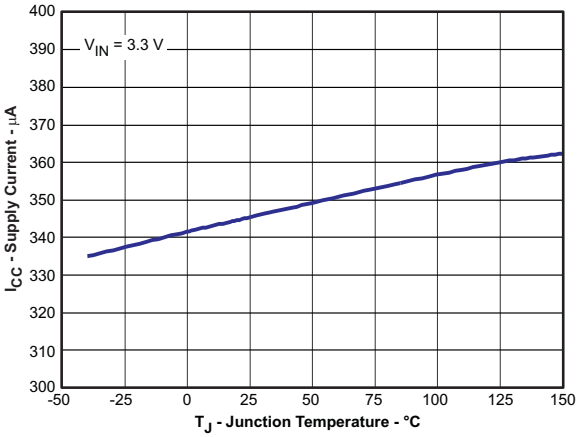


Figure 18.

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TYPICAL CHARACTERISTICS CURVES (continued)

SUPPLY CURRENT vs INPUT VOLTAGE

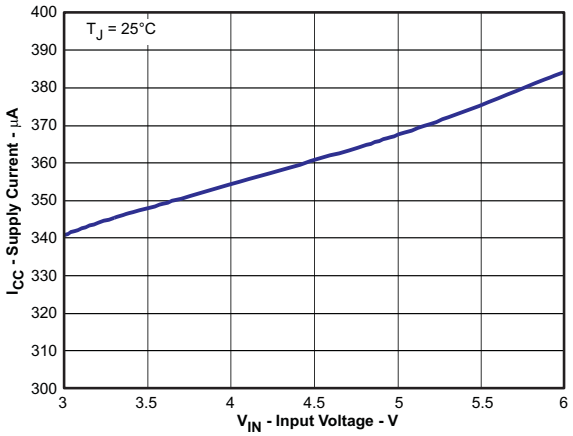


Figure 19.

PWRGD THRESHOLD vs TEMPERATURE

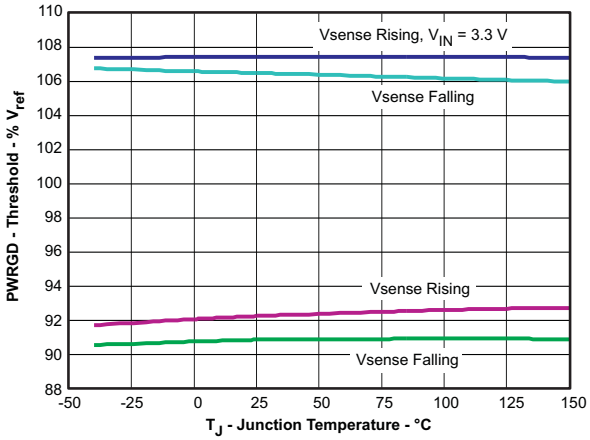


Figure 20.

PWRGD ON RESISTANCE vs TEMPERATURE

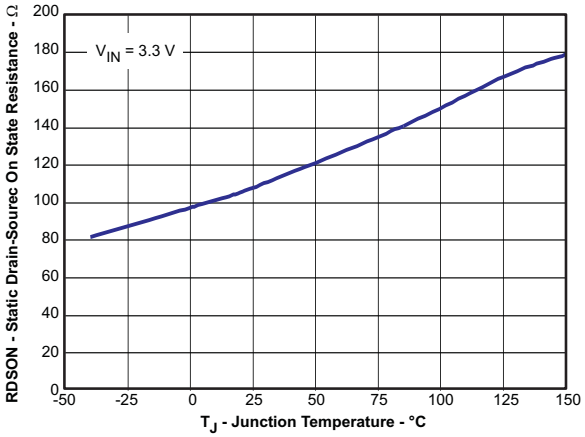


Figure 21.

OVERVIEW

The TPS54218 is a 6-V, 2 A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54218 has a typical default start up voltage of 2.6 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS54218 is 350 µA when not switching and under no load. When the device is disabled, the supply current is less than 5 µA.

The integrated 30 mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 2 amperes.

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The TPS54218 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54218 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.8 V reference.

The TPS54218 has a power good comparator (PWRGD) with 2% hysteresis.

The TPS54218 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power good comparator. When the regulated output voltage is greater than 109% of the nominal voltage, the overvoltage comparator is activated, and the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 105%.

The SS (slow start) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for slow start. The SS pin is discharged before the output power up to ensure a repeatable restart after an over-temperature fault, UVLO fault or disabled condition.

The use of a frequency foldback circuit reduces the switching frequency during startup and over current fault conditions to help limit the inductor current.

DETAILED DESCRIPTION

FIXED FREQUENCY PWM CONTROL

The TPS54218 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

SLOPE COMPENSATION AND OUTPUT CURRENT

The TPS54218 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

BOOTSTRAP VOLTAGE (BOOT) AND LOW DROPOUT OPERATION

The TPS54218 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics overtemperature and voltage.

To improve drop out, the TPS54218 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.5 V. The high side MOSFET is turned off using an UVLO circuit, allowing for the low side MOSFET to conduct when the voltage from BOOT to PH drops below 2.5 V. Since the supply current sourced from the BOOT pin is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

ERROR AMPLIFIER

The TPS54218 has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS pin voltage or the internal 0.8 V voltage reference. The transconductance of the error amplifier is 225 µA/V during normal operation. When the voltage of VSENSE pin is below 0.8 V and the device is regulating using the SS voltage, the gm is 70 µA/V. The frequency compensation components are placed between the COMP pin and ground.

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VOLTAGE REFERENCE

The voltage reference system produces a precise ±1% voltage reference overtemperature by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits produce 0.8 V at the non-inverting input of the error amplifier.

ADJUSTING THE OUTPUT VOLTAGE

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 100 kΩ for the R1 resistor and use the Equation 1 to calculate R2. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.8\ V}{V_O - 0.8\ V} \right) \quad (1)$$

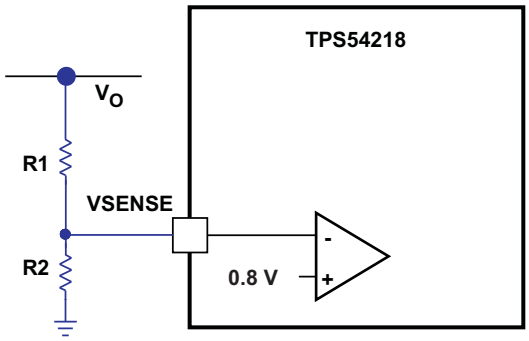


Figure 22. Voltage Divider Circuit

ENABLE AND ADJUSTING UNDER-VOLTAGE LOCKOUT

The TPS54218 is disabled when the VIN pin voltage falls below 2.6 V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 23 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (V_{STOP}) above 2.7 V. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pull-up current source that provides the default condition of the TPS54218 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 2.55 µA of hysteresis is added. When the EN pin is pulled below 1.18 V, the 2.55 µA is removed. This additional current facilitates input voltage hysteresis.

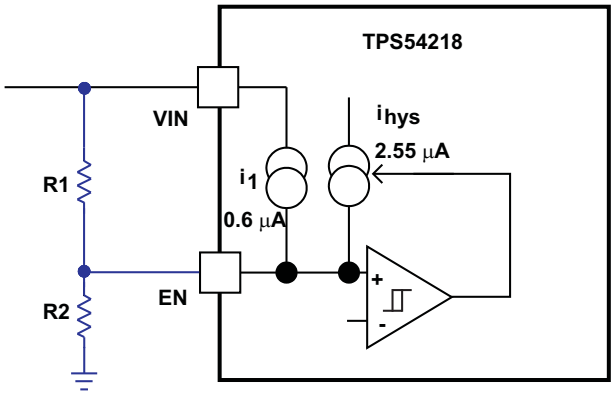


Figure 23. Adjustable Under Voltage Lock Out

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$$R1 = \frac{0.944 \cdot V_{START} - V_{STOP}}{2.59 \times 10^{-6}} \quad (2)$$

$$R2 = \frac{1.18 \cdot R1}{V_{STOP} - 1.18 + R1 \cdot 3.2 \times 10^{-6}} \quad (3)$$

SLOW START PIN

The TPS54218 regulates to the lower of the SS pin and the internal reference voltage. A capacitor on the SS pin to ground implements a slow start time. The TPS54218 has an internal pull-up current source of 1.8µA which charges the external slow start capacitor. Equation 4 calculates the required slow start capacitor value where Tss is the desired slow start time in ms, I_{SS} is the internal slow start charging current of 1.8 µA, and Vref is the internal voltage reference of 0.8 V.

$$C_{SS}(nF) = \frac{T_{SS}(mS) \times I_{SS}(\mu A)}{V_{ref}(V)} \quad (4)$$

If during normal operation, the VIN goes below the UVLO, EN pin pulled below 1.2 V, or a thermal shutdown event occurs, the TPS54218 stops switching and the SS is discharged to 0 volts before reinitiating a powering up sequence.

SEQUENCING

Many of the common power supply sequencing methods can be implemented using the SS, EN and PWRGD pins. The sequential method can be implemented using an open drain or collector output of a power on reset pin of another device. Figure 24 shows the sequential method. The power good is coupled to the EN pin on the TPS54218 which enables the second power supply once the primary supply reaches regulation.

Ratiometric start up can be accomplished by connecting the SS pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time the pull up current source must be doubled in Equation 4. The ratiometric method is illustrated in Figure 26.

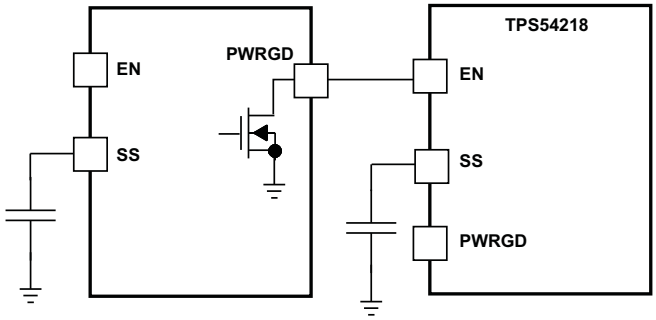


Figure 24. Sequential Start-Up Sequence

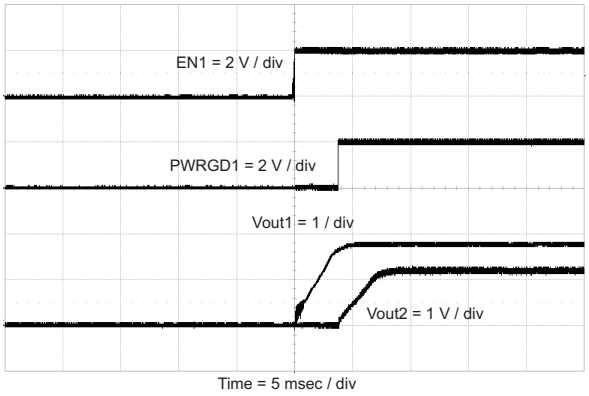


Figure 25. Sequential Startup using EN and PWRGD

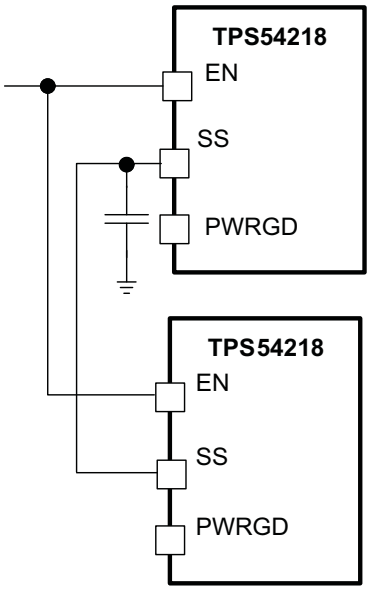


Figure 26. Schematic for Ratiometric Start-Up Sequence

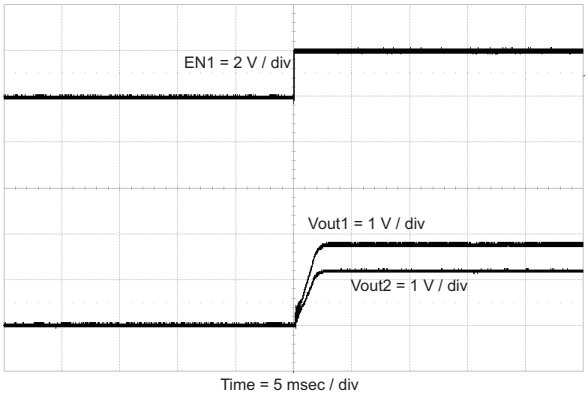


Figure 27. Ratiometric Start-Up using Coupled SS Pins

CONSTANT SWITCHING FREQUENCY and TIMING RESISTOR (RT/CLK Pin)

The switching frequency of the TPS54218 is adjustable over a wide range from 200 kHz to 2000 kHz by placing a maximum of 1000kΩ and minimum of 85 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in Figures 5 and 6, or Equation 5.

$$RT\ (k\Omega) = \frac{311890}{Fsw(kHz)^{1.0793}} \quad (5)$$

$$Fsw(kHz) = \frac{133870}{RT(k\Omega)^{0.9393}} \quad (6)$$

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is typically 60 ns at full current load and 110 ns at no load, and limits the maximum operating input voltage or output voltage.

OVERCURRENT PROTECTION

The TPS54218 implements a cycle by cycle current limit. During each switching cycle the high side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

FREQUENCY SHIFT

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS54218 implements a frequency shift. If frequency shift was not implemented, during an overcurrent condition the low side MOSFET may not be turned off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, during an overcurrent condition the switching frequency is reduced from 100%, then 75%, then 50%, then 25% as the voltage decreases from 0.8 to 0 volts on VSENSE pin to allow the low side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 to 0.8 volts. See Figure 7 for details.

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REVERSE OVERCURRENT PROTECTION

The TPS54218 implements low side current protection by detecting the voltage across the low side MOSFET. When the converter sinks current through its low side FET, the control circuit turns off the low side MOSFET if the reverse current is more than 1.3 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into pre-biased outputs.

SYNCHRONIZE USING THE RT/CLK PIN

The RT/CLK pin is used to synchronize the converter to an external system clock. See Figure 28. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on time of at least 75ns. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to the frequency set by the resistor. The square wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V typically. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin.

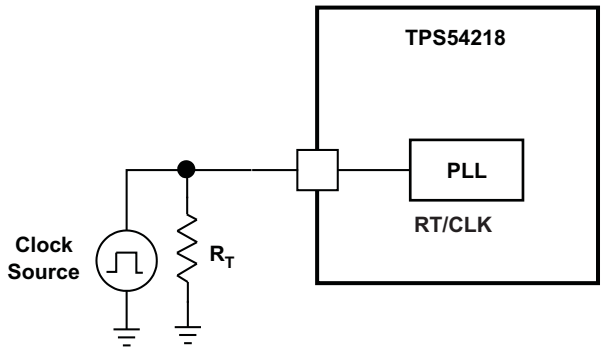


Figure 28. Synchronizing to a System Clock

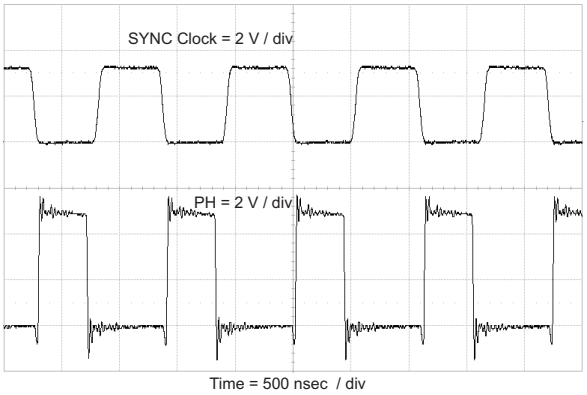


Figure 29. Plot of Synchronizing to System Clock

POWER GOOD (PWRGD PIN)

The PWRGD pin output is an open drain MOSFET. The output is pulled low when the VSENSE voltage enters the fault condition by falling below 91% or rising above 107% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 105% of the internal voltage reference the PWRGD output MOSFET is turned off. It is recommended to use a pull-up resistor between the values of 1kΩ and 100kΩ to a voltage source that is 6 V or less. The PWRGD is in a valid state once the VIN input voltage is greater than 1.2 V.

OVERVOLTAGE TRANSIENT PROTECTION

The TPS54218 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold the high side MOSFET is allowed to turn on the next clock cycle.

THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 160°C, the device reinitiates the power up sequence by discharging the SS pin to 0 volts. The thermal shutdown hysteresis is 15°C.

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SMALL SIGNAL MODEL FOR LOOP RESPONSE

Figure 30 shows an equivalent model for the TPS54218 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm of 225 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Ro and capacitor Co model the open loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

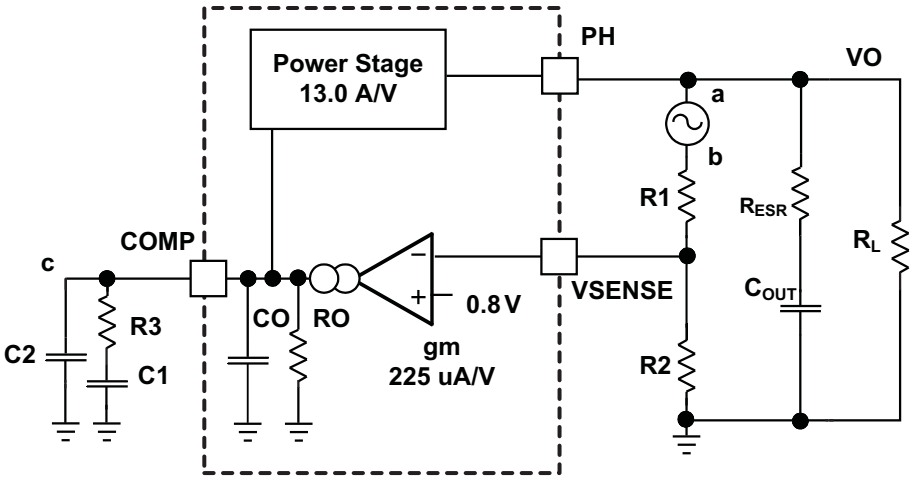


Figure 30. Small Signal Model for Loop Response

SIMPLE SMALL SIGNAL MODEL FOR PEAK CURRENT MODE CONTROL

Figure 30 is a simple small signal model that can be used to understand how to design the frequency compensation. The TPS54218 power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 7 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 30) is the power stage transconductance. The gm for the TPS54218 is 13 A/V. The low frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 8. As the load current increases and decreases, the low frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current [see Equation 9]. The combined effect is highlighted by the dashed line in the right half of Figure 31. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

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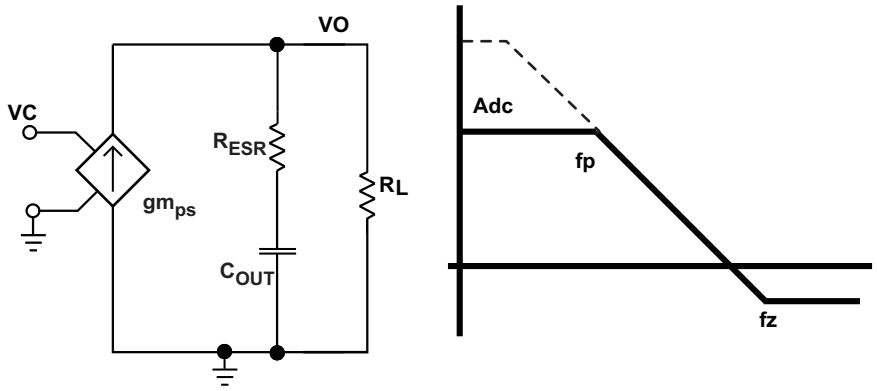


Figure 31. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (7)$$

$$Adc = gm_{ps} \times R_L \quad (8)$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (9)$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (10)$$

SMALL SIGNAL MODEL FOR FREQUENCY COMPENSATION

The TPS54218 uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in Figure 32. The Type 2 circuits are most likely implemented in high bandwidth power supply designs using low ESR output capacitors. In Type 2A, one additional high frequency pole is added to attenuate high frequency noise.

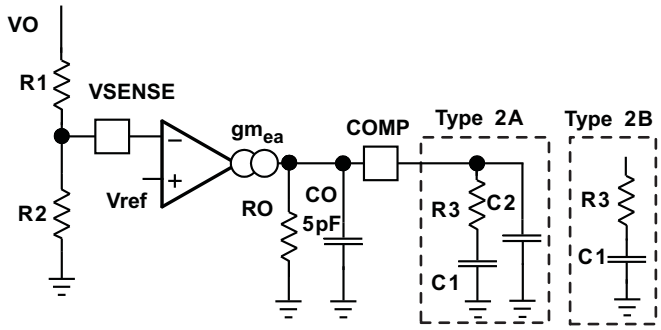


Figure 32. Types of Frequency Compensation

The design guidelines for TPS54218 loop compensation are as follows:

1. The modulator pole, fpmod, and the esr zero, fz1 must be calculated using Equation 11 and Equation 12. Derating the output capacitor (C_{OUT}) may be needed if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use Equation 13 and Equation 14 to estimate a starting point for the crossover frequency, fc. Equation 13 is the geometric mean of the modulator pole and the esr zero and Equation 14 is the mean of modulator pole and the switching frequency. Use the lower value of Equation 13 or Equation 14 as the maximum crossover frequency.

$$fp\ mod = \frac{I_{OUT}\ max}{2\pi \times V_{OUT} \times C_{OUT}} \quad (11)$$

$$fz\ mod = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (12)$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \quad (13)$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \quad (14)$$

2. R3 can be determined by

$$R3 = \frac{2\pi \times fc \times V_{OUT} \times C_{OUT}}{gm_{ea} \times V_{ref} \times gm_{ps}} \quad (15)$$

   Where is the gm_{ea} amplifier gain (225 µA/V), gm_{ps} is the power stage gain (13 A/V).

3. Place a compensation zero at the dominant pole $fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$. C1 can be determined by

$$C1 = \frac{R_L \times C_{OUT}}{R3} \quad (16)$$

4. C2 is optional. It can be used to cancel the zero from te C_{OUT} ESR.

$$C2 = \frac{R_{ESR} \times C_{OUT}}{R3} \quad (17)$$

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APPLICATION INFORMATION

DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE

This example details the design of a high frequency switching regulator design using ceramic output capacitors. This design is available as the HPA511 evaluation module (EVM). A few parameters must be known in order to start the design process. These parameters are typically determined on the system level. For this example, we start with the following known parameters:

Output Voltage	1.8 V
Transient Response 1 to 2A load step	ΔV_{OUT} = 3%
Maximum Output Current	2 A
Input Voltage	3.3 V nom. 3 V to 6 V
Output Voltage Ripple	< 30 mV_{PP}
Start Input Voltage (rising VIN)	3.1 V
Stop Input Voltage (falling VIN)	2.8 V
Switching Frequency (Fsw)	1000 kHz

SELECTING THE SWITCHING FREQUENCY

The first step is to decide on a switching frequency for the regulator. Typically, you want to choose the highest switching frequency possible since this produces the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 200 kHz to 2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 1MHz is selected to achieve both a small solution size and a high efficiency operation. Using Equation 5, R4 is calculated to be 180 kΩ. A standard 1% 182 kΩ value was chosen in the design.

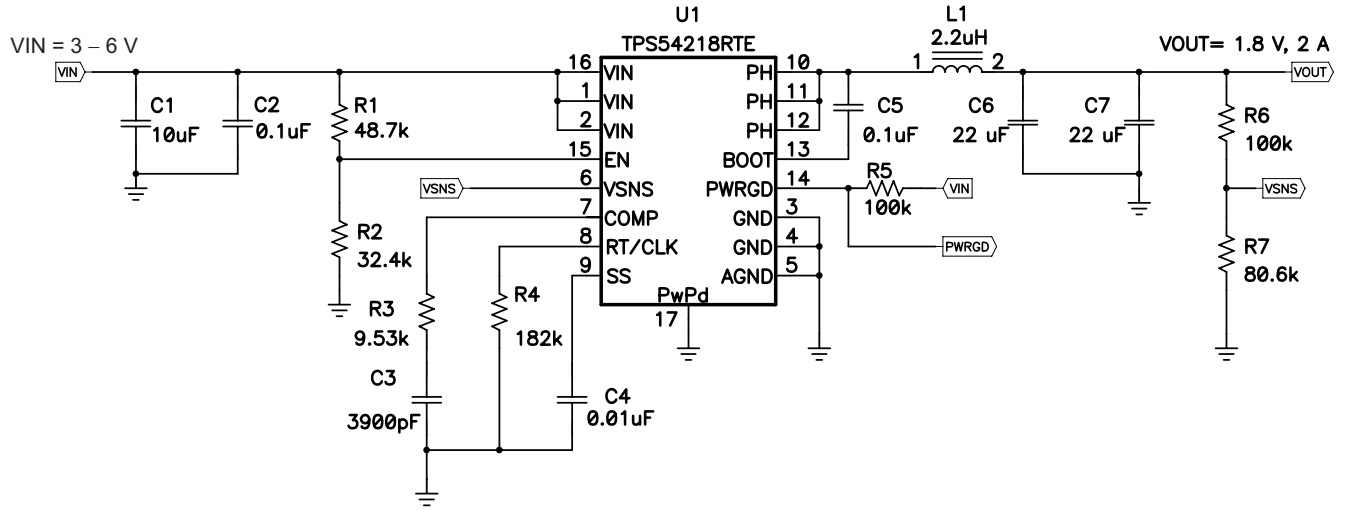


Figure 33. High Frequency, 1.8 V Output Power Supply Design with Adjusted UVLO

OUTPUT INDUCTOR SELECTION

The inductor selected works for the entire TPS54218 input voltage range. To calculate the value of the output inductor, use Equation 18. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

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For this design example, use K_{IND} = 0.3 and the inductor value is calculated to be 2.10 µH. For this design, a nearest standard value was chosen: 2.2 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 20 and Equation 21.

For this design, the RMS inductor current is 2 A and the peak inductor current is 2.3 A. The chosen inductor is a Coilcraft XPL7030-222ML_. It has a RMS current rating of 9.7 A and a saturation current rating of 16 A. The current ratings for this exceed the requirement, but the inductor was chosen for small physical size and low series resistance for high efficiency.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L1 = \frac{V_{IN}max - V_{OUT}}{I_{OUT} \times K_{ind}} \times \frac{V_{OUT}}{V_{IN}max \times fsw} \tag{18}$$

$$I_{ripple} = \frac{V_{IN}max - V_{OUT}}{L1} \times \frac{V_{OUT}}{V_{IN}max \times fsw} \tag{19}$$

$$I_{Lrms} = \sqrt{{I_{OUT}}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN}max - V_{OUT})}{V_{IN}max \times L1 \times fsw} \right)^2} \tag{20}$$

$$I_{Lpeak} = I_{OUT} + \frac{I_{ripple}}{2} \tag{21}$$

OUTPUT CAPACITOR

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 22 shows the necessary minimum output capacitance.

For this example, the transient load response is specified as a 3% change in V_{OUT} for a load step from 1A (50% load) to 2A (100%). For this example, ΔI_{OUT} = 2-1 = 1 A and ΔV_{OUT} = 0.03 × 1.8 = 0.054 V. Using these numbers gives a minimum capacitance of 37 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 23 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, V_{ripple} is the maximum allowable output voltage ripple, and I_{ripple} is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 23 yields 2.18 nF.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{fsw \times \Delta V_{OUT}} \tag{22}$$

$$C_{OUT} > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{Oripple}}{I_{ripple}}}$$

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Where ΔI_{OUT} is the change in output current, Fsw is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. (23)

Equation 24 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 24 indicates the ESR should be less than 57 mΩ. In this case, the ESR of the ceramic capacitor is much less than 57 mΩ.

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, two 22 µF 10 V X5R ceramic capacitors with 3 mΩ of ESR are used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 25 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 25 yields 151mA.

$$R_{ESR} < \frac{V_{Oripple}}{I_{ripple}} \tag{24}$$

$$Icorms = \frac{V_{OUT} \times (V_{IN}max - V_{OUT})}{\sqrt{12} \times V_{IN}max \times L1 \times fsw} \tag{25}$$

INPUT CAPACITOR

The TPS54218 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54218. The input ripple current can be calculated using Equation 26.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 10 V voltage rating is required to support the maximum input voltage. For this example, one 10 µF and one 0.1 µF 10 V capacitors in parallel have been selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 27. Using the design example values, I_{OUT}max = 2 A, C_{IN} = 10 µF, Fsw = 1 MHz, yields an input voltage ripple of 34 mV and a rms input ripple current of 0.98 A.

$$Icirms = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}min} \times \frac{(V_{IN}min - V_{OUT})}{V_{IN}min}} \tag{26}$$

$$\Delta V_{IN} = \frac{I_{OUT}max \times 0.25}{C_{IN} \times fsw} \tag{27}$$

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SLOW START CAPACITOR

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54218 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow start capacitor value can be calculated using Equation 28. For the example circuit, the slow start time is not too critical since the output capacitor value is 44 µF which does not require much current to charge to 1.8 V. The example circuit has the slow start time set to an arbitrary value of 4ms which requires a 10 nF capacitor. In TPS54218, Iss is 2 µA and Vref is 0.8 V.

$$C_{SS}(nF) = \frac{T_{SS}(mS) \times I_{SS}(\mu A)}{V_{ref}(V)} \quad (28)$$

BOOTSTRAP CAPACITOR SELECTION

A 0.1 µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

UNDERVOLTAGE LOCK OUT SET POINT

The Undervoltage Lock Out (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54218. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 3.1 V (V_{START}). After the regulator starts switching, it should continue to do so until the input voltage falls below 2.8 V (V_{STOP}).

The programmable UVLO and enable voltages are set using a resistor divider between Vin and ground to the EN pin. Equation 29 and Equation 30 can be used to calculate the resistance values necessary. From Equation 29 and Equation 30, a 48.7 kΩ between Vin and EN and a 32.4 kΩ between EN and ground are required to produce the 3.1 and 2.8 volt start and stop voltages.

$$R1 = \frac{0.944 \cdot V_{START} - V_{STOP}}{2.59 \times 10^{-6}} \quad (29)$$

$$R2 = \frac{1.18 \cdot R1}{V_{STOP} - 1.18 + R1 \cdot 3.2 \times 10^{-6}} \quad (30)$$

OUTPUT VOLTAGE AND FEEDBACK RESISTORS SELECTION

For the example design, 100 kΩ was selected for R6. Using Equation 31, R7 is calculated as 80 kΩ. The nearest standard 1% resistor is 80.5 kΩ.

$$R7 = \frac{V_{ref}}{V_{OUT} - V_{ref}} R6 \quad (31)$$

Due to the internal design of the TPS54218, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 32

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$$V_{OUT}min = \left(Ontimemin \times F_S max \times \left(V_{IN}max - \left(I_{OUT}min \times \left(2 \times RDS\right)\right)\right)\right) - \left(I_{OUT}min \times \left(R_L + R_{DS}\right)\right)$$

Where:

V_{OUT}min = minimum achievable output voltage

Ontimemin = minimum controllable on-time (60 ns typical. 110 nsec no load)

$F_S$max = maximum switching frequency including tolerance

V_{IN}max = maximum input voltage

I_{OUT}min = minimum load current

R_{DS} = minimum high side MOSFET on resistance (30 - 44 mΩ)

R_L = series resistance of output inductor (32)

There is also a maximum achievable output voltage which is limited by the minimum off time. The maximum output voltage is given by Equation 33

$$V_{OUT}max = \left(1 - \left(Offtimemax \times F_S max\right)\right) \times \left(V_{IN}min - \left(I_{OUT}max \times \left(2 \times R_{DS}\right)\right)\right) - I_{OUT}max \times \left(R_L + R_{DS}\right)$$

Where:

V_{OUT}max = maximum achievable output voltage

Offtimeman = maximum off time (60 nsec typical)

$F_S$max = maximum switching frequency including tolerance

V_{IN}min = minimum input voltage

I_{OUT}max = maximum load current

R_{DS} = maximum high side MOSFET on resistance (60 - 70 mΩ)

R_L = series resistance of output inductor (33)

COMPENSATION

There are several industry techniques used to compensate DC/DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54218. Since the slope compensation is ignored, the actual cross over frequency is usually lower than the cross over frequency used in the calculations. Use SwitcherPro software for a more accurate design.

To get started, the modulator pole, fpmod, and the esr zero, fz1 must be calculated using Equation 34 and Equation 12. For C_{OUT}, derating the capacitor is not needed as the 1.8 V output is a small percentage of the 10 V capacitor rating. If the output is a high percentage of the capacitor rating, use the capacitor manufacturer information to derate the capacitor value. Use Equation 36 and Equation 37 to estimate a starting point for the crossover frequency, fc. For the example design, fpmod is 4.02 kHz and fpmod is 1206 kHz. Equation 36 is the geometric mean of the modulator pole and the esr zero and Equation 37 is the mean of modulator pole and the switching frequency. Equation 36 yields 69.6 kHz and Equation 37 gives 44.8 kHz. Use the lower value of Equation 36 or Equation 37 as the maximum crossover frequency. For this example, fc is 45 kHz. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole (if needed).

$$fp\ mod = \frac{I_{OUT}\,max}{2\pi \times V_{OUT} \times C_{OUT}} \quad (34)$$

$$fz\ mod = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (35)$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \quad (36)$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \quad (37)$$

The compensation design takes the following steps:

1. Set up the anticipated cross-over frequency. Use Equation 38 to calculate the compensation network's resistor value. In this example, the anticipated cross-over frequency (fc) is 45 kHz. The power stage gain (gm_{ps}) is 13 A/V and the error amplifier gain (gm_{ea}) is 225 A/V.

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$$R3 = \frac{2\pi \times fc \times V_{OUT} \times C_{OUT}}{gm \times V_{ref} \times V_{Igm}} \quad (38)$$

2. Place compensation zero at the pole formed by the load resistor and the output capacitor. The compensation network's capacitor can be calculated from Equation 39.

$$C3 = \frac{R_{OUT} \times C_{OUT}}{R3} \quad (39)$$

3. An additional pole can be added to attenuate high frequency noise. In this application, it is not necessary to add it.

From the procedures above, the compensation network includes a 9.53 kΩ resistor and a 3900 pF capacitor.

APPLICATION CURVES

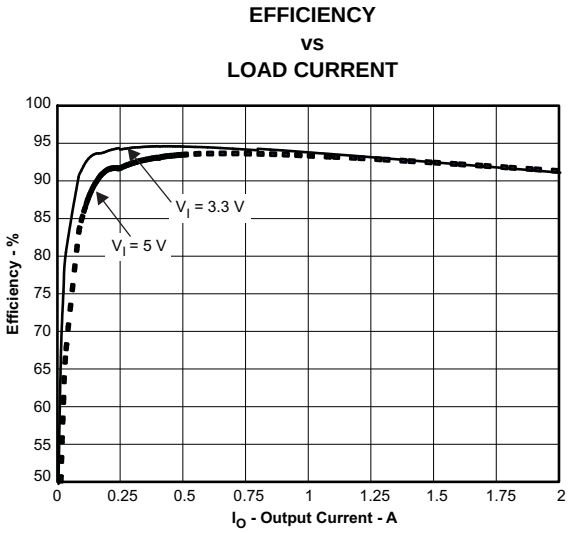


Figure 34.

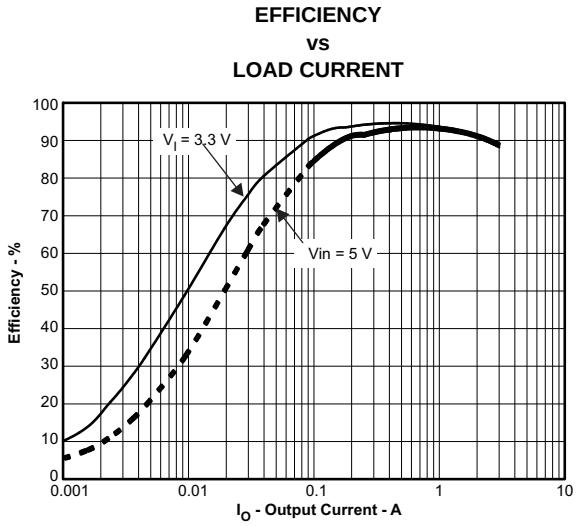


Figure 35.

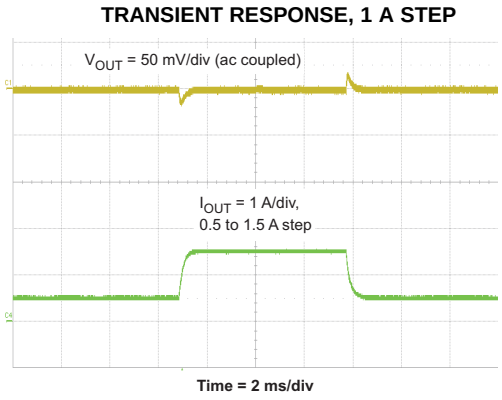


Figure 36.

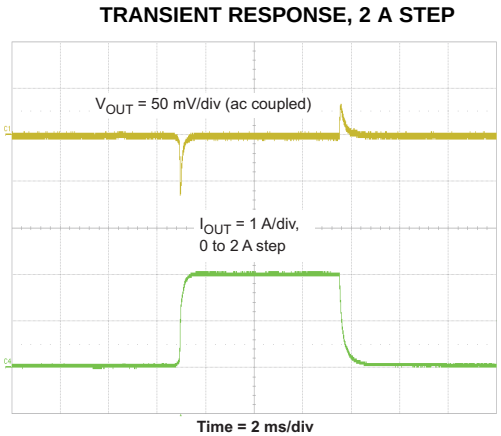


Figure 37.

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POWER UP V_{OUT}, VIN

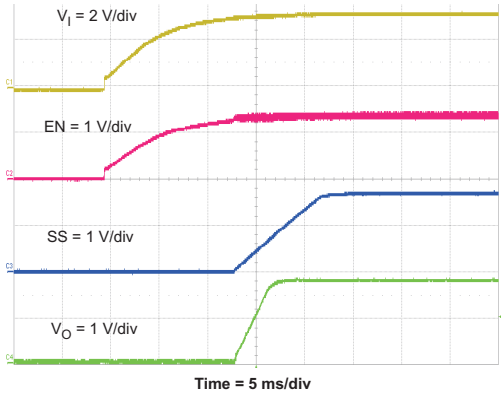


Figure 38.

POWER DOWN V_{OUT}, VIN

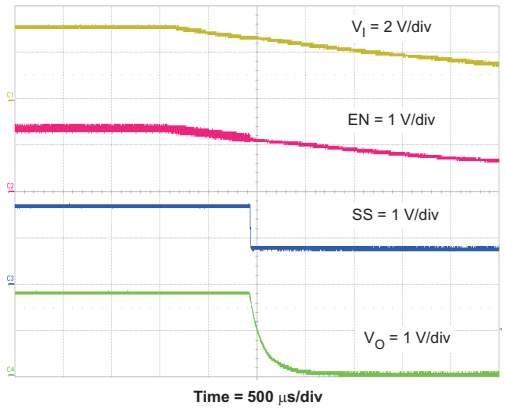


Figure 39.

POWER UP V_{OUT}, EN

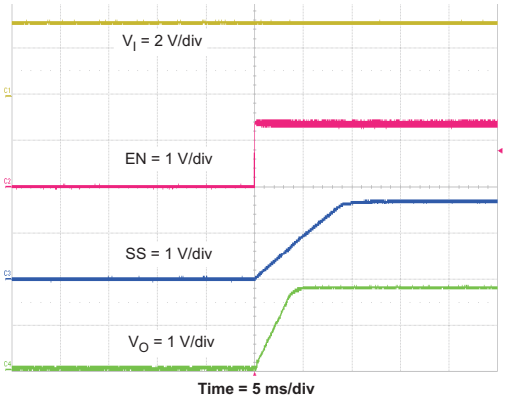


Figure 40.

POWER DOWN V_{OUT}, EN

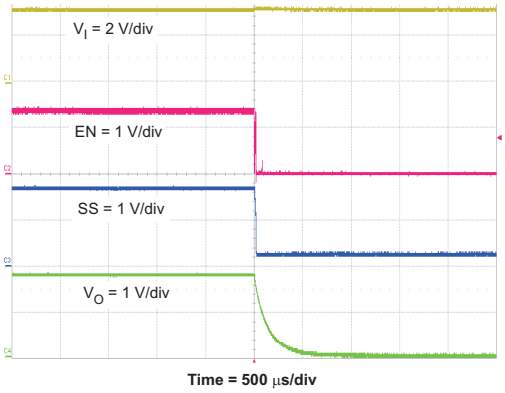


Figure 41.

OUTPUT RIPPLE, 0 A

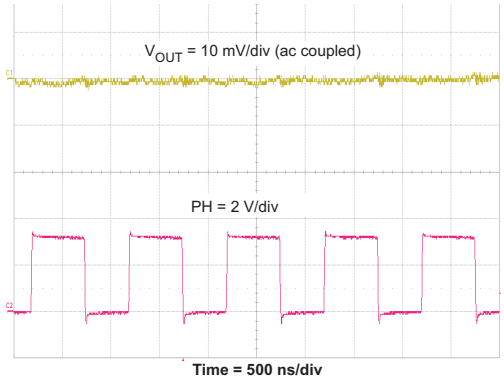


Figure 42.

OUTPUT RIPPLE, 2 A

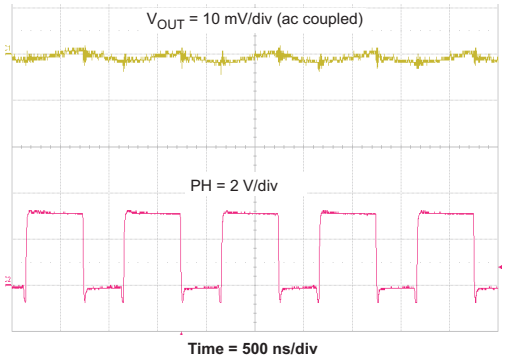


Figure 43.

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INPUT RIPPLE, 0 A

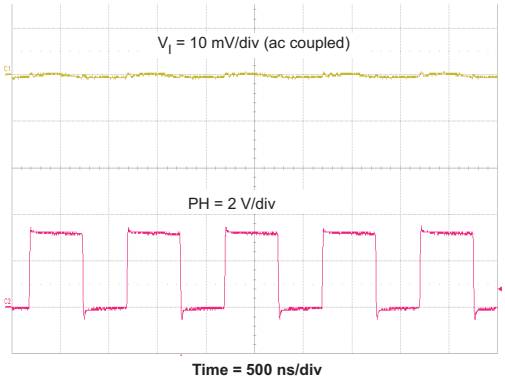


Figure 44.

INPUT RIPPLE, 2 A

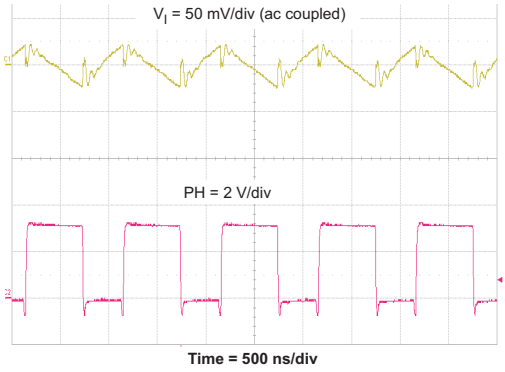


Figure 45.

CLOSED LOOP RESPONSE, VIN (3.3 V), 2 A

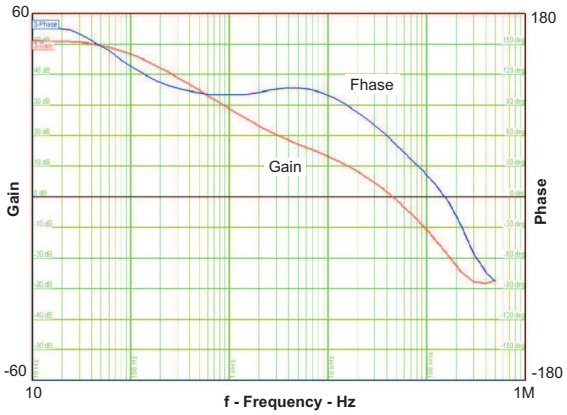


Figure 46.

LOAD REGULATION VS LOAD CURRENT

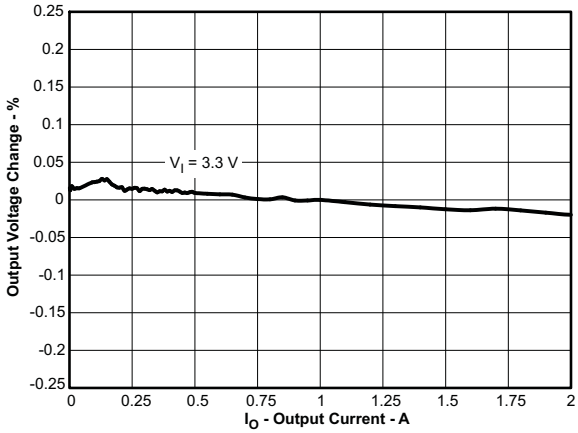


Figure 47.

LOAD REGULATION VS LOAD CURRENT

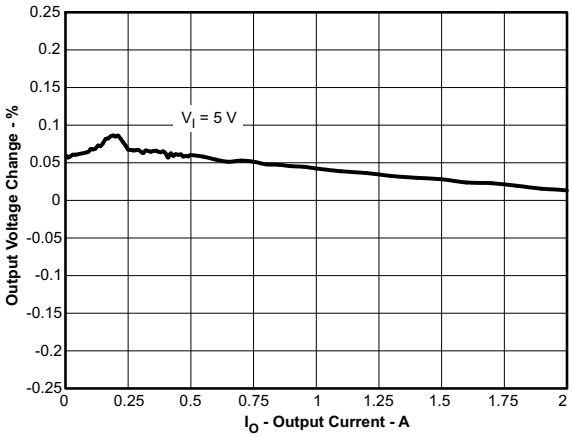


Figure 48.

REGULATION VS INPUT VOLTAGE

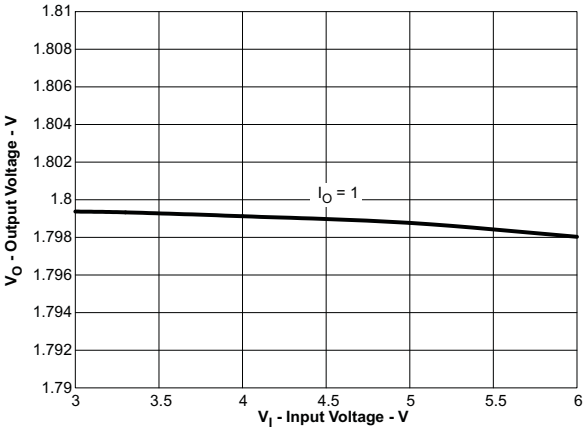


Figure 49.

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POWER DISSIPATION ESTIMATE

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. The power dissipation of the IC (Ptot) includes conduction loss (Pcon), dead time loss (Pd), switching loss (Psw), gate drive loss (Pgd) and supply current loss (Pq).

$$Pcon = I_{OUT}^{2} \times R_{DS(on)}$$

$$Pd = \mathit{f}sw \times I_{OUT} \times 0.7 \times 60 \times 10^{-9}$$

$$Psw = 2 \times V_{IN}^{2} \times \mathit{f}sw \times I_{OUT} \times 0.25 \times 10^{-9}$$

$$Pgd = 2 \times V_{IN} \times 3 \times 10^{-9} \times \mathit{f}sw$$

$$Pq = 350 \times 10^{-6} \times V_{IN}$$

Where:

I_{OUT} is the output current (A).
$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
V_{OUT} is the output voltage (V).
V_{IN} is the input voltage (V).
$\mathit{f}sw$ is the switching frequency (Hz).

So

$$Ptot = Pcon + Pd + Psw + Pgd + Pq$$

For given T_A,

$$T_J = T_A + Rth \times Ptot$$

For given T_J max = 150°C

$$T_A max = T_J max - Rth \times Ptot$$

Where:

Ptot is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
Rth is the thermal resistance of the package (°C/W).
$T_J$max is maximum junction temperature (°C).
$T_A$max is maximum ambient temperature (°C).

There are additional power losses in the regulator circuit due to the inductor ac and dc losses and trace resistance that impact the overall efficiency of the regulator. As an example, the maximum ambient temperature versus power dissipation for the EVM is shown in Figure 51.

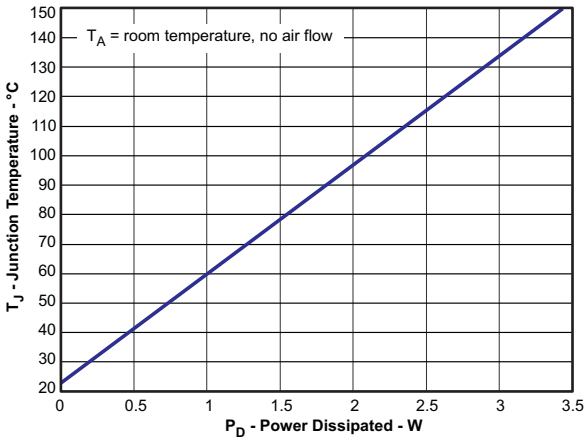


Figure 50. Junction Temperature vs IC Power Dissipation

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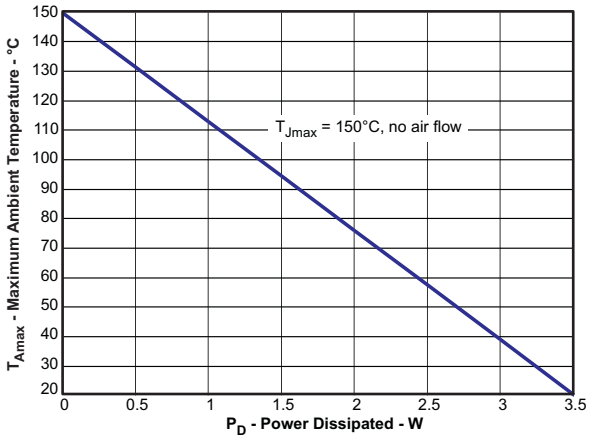


Figure 51. Maximum Ambient Temperature vs IC power Dissipation

LAYOUT

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 52 for a PCB layout example. The GND pins and AGND pin should be tied directly to the power pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors. For operation at full rated load, the top side ground area along with any additional internal ground planes must provide adequate heat dissipating area.

Locate the input bypass capacitor as close to the IC as possible. The PH pin should be routed to the output inductor. Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It is possible to obtain acceptable performance with alternate PCB layouts; however, this layout has been shown to produce good results and is meant as a guideline.

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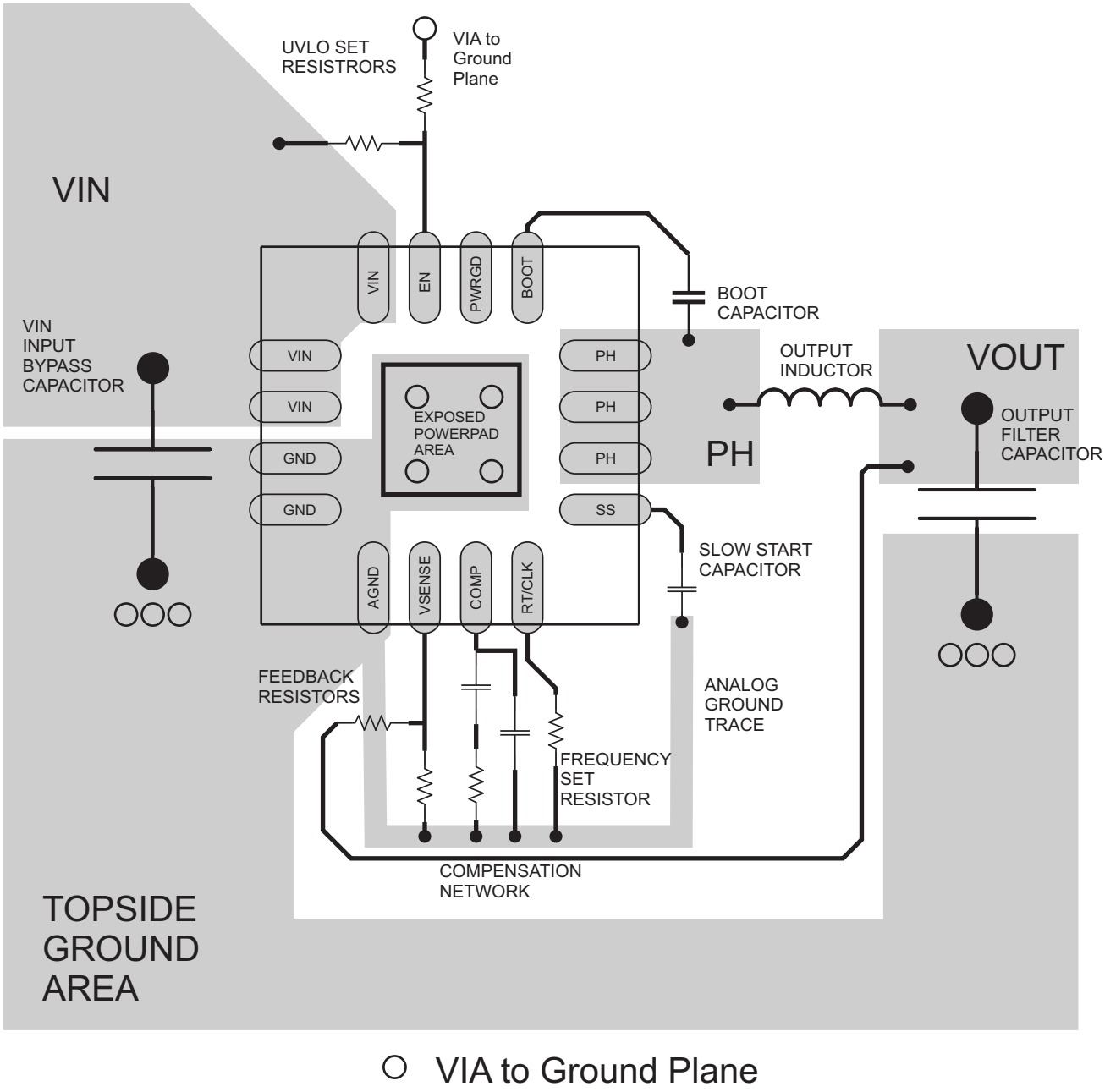


Figure 52. PCB Layout Example

REVISION HISTORY

Changes from Original (September 2009) to Revision A	Page
• Added "Instantaneous peak current" to the Current Limit in the Electrical Characteristics table	3

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS54218RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS54218RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

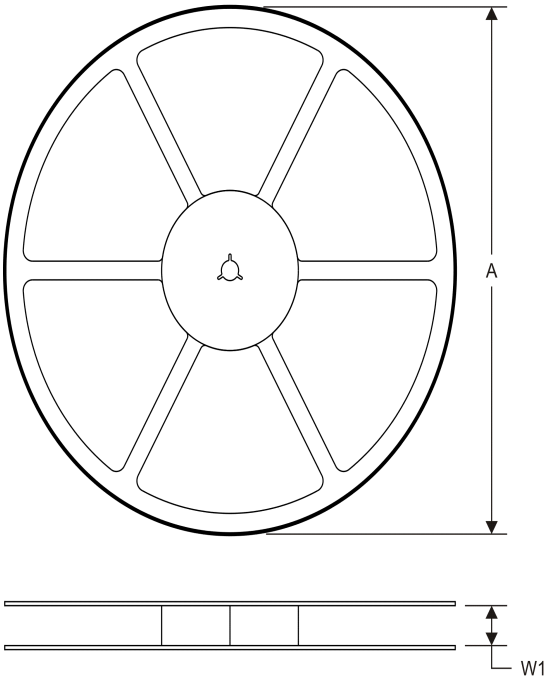
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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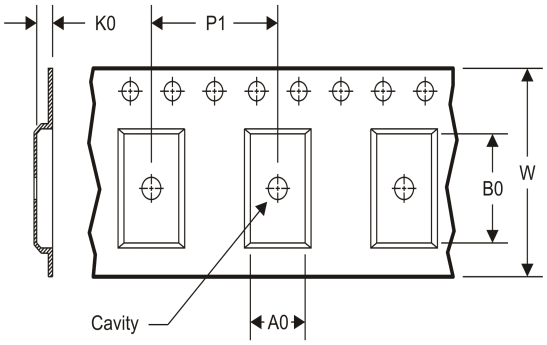
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



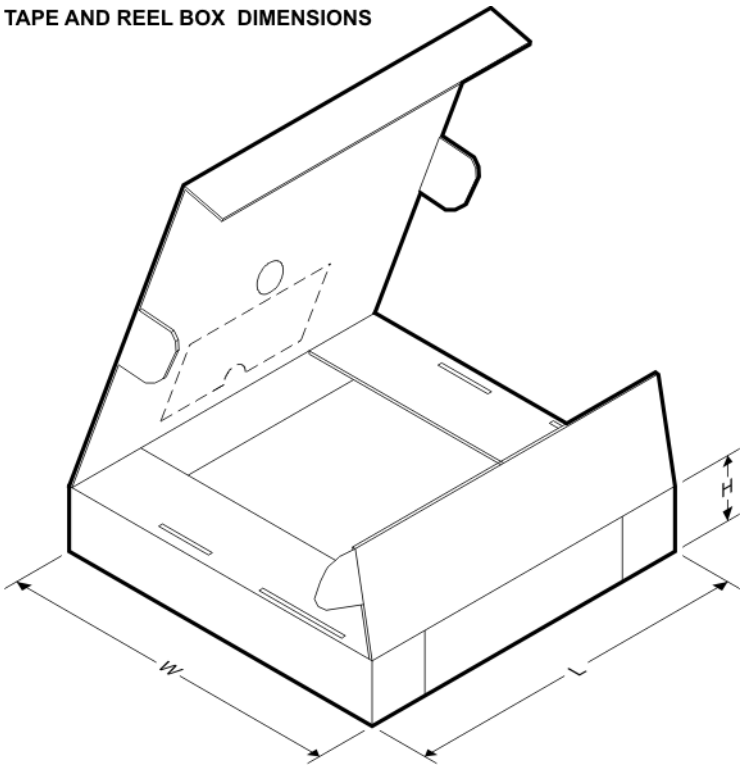
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54218RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54218RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54218RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

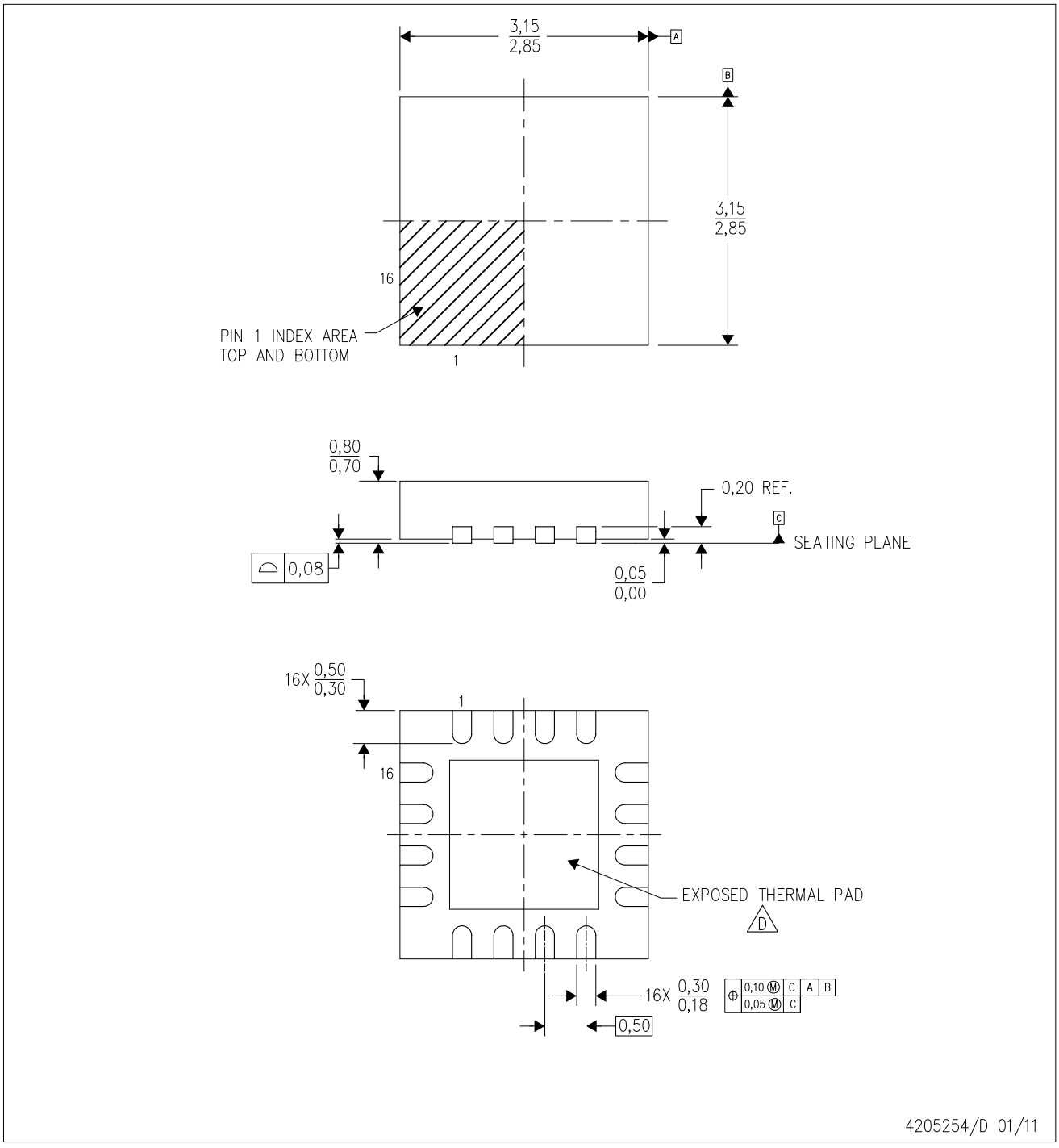
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54218RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS54218RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS54218RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

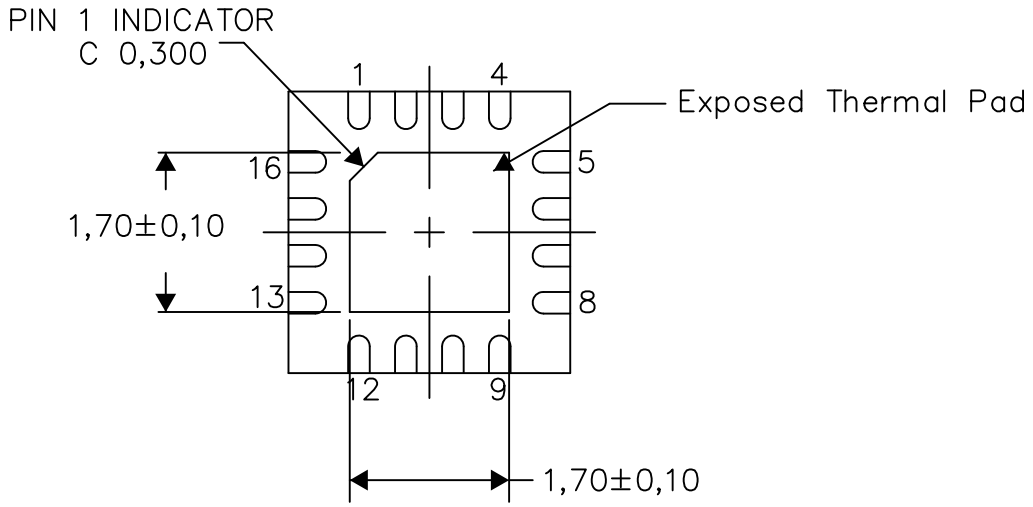
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



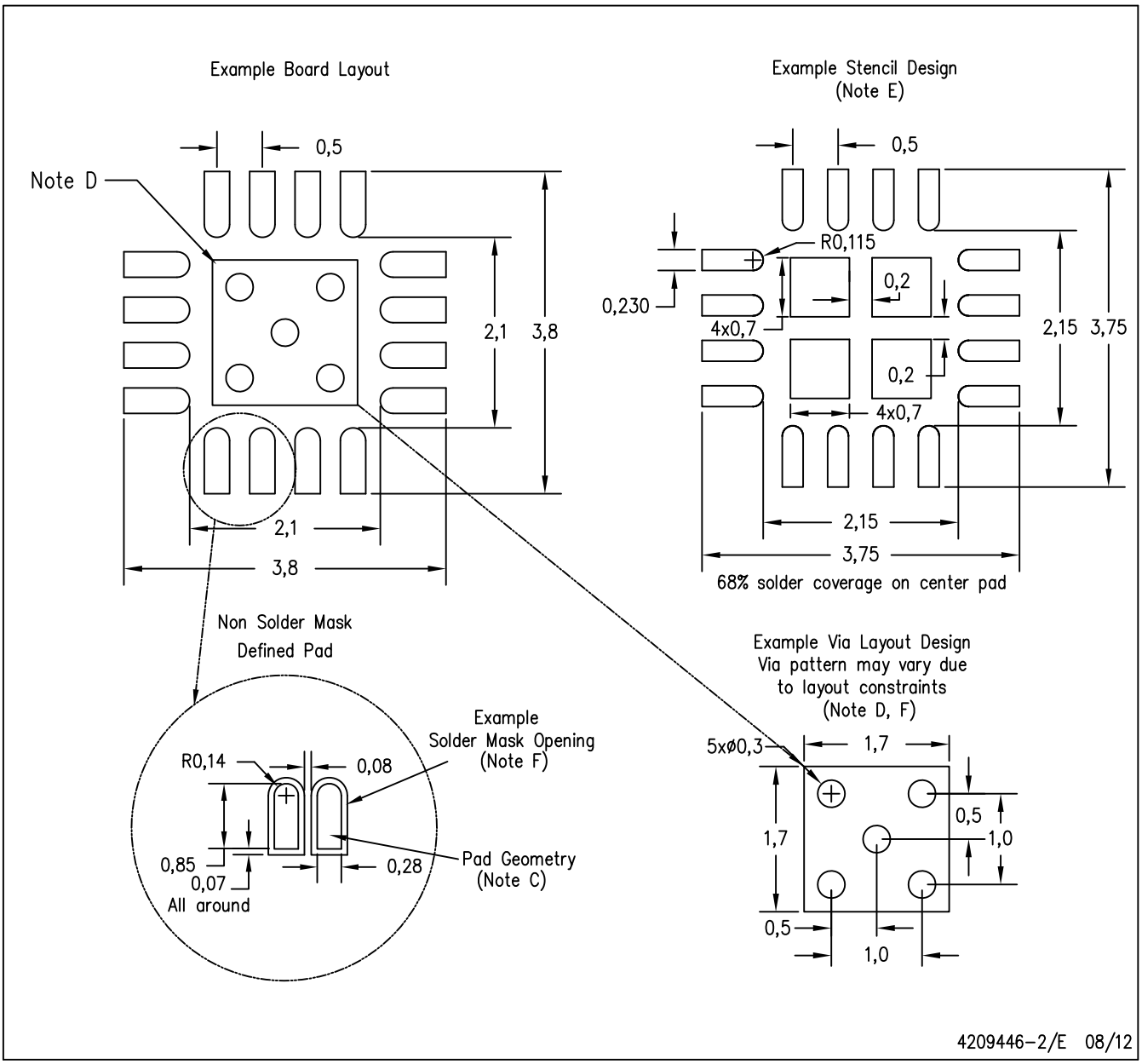
Bottom View

Exposed Thermal Pad Dimensions

4206446–3/J 05/12

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

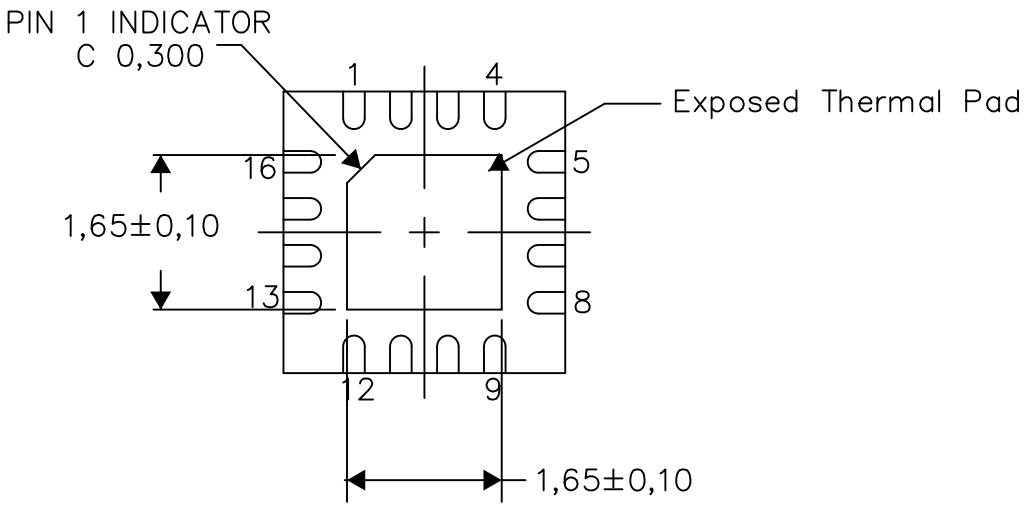
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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NOTE: A. All linear dimensions are in millimeters

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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