



ACE7333C

28V, 3A, 500KHz Synchronous Step-Down DC/DC Converter

Description

The ACE7333C is a fully integrated synchronous rectified step-down converter that provides wide 3.8V to 28V input voltage range and 3A continuous load current capability. The ACE7333C can operate at PFM mode to achieve high efficiency and reduce power loss at light load. In shutdown mode, the Max supply current is about 3 μ A.

The ACE7333C protection function includes cycle-by-cycle current limit, UVLO and thermal shutdown. Besides, internal soft-start prevents inrush current at fast power-on. This device uses slope compensated current mode control which provides fast load transient response. Internal loop compensation function reduces the external compensator components and simplifies the design process.

The ACE7333C requires a minimum number of readily available standard external components and is available in ESOP-8 (Exposed Pad) package and provides good thermal conductance.

Features

- Wide Input Voltage Range: 3.8V to 28V
- 3A Output Current
- 0.8V Reference Voltage
- Low RDS(ON) Integrated Power MOSFET (150/90m Ω)
- 3 μ A(Max) Shutdown Current
- Integrated internal compensation
- High Efficiency at Light Load
- Internal 1ms Soft-Start
- Cycle-by-Cycle Current Limit
- Over-Temperature Protection with Auto Recovery
- Under Voltage Lockout(UVLO)
- Hiccup Short Circuit Protection
- Available in ESOP8 Exposed Pad Package
- RoHS Compliant

Application

- Distributed Power System
- Flat Panel Television and Monitors
- STB (Set-Top-Box)
- Networking, XDSL Modem

Recommended Work Conditions

Item	Min	Max.	Unit
Supply Voltage VIN	3.8	28	V
Ambient Temperature	-40	85	$^{\circ}$ C



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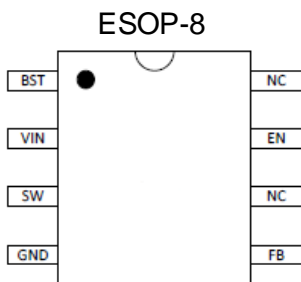
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Absolute Maximum Ratings

Parameter	Value
Supply Voltage V_{IN}	-0.3V to 30V
Switch Node Voltage V_{SW}	-0.3V to ($V_{IN}+0.5V$)
Boost Voltage V_{BST}	$V_{SW}-0.3V$ to $V_{SW}+5V$
Enable Voltage V_{EN}	-0.3V to 12V
The others Pins	-0.3V to 6V
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10s)	300°C

Note: Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.

Packaging Type

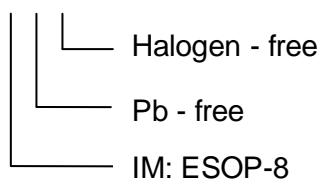


Pinout Description

Pin NO.	Name	Description
1	BST	High side power transistor gate drive boost input.
2	VIN	Power input. Bypass with a 22uF ceramic capacitor to GND.
3	SW	Power switching node to connect inductor.
4	GND	Ground.
5	FB	Feedback input with reference voltage set to 0.8V.
6	NC	No connection
7	EN	Enable input. Set this pin to high level to enable the part, low level to disable.
8	NC	No connection

Ordering information

ACE7333C XX+ H

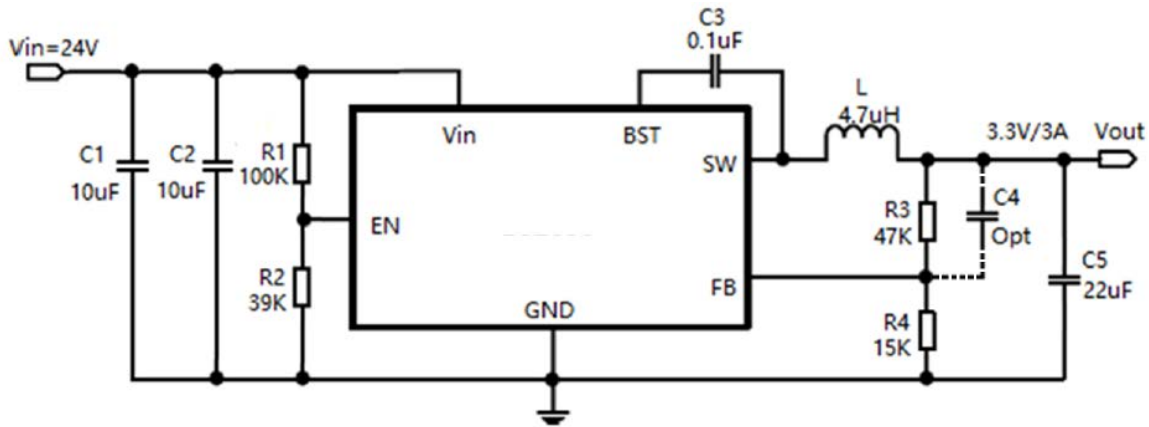




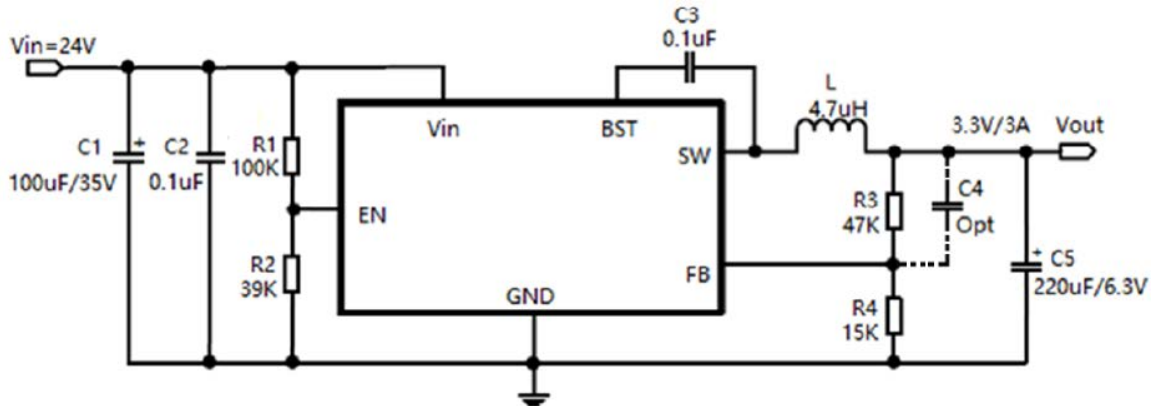
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Typical Application



C_{IN} & C_{OUT} use Ceramic Capacitors Application Circuit



C_{IN} & C_{OUT} use Electrolytic Capacitors Application Circuit

Note: If the input voltage is below 12V, R1 can be set to 0K and R2 can be removed.

$V_{IN}=24V$, the recommended BOM list is shows as below.

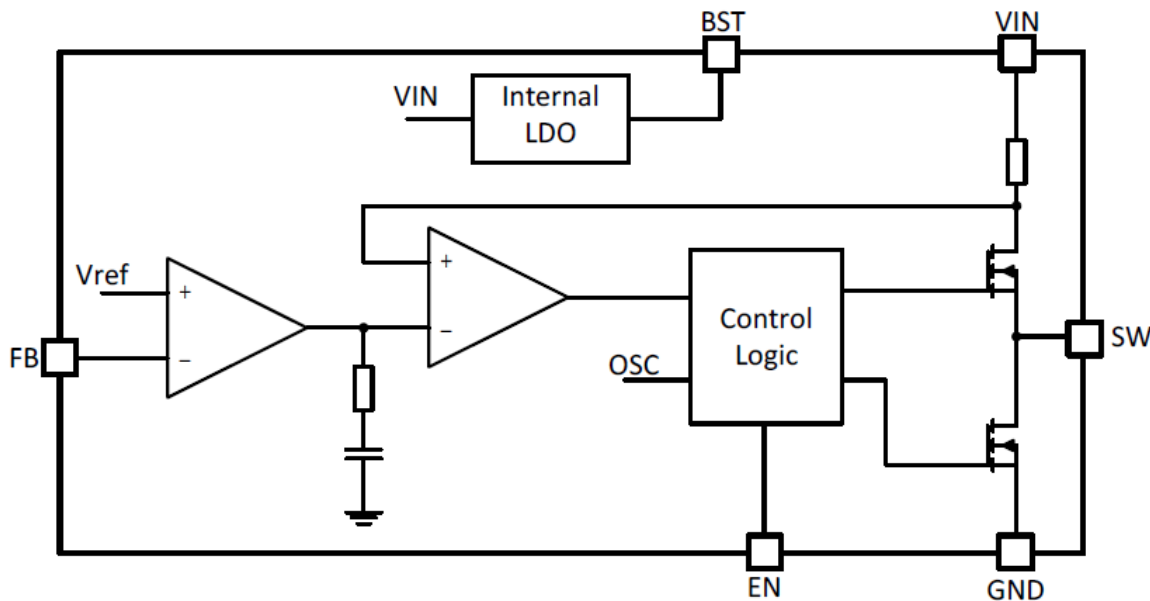
V_{OUT}	C1	C2	L	R3	R4	C5
5V	10uF/MLCC	10uF/MLCC	3.3uH-6.8uH	68K	13K	22uF/MLCC
3.3V			2.2uH-4.7uH	47K	15K	
2.8V			2.2uH-4.7uH	30K	12K	
2.5V			2.2uH-4.7uH	39K	18K	
1.8			2.2uH-4.7uH	15K	12K	
1.2V			2.2uH-3.3uH	7.5K	15K	
5V	100uF/35V/ECL	0.1uF/MLCC	3.3uH-6.8uH	68K	13K	220uF/6.3V/ECL
3.3V			2.2uH-4.7uH	47K	15K	
2.8V			2.2uH-4.7uH	30K	12K	
2.5V			2.2uH-4.7uH	39K	18K	
1.8			2.2uH-3.3uH	15K	12K	
1.2V			2.2uH-3.3uH	7.5K	15K	



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Block Diagram



Electrical Characteristics

($V_{IN} = 12V$, $T_A = 25^\circ C$, unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		3.8		28	V
UVLO Threshold	Vin Rising		3.8		V
UVLO Hypothesis	Vin Falling		200		mV
Supply Current in Operation	$V_{EN} = 5V$, $V_{FB} = 1V$		150		uA
Supply Current in Shutdown	$V_{EN} = 0V$		1		uA
Regulated Feedback Voltage	$3.8V \leq V_{IN} \leq 30V$	0.784	0.8	0.816	V
High-side Switch On Resistance	$V_{BST-SW} = 5V$		150		mΩ
Low-side Switch On Resistance	$V_{IN} = 5V$		90		mΩ
High-side Switch Leakage Current	$V_{EN} = 0V$, $V_{SW} = 0V$		0.1	1	uA
Upper Switch Current Limit	Minimum Duty Cycle		5		A
Oscillation Frequency			500		KHz
Maximum Duty Cycle			93		%
Minimum On Time			100		ns
EN Input Voltage "H"		1.5			V
EN Input Voltage "L"				0.6	V
Thermal Shutdown			160		°C

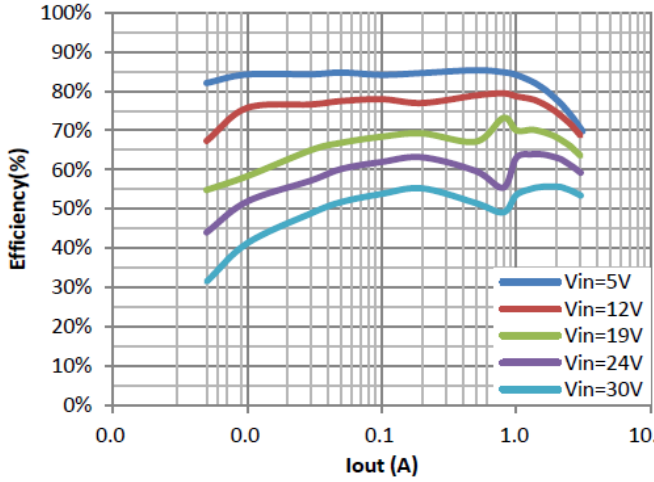


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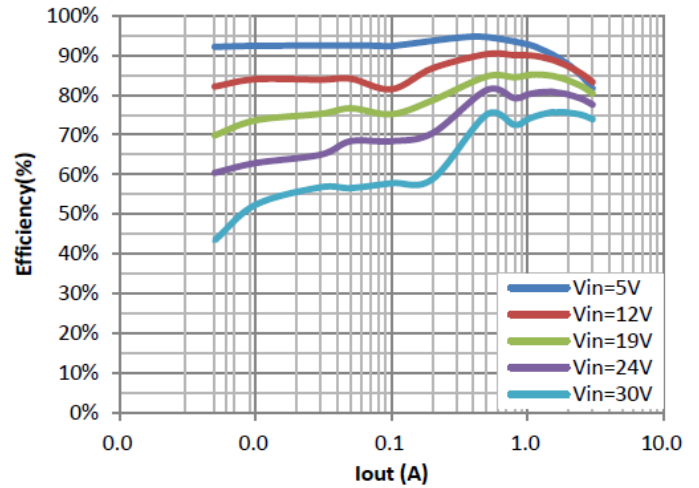
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Typical Performance Characteristics

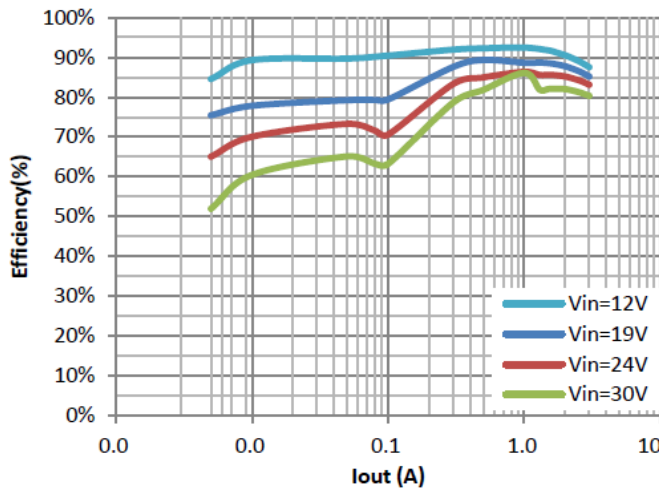
Efficiency vs. I_{out}
V_{out}=1.2V



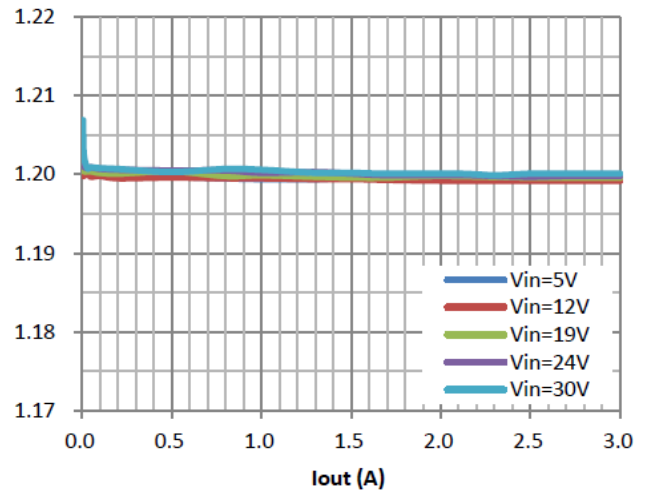
Efficiency vs. I_{out}
V_{out}=3.3V



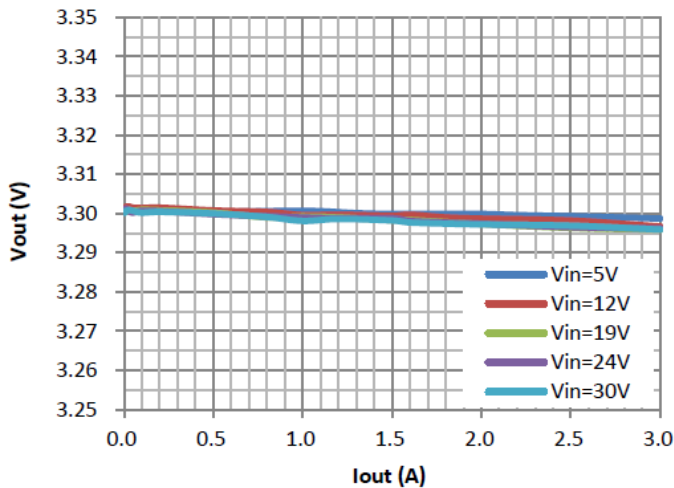
Efficiency vs. I_{out}
V_{out}=5.0V



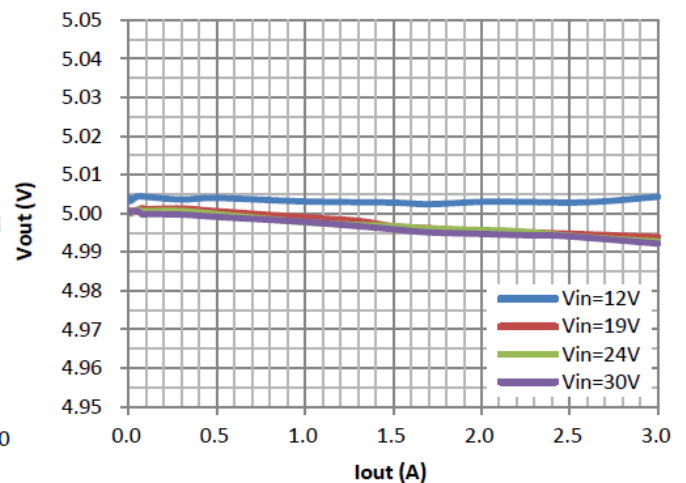
V_{out} vs. I_{out}
V_{out}=1.2V



V_{out} vs. I_{out}
V_{out}=3.3V



V_{out} vs. I_{out}
V_{out}=5.0V





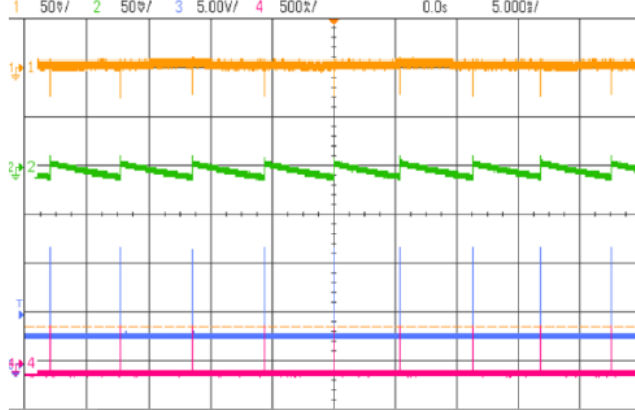
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Steady State Waveform

Vin=12V, Vout=3.3V, Cin=Cout=10uF*2, L=4.7uH, Iout=0A

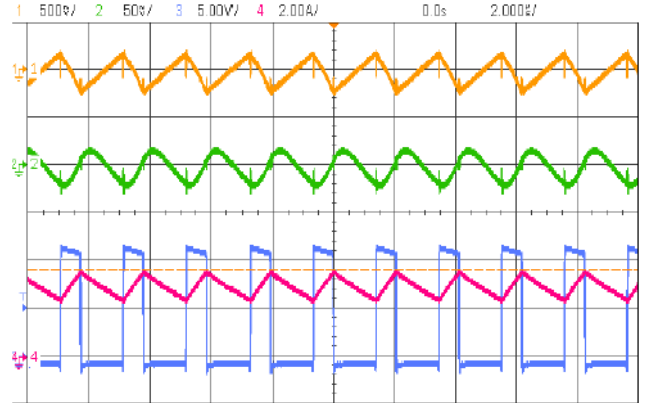
Ch1—Vin, Ch2—Vout, Ch3—V_{SW}, Ch4—I_{SW}



Steady State Waveform

Vin=12V, Vout=3.3V, Cin=Cout=10uF*2, L=4.7uH, Iout=3A

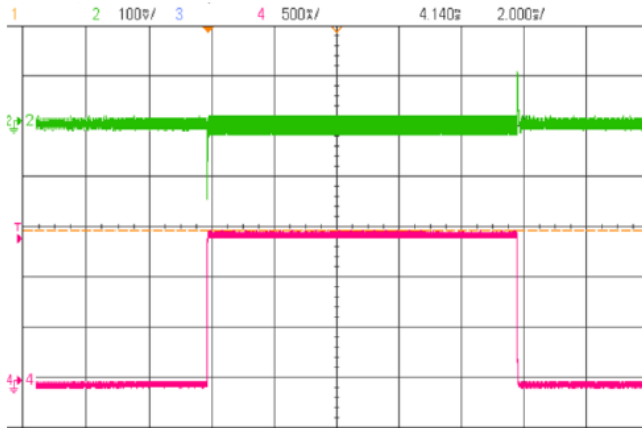
Ch1—Vin, Ch2—Vout, Ch3—V_{SW}, Ch4—I_{SW}



Load Transient

Vin=12V, Vout=3.3V, Iout=0.01~1.5A

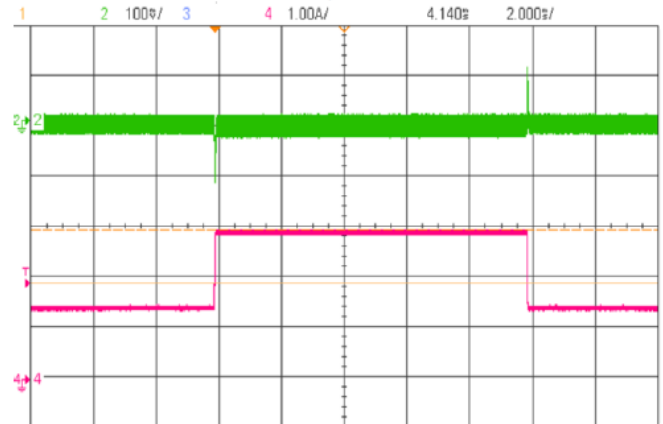
Ch2—Vout, Ch4—I_L



Load Transient

Vin=12V, Vout=3.3V, Iout=1.5~3A

Ch2—Vout, Ch4—I_L





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Functional Descriptions

Loop Operation

The ACE7333C is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 3A of output current, integrated with a 150/90mΩ synchronous MOSFET pair, eliminating the need for external diode. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

Internal Soft-Start

The soft-start is important for many applications because it eliminates power-up initialization problems. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

Over-Current-Protection and Hiccup

The ACE7333C has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Under-Voltage (UV) threshold (typically 300mV) to trigger a UV event, the ACE7333C enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short-circuited to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The ACE7333C exits hiccup mode once the overcurrent condition is removed.

Light Load Operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFETs, power is lost due to the finite R_{DS(ON)}s of the MOSFETs and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. ACE7333C employs a proprietary control scheme that improves efficiency in this situation by enabling the device into a power save mode during light load, thereby extending the range of high efficiency operation.

Startup and Shutdown

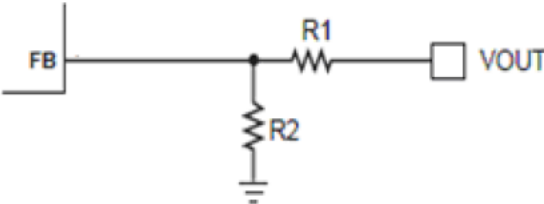
If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.



Applications Information

Setting Output Voltages

The external resistor divider is used to set the output voltage. The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. The recommended value of the R1 should be below 100K to provide optimal transient response. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$


Selecting the Inductor

Use a 2.2µH-to-6.8µH inductor with a DC current rating of at least 25% higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2} \right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.



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For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

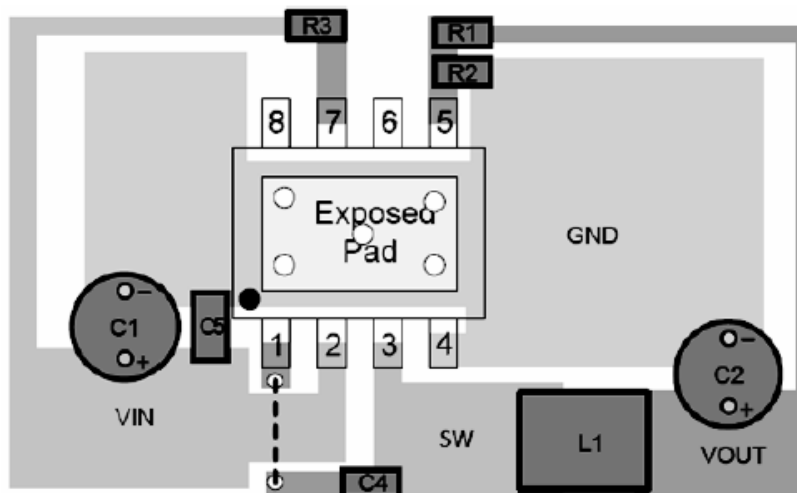
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The ACE7333C can be optimized for a wide range of capacitance and ESR values.

PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (SW).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.



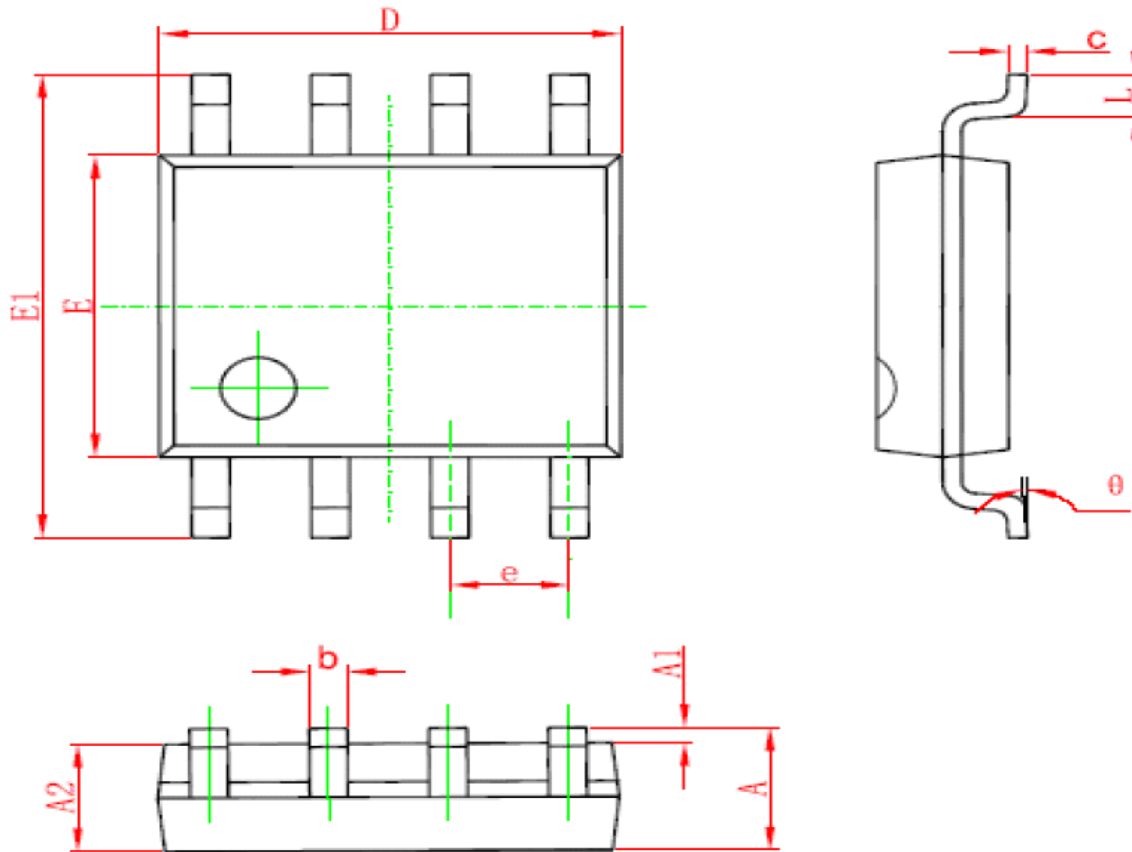


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Packing Information

ESOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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