SONY

CXD1198AQ

CD-ROM Subcode Decoder

For the availability of this product, please contact the sales office.

Description

The CXD1198AQ is a CD-ROM subcode decoder LSI.

Features

- Real time error correction of subcodes
- Connection possible with DRAM up to 1 MB as buffer memory
- Automatic generation of sync patterns
- Error pointer buffering function (separated mode, mixed mode)
- 4 MB/s maximum rate for transferring data with SCSI control LSI

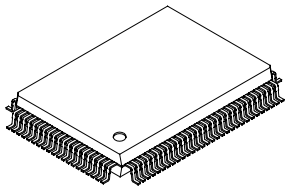
Applications

CD-ROM drives

Structure

Silicon gate CMOS IC

100 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	–0.5 to +7.0	V
• Input voltage	V_I	–0.5 to V_{DD} +0.5	V
• Output voltage	V_O	–0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

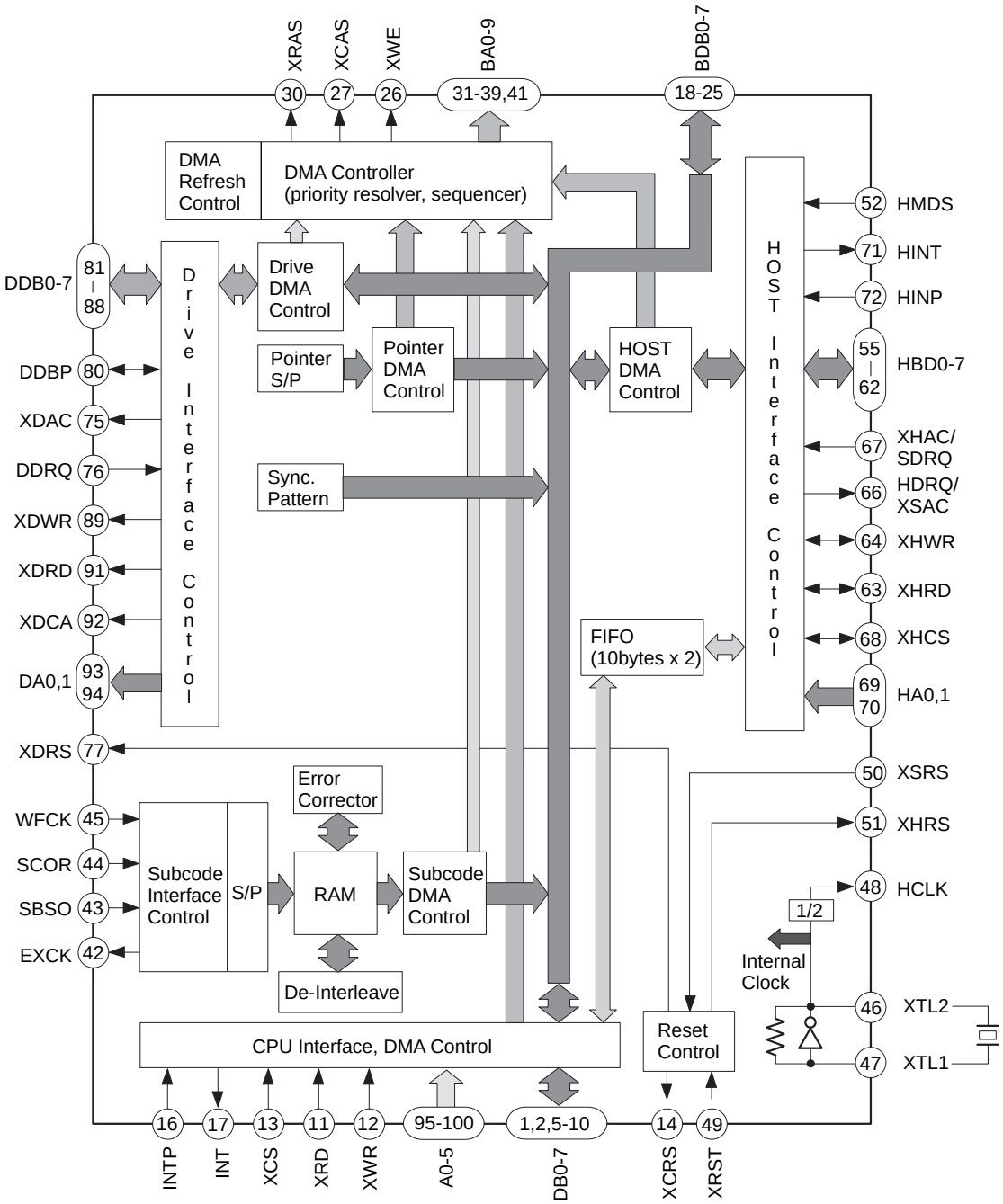
Recommended Operating Conditions

• Supply voltage	V_{DD}	5.0±0.5	V
• Operating temperature	Topr	–20 to +75	°C

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E92632A78-TE

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	DB0	I/O	CPU data bus
2	DB1	I/O	CPU data bus
3	V_{DD}		Power supply (+5 V)
4	V_{SS}		GND
5	DB2	I/O	CPU data bus
6	DB3	I/O	CPU data bus
7	DB4	I/O	CPU data bus
8	DB5	I/O	CPU data bus
9	DB6	I/O	CPU data bus
10	DB7	I/O	CPU data bus
11	XRD	I	Register read strobe negative logic signal in this IC
12	XWR	I	Register write strobe negative logic signal in this IC
13	XCS	I	Chip select signal to this IC
14	XCRS	O	Reset negative logic signal to CPU
15	V_{SS}		GND
16	INTP	I	INT signal polarity control input signal
17	INT	O	Interrupt request signal to CPU
18	BDB0	I/O	Buffer memory data bus
19	BDB1	I/O	Buffer memory data bus
20	BDB2	I/O	Buffer memory data bus
21	BDB3	I/O	Buffer memory data bus
22	BDB4	I/O	Buffer memory data bus
23	BDB5	I/O	Buffer memory data bus
24	BDB6	I/O	Buffer memory data bus
25	BDB7	I/O	Buffer memory data bus
26	XWE	O	Strobe negative logic signal for writing in buffer memory
27	XCAS	O	Strobe negative logic signal for column address in buffer memory
28	V_{DD}		Power supply (+5 V)
29	V_{SS}		GND
30	XRAS	O	Strobe negative logic signal for row address in buffer memory
31	BA0	O	Buffer memory address
32	BA1	O	Buffer memory address
33	BA2	O	Buffer memory address
34	BA3	O	Buffer memory address

Pin No.	Symbol	I/O	Description
35	BA4	O	Buffer memory address
36	BA5	O	Buffer memory address
37	BA6	O	Buffer memory address
38	BA7	O	Buffer memory address
39	BA8	O	Buffer memory address
40	V_{SS}		GND
41	BA9	O	Buffer memory address
42	EXCK	O	Subcode data readout clock output signal to the CXD2500
43	SBSI	I	Subcode data input signal from the CXD2500
44	SBSY	I	Subcode frame sync input signal from the CXD2500
45	WFCK	I	Write frame clock input signal from the CXD2500
46	XTL2	O	Crystal oscillator circuit output
47	XTL1	I	Crystal oscillator circuit input
48	HCLK	O	Crystal 1/2 frequency-divided clock output
49	XRST	I	Reset negative logic input signal
50	XSRS	I	SCSI bus reset negative logic input signal
51	XHRS	O	Reset negative logic output signal to host
52	HMDS	I	Host mode select input signal
53	V_{DD}		Power supply (+5 V)
54	V_{SS}		GND
55	HDB7	I/O	Host data bus
56	HDB6	I/O	Host data bus
57	HDB5	I/O	Host data bus
58	HDB4	I/O	Host data bus
59	HDB3	I/O	Host data bus
60	HDB2	I/O	Host data bus
61	HDB1	I/O	Host data bus
62	HDB0	I/O	Host data bus
63	XHRD	I/O	Data read strobe signal from host or to SCSI control IC
64	XHWR	I/O	Data write strobe signal from host or to SCSI control IC
65	V_{SS}		GND
66	HDRQ /XSAC	O	Data request positive logic signal to host or DMA acknowledge negative logic signal to SCSI control IC
67	XHAC /SDRQ	I	DMA acknowledge negative logic signal from host or data request positive logic signal from SCSI control IC

Pin No.	Symbol	I/O	Description
68	XHCS	I	Chip select input signal from host
69	HA0	I	Host address signal
70	HA1	I	Host address signal
71	HINT	O	Interrupt request signal to host
72	HINP	I	HINT signal polarity control input signal
73	NC1	O	No connection; leave open.
74	NC2	O	No connection; leave open.
75	XDAC	O	DMA acknowledge negative logic signal to the CXD1186BQ
76	DDRQ	I	Data request positive logic signal from the CXD1186BQ
77	XDRS	O	Reset negative logic signal to the CXD1186BQ
78	V_{DD}		Power supply (+5 V)
79	V_{SS}		GND
80	DDBP	I/O	Error pointer bus connected with the CXD1186BQ
81	DDB7	I/O	Data bus connected with the CXD1186BQ
82	DDB6	I/O	Data bus connected with the CXD1186BQ
83	DDB5	I/O	Data bus connected with the CXD1186BQ
84	DDB4	I/O	Data bus connected with the CXD1186BQ
85	DDB3	I/O	Data bus connected with the CXD1186BQ
86	DDB2	I/O	Data bus connected with the CXD1186BQ
87	DDB1	I/O	Data bus connected with the CXD1186BQ
88	DDB0	I/O	Data bus connected with the CXD1186BQ
89	XDWR	O	Host register write strobe negative logic signal to the CXD1186BQ
90	V_{SS}		GND
91	XDRD	O	Host register read strobe negative logic signal to the CXD1186BQ
92	XDCS	O	Chip select negative logic signal for host register read/write to the CXD1186BQ
93	DA1	O	Address signal to the CXD1186BQ
94	DA0	O	Address signal to the CXD1186BQ
95	A5	I	CPU address signal
96	A4	I	CPU address signal
97	A3	I	CPU address signal
98	A2	I	CPU address signal
99	A1	I	CPU address signal
100	A0	I	CPU address signal

Electrical Characteristics

DC characteristics

(V_{DD}=5.0±0.5 V, V_{SS}=0 V, Topr=–20 to +75 °C)

Item			Symbol	Conditions	Min.	Typ.	Max.	Unit
TTL input voltage		High level	V_{IH1}		2.2			V
		Low level	V_{IL1}				0.8	V
CMOS input voltage		High level	V_{IH2}		0.7V_{DD}			V
		Low level	V_{IL2}				0.3V_{DD}	V
Input current of pull-up input			I_{IL}	V_{IL}=0 V	–40	–100	–240	µA
Input current of pull-down input			I_{IH}	V_{IH}=V_{DD}	40	100	240	µA
CMOS Schmitt input voltage		High level	Vt+		0.8V_{DD}			V
		Low level	Vt–				0.2V_{DD}	V
	Hysteresis		Vt+–Vt–			0.6		V
Output voltage		High level	V_{OH1}	I_{OH1}=–2 mA	V_{DD}–0.8			V
		Low level	V_{OL1}	I_{OL1}=4 mA			0.4	V
Charge pump output voltage		High level	V_{OH2}	I_{OH2}=–6 mA	V_{DD}–0.8			V
		Low level	V_{OL2}	I_{OL2}=4 mA			0.4	V
Oscillation cell	Input voltage	High level	V_{IH3}		0.7V_{DD}			V
		Low level	V_{IL3}				0.3V_{DD}	V
	Logic threshold		LVth			V_{DD}/2		V
	Feedback resistance		R_{FB}	V_{IN}=V_{SS} or V_{DD}	250 k	1 M	2.5 M	Ω
	Output voltage	High level	V_{OH3}	I_{OH3}=–3 mA	V_{DD}/2			V
		Low level	V_{OL3}	I_{OL3}=3 mA			V_{DD}/2	V

CMOS input pins : DDRQ, SBSY, SBSI, A5 to 0, XWR, XRD, XCS, INTP
CMOS Schmitt input pins : WFCK, XRST
Pull-up input pins : XHCS, HA1, HA0
PUll-down input pin : HMDS
Charge pump output pins : HINT, BA9 to 0
Oscillation cell input pin : XTL1
Oscillation cell output pin : XTL2

The characteristics for all other pins follow the TTL input and output voltage items. All bidirectional data buses are pulled up by standard 25 kΩ resistance.

Input/output capacitance

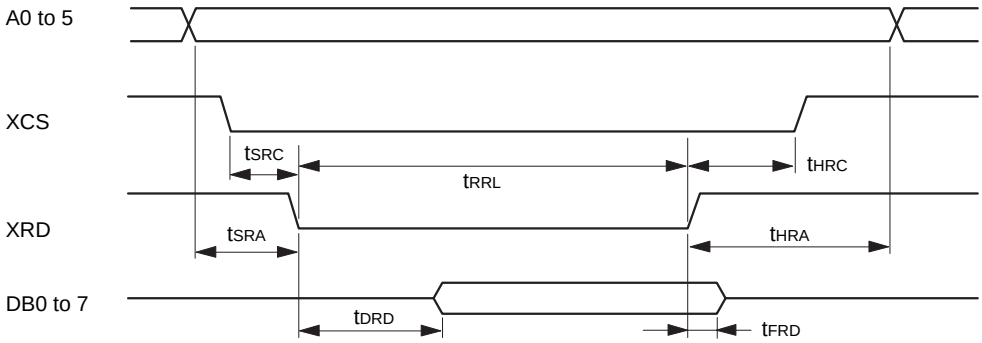
V_{DD}=V_I=0 V, f=1 MHz

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	CIN			9	pF
Output pin	COUT			11	pF
I/O pin	CI/O			11	pF

AC characteristics (Ta=–20 to +75 °C, V_{DD}=5 V±10 %, output load=75 pF, f≤24 MHz)

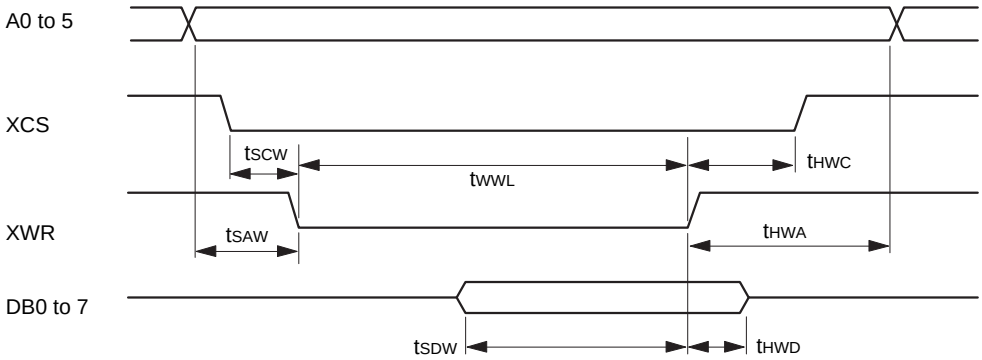
1. CPU interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XRD↓)	t_{SRA}	20			ns
Chip select setup time (vs. XRD↓)	t_{SRC}	0			ns
Data delay time (vs. XRD↓)	t_{DRD}			80	ns
Data float time (vs. XRD↑)	t_{FRD}	3		10	ns
Chip select hold time (vs. XRD↑)	t_{HRC}	0			ns
Address hold time (vs. XRD↑)	t_{HRA}	0			ns
Low-level XRD pulse width	t_{RRL}	100			ns

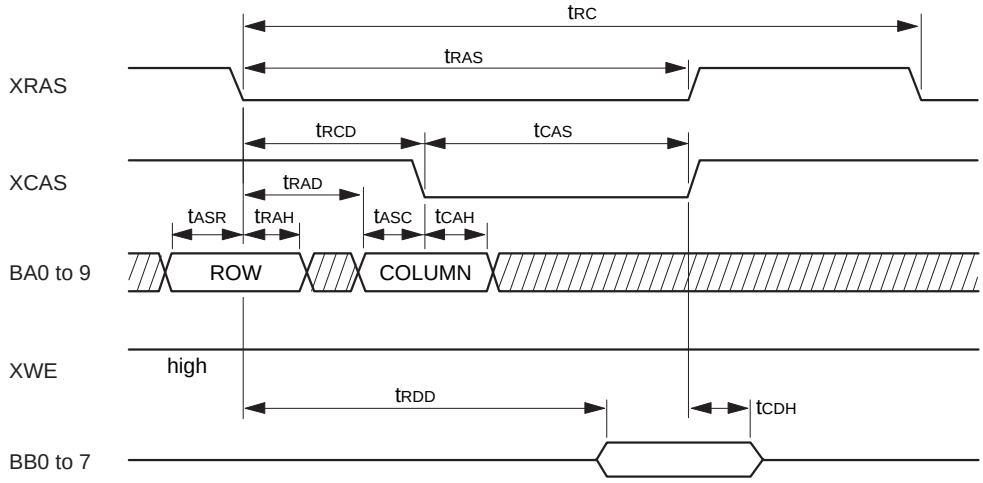
(2) Write



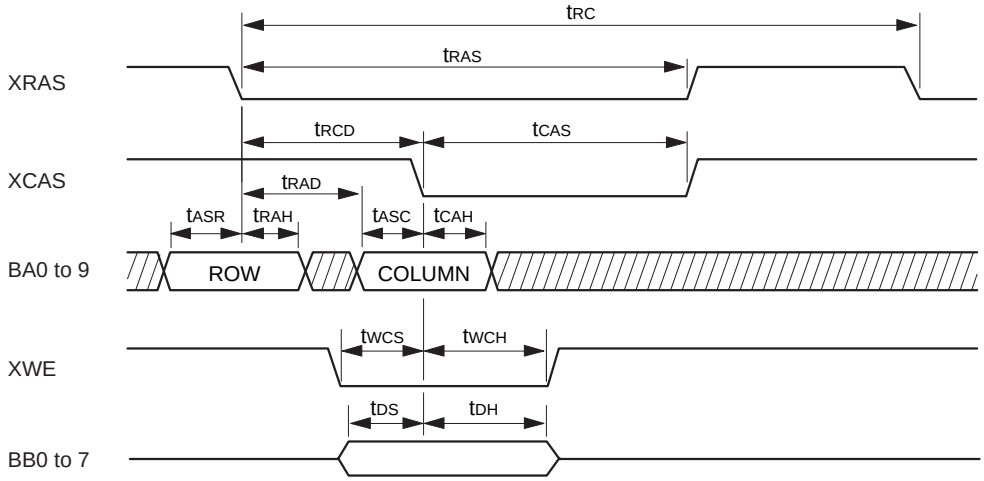
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XWR↓)	t_{SAW}	20			ns
Chip select setup time (vs. XWR↓)	t_{SCW}	0			ns
Data setup time (vs. XWR↓)	t_{SDW}	40			ns
Data hold time (vs. XWR↑)	t_{HWD}	10			ns
Chip select hold time (vs. XWR↑)	t_{HWC}	0			ns
Address hold time (vs. XWR↑)	t_{HWA}	0			ns
Low-level XWR pulse width	t_{WWL}	50			ns

2. DRAM interface

(1) Read



(2) Write

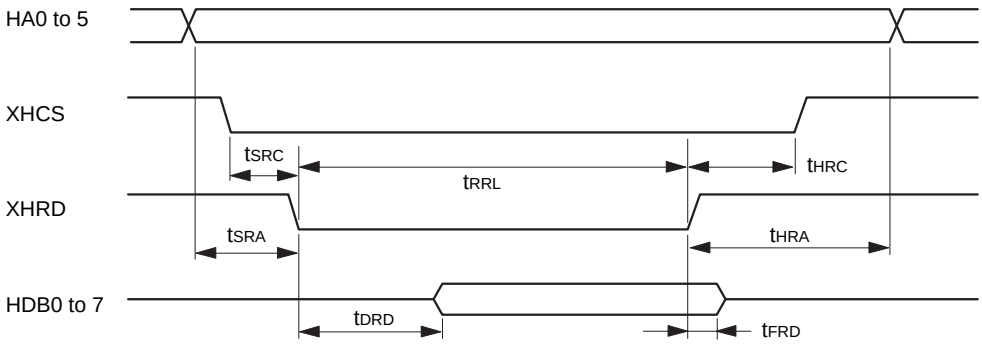


Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	t_{RC}		4Tw		ns
RAS pulse width	t_{RAS}	2Tw+5		2Tw+19	ns
RAS/CAS delay time	t_{RCD}		Tw		ns
CAS pulse width	t_{CAS}	Tw+5		Tw+19	ns
RAS/column address delay time	t_{RAD}	Tw/2+5		Tw/2+17	ns
Row address setup time	t_{ASR}	10			ns
Row address hold time	t_{RAH}	Tw/2			ns
Column address setup time	t_{ASC}	0			ns
Column address hold time	t_{CAH}	Tw/2			ns
Delay time from RAS	t_{RDD}			2TW	ns
Hold time from CAS	t_{CDH}	0			ns
Write command setup time	t_{WCS}	10			ns
Write command hold time	t_{WCH}	20			ns
Data output setup time	t_{DS}	10			ns
Data output hold time	t_{DH}	20			ns

Tw is 1/f here.

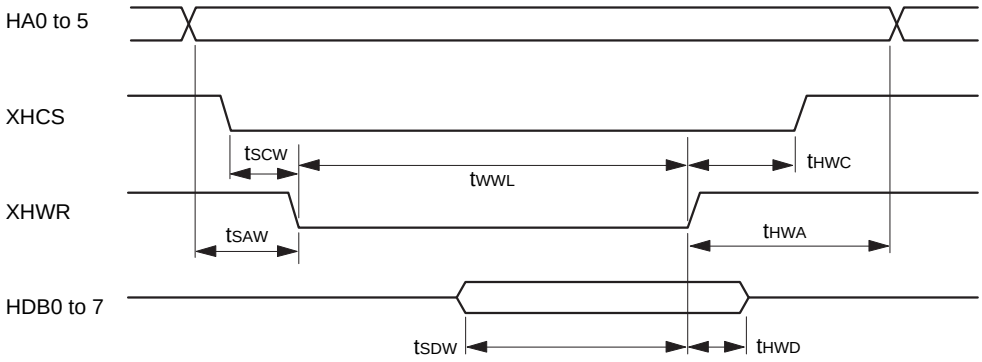
3. Host interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XHRD↓)	t_{SRA}	20			ns
Chip select setup time (vs. XHRD↓)	t_{SRC}	0			ns
Data delay time (vs. XHRD↓)	t_{DRD}			70	ns
Data float time (vs. XHRD↑)	t_{FRD}	2			ns
Chip select hold time (vs. XHRD↑)	t_{HRC}	0			ns
Address hold time (vs. XHRD↑)	t_{HRA}	0			ns
Low-level XHRD pulse width	t_{RRL}	100			ns

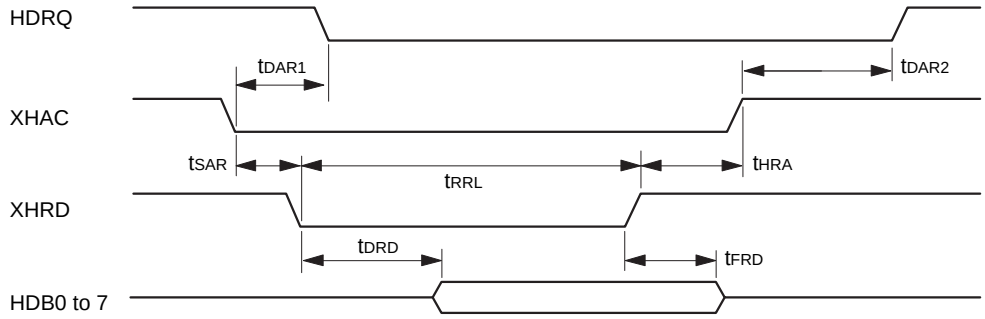
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XHWR↓)	t_{SAW}	20			ns
Chip select setup time (vs. XHWR↓)	t_{SCW}	0			ns
Data setup time (vs. XHWR↓)	t_{SDW}	40			ns
Data hold time (vs. XHWR↑)	t_{HWD}	10			ns
Chip select hold time (vs. XHWR↑)	t_{HWC}	0			ns
Address hold time (vs. XHWR↑)	t_{HWA}	0			ns
Low-level XHWR pulse width	t_{WWL}	50			ns

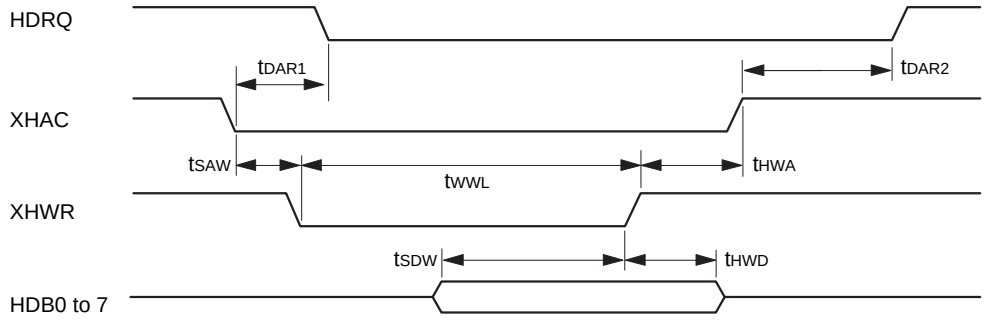
4. Host DMA cycle (80-series bus)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (vs. XHAC↓)	t_{DAR1}			35	ns
HDRQ rise time (vs. XHAC↑)	t_{DAR2}			55	ns
XHAC setup time (vs. XHRD↓)	t_{SAR}	0			ns
XHAC hold time (vs. XHRD↑)	t_{HRA}	0			ns
Low-level XHRD pulse width	t_{RRL}	100			ns
Data delay time (vs. XHRD↓)	t_{DRD}			70	ns
Data float time (vs. XHRD↑)	t_{FRD}	0			ns

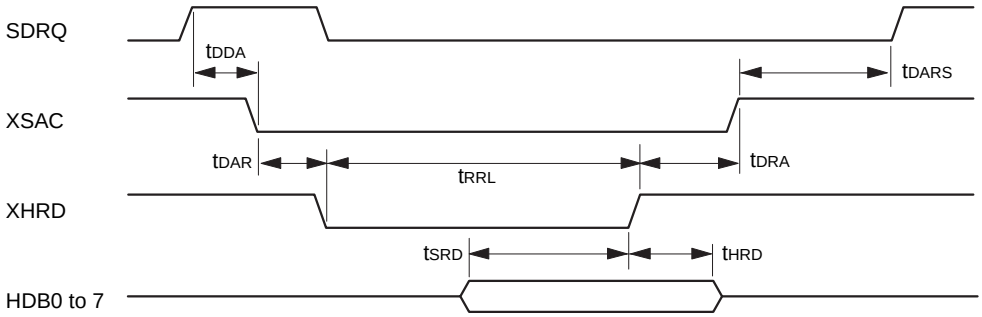
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (vs. XHAC↓)	t_{DAR1}			35	ns
HDRQ rise time (vs. XHAC↑)	t_{DAR2}			55	ns
XHAC setup time (vs. XHWR↓)	t_{SAW}	0			ns
XHAC hold time (vs. XHWR↑)	t_{HWA}	0			ns
Low-level XHWR pulse width	t_{WWL}	50			ns
Data setup time (vs. XHWR↓)	t_{SDW}	40			ns
Data float time (vs. XHWR↑)	t_{HWD}	10			ns

5. Host DMA cycle (SCSI bus)

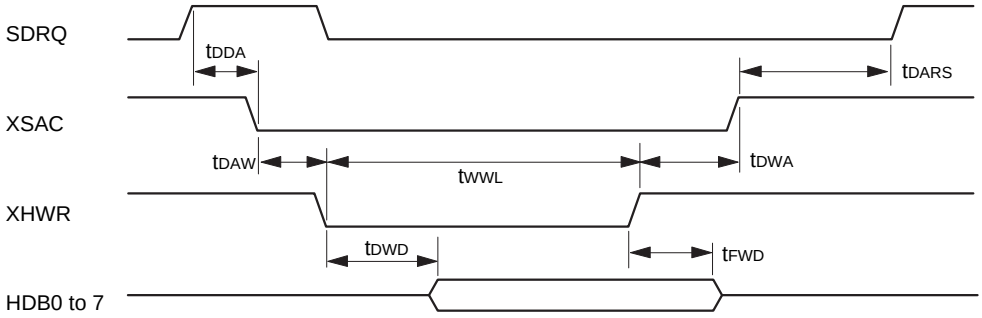
(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall time (vs. SDRQ↓)	t_{DDA}			T_W+31	ns
HDRQ cycle time (vs. XSAC↑)	t_{DARS}			T_W	ns
XHRD delay time (vs. XSAC↑)	t_{DAR}		0		ns
XSAC delay time (vs. XHRD↑)	t_{DRA}		23		ns
Low-level XHRD pulse width	t_{RRL}		2T_W		ns
Data setup time (vs. XHRD↑)	t_{SRD}	15			ns
Data hold time (vs. XHRD↑)	t_{HRD}	5			ns

T_W is 1/f here.

(2) Write

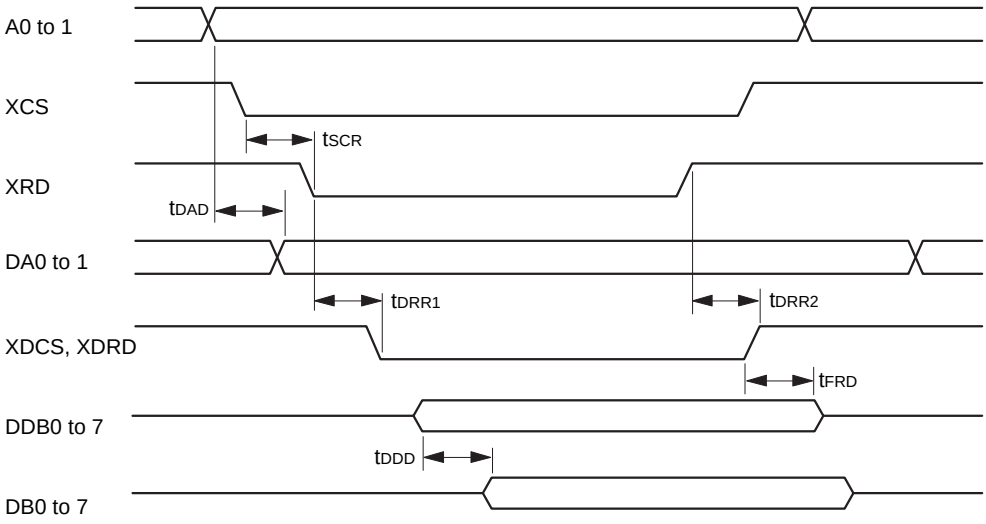


Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall time (vs. SDRQ↓)	t_{DDA}			T_W+31	ns
SDRQ rise time (vs. XSAC↑)	t_{DARS}			T_W	ns
XHWR delay time (vs. XSAC↓)	t_{DAW}			0	ns
XSAC delay time (vs. XHWR↑)	t_{DWA}		24		ns
Low-level XHWR pulse width	t_{WWL}		2T_W		ns
Data delay time (vs. XHWR↓)	t_{DWD}			38	ns
Data float time (vs. XHWR↑)	t_{FWD}	10			ns

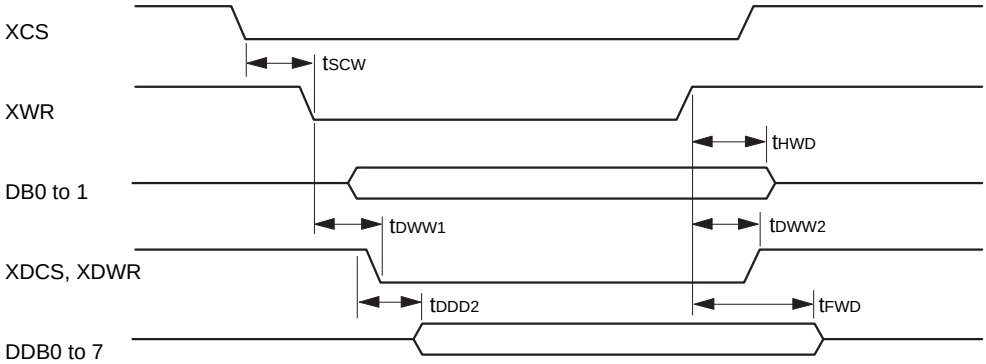
T_W is 1/f here.

6. Drive interface

(1) Read



(2) Write

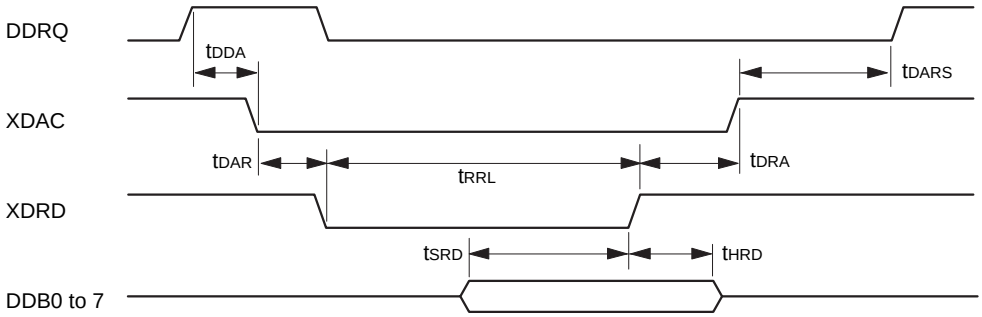


Item	Symbol	Min.	Typ.	Max.	Unit
Drive address delay time (vs. A1 to 0)	t_{DAD}			45	ns
Chip select setup time (vs. XRD↓)	t_{SCR}	0			ns
Drive read signal delay time (vs. XRD↓)	t_{DRR1}			35	ns
CPU data delay time (vs. DDB0 to 7)	t_{DDD}			70	ns
Drive read signal delay time (vs. XRD↑)	t_{DDR2}		27		ns
Data float time (vs. XDRD↑)	t_{FRD}	0			ns
Chip select setup time (vs. XWR↓)	t_{SCW}	0			ns
Drive write signal delay time (vs. XWR↓)	t_{DWW1}			30	ns
Data delay time (vs. DB0 to 7)	t_{DDD2}			70	ns
Data hold time (vs. XWR↑)	t_{HWD}	10			ns
Drive write signal delay time (vs. XWR↑)	t_{DWW2}		24		ns
Data float time (vs. XWR↑)	t_{FWD}	T_W			ns

T_W is 1/f here.

7. Drive DMA cycle

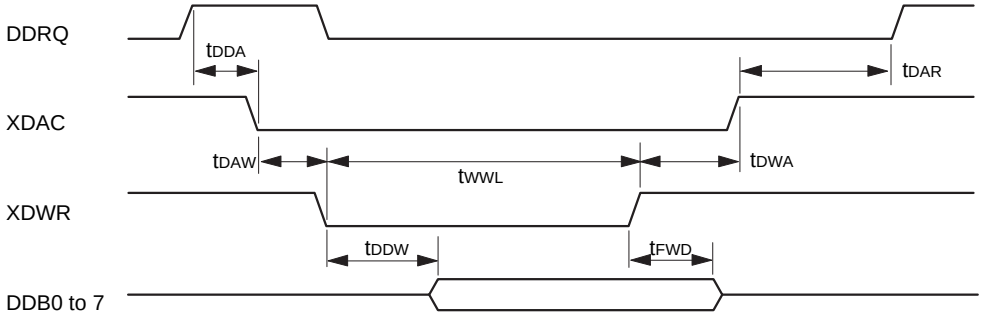
(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
XDAC fall time (vs. DDRQ↑)	t_{DDA}			T_W+32	ns
DDRQ cycle time (vs. XDAC↑)	t_{DARS}			TW	ns
XDRD delay time (vs. XDAC↓)	t_{DAR}			8	ns
XDAC delay time (vs. XDRD↑)	t_{DRA}	0		T_W–5	ns
Low-level XDRD pulse width	t_{RRL}		2T_W+10		ns
Data setup time (vs. XDRD↓)	t_{SRD}	25			ns
Data hold time (vs. XDRD↓)	t_{HRD}	0			ns

T_W is 1/f here.

(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
XDAC fall time (vs. DDRQ↑)	t_{DDA}			T_W+32	ns
DDRQ rise time (vs. XDAC↑)	t_{DARS}			T_W	ns
XDWR delay time (vs. XDAC↓)	t_{DAW}			5	ns
XDAC delay time (vs. XDWR↑)	t_{DWA}			T_W	ns
Low-level XDWR pulse width	t_{WWL}	2T_W+5		2T_W+18	ns
Data delay time (vs. XDWR↓)	t_{DDW}			60	ns
Data float time (vs. XDWR↑)	t_{FWD}	10			ns

T_W is 1/f here.

Description of Functions

1. Pin description

1-1. Drive interface (16 pins)

(1) DDB0 to 7 (Drive Data Bus : bidirectional)
Data bus input/output signals connected with the CXD1186BQ; connected to the HDB0 to 7 pins of the CXD1186BQ.

(2) DDBP (Drive Data Pointer : bidirectional)
Error pointer input/output signal connected with the CXD1186BQ; connected to the HDBE pin of the CXD1186BQ.

(3) XDCS (Drive Chip Select : negative logic output)
Chip select negative logic output signal for reading/writing host interface registers of the CXD1186BQ; connected to the XHCS pin of the CXD1186BQ. The host interface registers of the CXD1186BQ are mapped in 20H to 23H within register address space (00H to 3FH) of this IC.

(4) XDWR (Drive Write Strobe : negative logic output)
Strobe negative logic output signal for writing data into host interface registers of the CXD1186BQ; connected to the XHWR pin of the CXD1186BQ.

(5) XDRD (Drive Read Strobe : negative logic output)
Strobe negative logic output signal for reading data into host interface registers of the CXD1186BQ; connected to the XHRD pin of the CXD1186BQ.

(6) DA0, 1 (Drive Address : output)
Address output signals to the CXD1186BQ; connected to the HA0 and 1 pins of the CXD1186BQ.

(7) DDRQ (Drive DMA Request : positive logic input)
DMA request input signal from the CXD1186BQ; connected to the HDRQ pin of the CXD1186BQ.

(8) XDAC (Drive Acknowledge : negative logic output)
DMA acknowledge negative logic output signal to the CXD1186BQ in response to DDRQ; connected to the XHAC pin of the CXD1186BQ.

1-2. Host interface (18pins)

(1) HDB0 to 7 (Host Data Bus : bidirectional)
Data bus input/output signals connected with host or SCSI control LSI (CXD1185); connected to the D0 to 7 pins for the SCSI control LSI (CXD1185).

(2) HMDS (Host Mode Select : input)
Input signal for selecting host mode. When connected with Intel 80-series CPU bus, set to low or open; when connected with the SCSI control LSI (CXD1185), set to high.

(3) HDRQ/XSAC (Host DMA Request/SCSI DMA Acknowledge : output)
HMDS = low : DMA request positive logic signal to host
HMDS = high : DMA acknowledge negative logic signal to SCSI control LSI (CXD1185)

(4) XHAC/SDRQ (Host DMA Acknowledge/SCSI DMA Request : input)
HMDS = low : DMA acknowledge negative logic signal from host
HMDS = high : DMA request positive logic signal from SCSI control LSI (CXD1185)

(5) XHWR (Host Write Strobe : negative logic input/output)
HMDS = low : Data write strobe negative logic input signal from host
HMDS = high : Data write strobe negative logic output signal to SCSI control LSI (CXD1185); connected to the /WED pin of SCSI control LSI (CXD1185)

(6) XHRD (Host Read Strobe : negative logic input/output)
HMDS = low : Data read strobe negative logic input signal from host
HMDS = high : Data read strobe negative logic output signal to SCSI control LSI (CXD1185); connected to the /RED pin of SCSI control LSI (CXD1185)

(7) XHCS (Host Chip Select : negative logic input)
Pulled up by standard 50 kΩ resistance in the IC.
HMDS = low : Chip select negative logic input signal of host
HMDS = high : Not used; set to high or open

(8) HA0, 1 (Host Address : inputs)
Pulled up by standard 50 kΩ resistance in the IC.
HMDS = low : Address input signal from host
HMDS = high : Not used; set to high or open

(9) HINT (Host Interrupt : output)
Open drain output.
HMDS = low: Interrupt request signal to host
HMDS = high : Not used

(10) HINP (Host Interrupt Polarity : input)
Selects the polarity of the HINT signal; set to low when the HINT signal turns to Low active and high when it turns to High active.

1-3. Buffer Memory Interface (21 pins)

(1) BDB0 to 7 (Buffer Data Bus : input/output)
Buffer memory data bus signals

(2) BA0 to 9 (Buffer Address : output)
Buffer memory address signals; the addresses are output to different pins depending on the setting value of Bits 2 and 3 (Buffer Memory Size) of the Configuration Register: to BA0 to 7 at 64 kB, to BA0 to 8 at 256 kB and to BA0 to 9 at 1 MB.

(3) XRAS (Row Address Strobe : negative logic output)
Strobe negative logic output signal for row address in dynamic RAM.

(4) XCAS (Column Address Strobe : negative logic output)
Strobe negative logic output signal for column address in dynamic RAM.

(5) XWE (Write Enable : negative logic output)
Strobe negative logic output signal for writing in dynamic RAM.

(Note) Use a DRAM with an access time of 80 ns or less in this IC.

1-4. Subcode Interface (4 pins)

(1) WFCK (Write Frame Clock : input)
Write frame clock input signal from the CXD2500; connected to the WFCK pin of the CXD2500.

(2) SBSY (Subcode Sync : positive logic input)
Subcode frame sync input signal from the CXD2500; connected to the SCOR pin of the CXD2500.

(3) SBSI (Subcode Serial Input : input)
Channel P-W subcode data input signal from the CXD2500; connected to the SBSO pin of the CXD2500.

(4) EXCK (External Clock : output)
Readout clock signal to the CXD2500 for reading channel P-W subcode data input to SBSI; connected to the EXCK pin of the CXD2500.

1-5. CPU Interface (19 pins)

(1) DB0 to 7 (CPU Data Bus : input/output)
8-bit CPU data bus signals

(2) A0 to 5 (CPU Address : input)
Address input signals for selecting this IC internal register and the host interface registers of the CXD1186BQ from the CPU

(3) XWR (CPU Write : negative logic input)
Strobe negative logic input signal for the CPU to write data into this IC internal register and the host interface registers of the CXD1186BQ.

(4) XRD (CPU Read : negative logic input)
Strobe negative logic input signal for the CPU to read data from this IC internal register and the host interface registers of the CXD1186BQ.

(5) XCS (Chip Select : negative logic input)
Chip select negative logic input signal for the CPU to read/write data with the register in this IC and the host interface registers of the CXD1186BQ.

(6) INT (CPU Interrupt : output)
Interrupt request signal to CPU

(7) INTP (CPU Interrupt Polarity : input)
Selects the polarity of the INT signal; set to low when the INT signal turns to Low active and high when it turns to High active.

1-6. Clock Signals (3 pins)

(1) XTL1 (X'tal1 : input)

(2) XTL2 (X'tal2 : output)
Inserts a crystal oscillator with a 24 MHZ oscillation frequency between the XTL1 and XTL2 pins. Alternatively, inputs a 24 MHZ clock signal to the XTL1 pin.

(3) HCLK (Half Clock : output)
Half frequency divided clock of XTL2.

1-7. Reset Signals (5 pins)

(1) XRST (Reset : negative logic input)
Power on reset negative logic input signal

(2) XSRS (SCSI Bus Reset : negative logic input)
SCSI bus reset negative logic input signal

(3) XCRS (CPU Reset : negative logic output)
Reset negative logic output signal to the CPU; it is low in either of the cases below.
1) XRST = Low
2) XSRS = low

(4) XHRS (SCSI Reset : negative logic output)
Reset negative logic output signal to the SCSI LSI (CXD1185); it is low in any of the cases below.
1) XRST = Low
2) XSRS = low
3) SCSI reset bit (Bit 2) of reset control register = high

(5) XDRS (Drive Reset : negative logic output)
Reset negative logic output signal to drive block; it is low either of the cases below.
1) XRST = low
2) Drive reset bit (Bit 1) of reset control register = high

2. Description of Register Functions

2-1. Write Registers

(1) Reset Control Register (00H)

Bit 0 : BMM Reset
When this bit is “1”, all the circuits in this IC except for this register and the HCLK frequency divider circuit are initialized. This bit is automatically set to “0” after the IC has been initialized.

Bit 1 : Drive Reset
When this bit is “1”, the XDRS pin is set to low (activated).

Bit 2 : SCSI Reset
When this bit is “1”, the XSRS pin is set to low (activated).

Bit 3 : Reserved

Bit 4 : Reserved

Bit 5 : Reserved

Bit 6 : Reserved

Bit 7 : Reserved

(2) DMA Control Register-1 (01H)

Bit 0 : Drive DMA Enable
DMA with the CXD1186BQ is enabled when “1” is written in this bit.

Bit 1 : Drive DMA Source
Selects the transfer direction of DMA with the CXD1186BQ : when “0”, data is transferred from the buffer memory to the CXD1186BQ and when “1”, from the CXD1186BQ to the buffer memory. This bit is valid only when Bits 0 is “1”.

Bit 2 : Error Pointer Transfer Enable
When this bit is “1”, the error pointers are written into the buffer memory together with the main channel data. This bit is valid only when Bits 0 and 1 are both “1”.

Bit 3 : Error Pointer Transfer Mode
Selects the format for writing the error pointers into the buffer memory. When “0”, all the error pointers starting from the address selected by the Pointer DMA Address Counter are written separately from the main channel data (separated mode). When “1”, 1 byte of the error pointer is written immediately after 8-byte of the main channel data (mixed mode). (The value of Pointer DMA Address Counter is ignored in this case.) This bit is valid only when Bits 0, 1 and 2 are all “1”.

Bit 4 : Sync Pattern Enable
When this bit is “1” a 12-byte dummy sync pattern is written starting with the address selected by the Drive DMA Address Counter before the data is written from the CXD1186BQ into the buffer memory. (It is assumed in this case that the error pointer of the sync byte is “0”.) This bit is valid only when Bits 0 and 1 are both “1”.

Bit 5 : Reserved

Bit 6 : Reserved

Bit 7 : Reserved

(3) DMA Control Register-2 (02H)

Bit 0 : Host DMA Enable
DMA with the host is enabled when “1” is written in this bit.

Bit 1 : Host DMA Source
Selects the transfer direction of DMA with the host : when “0”, from the buffer memory to the host; and when “1”, from the host to the buffer memory. This bit is valid only when Bit 0 is “1”.

Bit 2 : CPU DMA Enable
DMA with the CPU is enabled via the CPU DMA Data Register when “1” is written in this bit.

Bit 3 : CPU DMA Source
Selects the transfer direction of DMA with the CPU : when “0”, data is transferred from the buffer memory to the CPU DMA Data Register; and when “1”, from the CPU DMA Data Register to the buffer memory. This bit is valid only when Bit 2 is “1”.

Bit 4: Subcode P-W Decode Enable
Decoding of the channel P-W subcode from the CXD2500 is enabled when this bit is “1”. Subcodes are decoded inside this IC.

Bit 5 : Subcode P-W DMA Enable
The channel P-W subcodes decoded inside this IC can be written into the buffer memory when “1”. However, even when this bit is “1”, DMA will commence 3 sectors after Bit 4 has been set to “1”.

Bit 6 : Subcode P-W ECC Enable
When this bit is “1”, errors in the channel R-W subcodes are corrected. This bit is a valid only when Bit 4 is “1”.

Bit 7 : Subcode P-W ECC Strategy
When this bit is “1”, double correction is provided while the channel R-W subcodes are corrected. This bit is valid only when Bit 4 is “1”.

(4) CPU DMA Data Register (03H)

Data is written into this register when it is written from the CPU into the buffer memory.

(5) Interrupt Mask Register (04H)

When “1” is written in all the bits of this register and one or more of the interrupt causes corresponding to these bits (with “1” written) arise, the INT pin is activated. The values of Bits 0 to 5 of this register do not affect the values of the interrupt status register. Use Bit 6 (Sub Q Interrupt) as the enable register rather than mask register. When Bit 6 (Sub Q Interrupt) is “1” and a Sub Q interrupt arrives, the values of Interrupt Status Register are set to “1”.

Bit 0 : Drive DMA Complete
BIt 1 : Subcode P-W DMA Complete
Bit 2 : Host DMA Complete
Bit 3 : Host Chip Reset Issued
BIt 4 : Host Command
BIt 5 : Error Pointer DMA Complete
Bit 6 : Sub Q Interrupt
Bit 7 : Reserved

(6) Clear Interrupt Status Register (05H)

When any of respective bits of this register is set to “1”, the corresponding interrupt status is cleared. The bit is automatically turns to “0” after the interrupt status have been cleared.

Bit 0 : Drive DMA Complete
Bit 1 : Subcode P-W DMA Complete
Bit 2 : Host DMA Complete
Bit 3 : Host Chip Reset Issued
Bit 4 : Host Command
Bit 5 : Error Pointer DMA Complete
Bit 6 : Sub Q Interrupt
Bit 7 : Reserved

(7) Host Result Register (06H)

This register is utilized to transfer the command execution result to the host when the HMDS pin is low. It consists of a 10-byte FIFO.

(8) Host Interface Control Register (07H)

Controls the host interface hardware when the HMDS pin is low. It has the same specifications as the host interface control register of the CXD1186BQ.

Bit 0 : Host Interrupt #1
This bit value becomes the value of HINTSTS#1 (bit 0) of the Status register on the host side.
Bit 1 : Host Interrupt #2
This bit value becomes the value of HINTSTS#2 (bit 1) of the Status register on the host side.
Bit 2 : Host Interrupt #3
This bit value becomes the value of HINTSTS#3 (bit 2) of the Status register on the host side.

(Note) Once “1” has been written into Bits 0 to 2, the bits will keep at “1” until they are cleared from the host or the chip is reset. This register cannot be accessed from the CPU to set Bits 0 to 2 from “1” to “0”. Accordingly, to set any of these bits, it is not necessary to take into consideration the value of the other bits. Writing “1” into these bits is prohibited when the corresponding Host Interrupt Status #1 to #3 bits of the Host Interface Status Register are “1”. Therefore, before writing “1” into these bits, the CPU must read the Host Interface Status Register and confirm that the corresponding Host Interrupt Status #1 to #3 bits are “0”.

Bit 3 : Reserved
Bit 4 : Reserved
Bit 5 : Reserved
Bit 6 : Clear Result
The host result register is cleared when “1” is written into this bit. This bit is automatically turns to “0” when the clearing of the host result register has been completed. There is therefore no need for the CPU to write “0” again.
Bit 7 : Clear Busy
The busy status bit of the host interrupt status register is cleared when “1” is written into this bit. This bit is automatically turns to “0” when the clearing of the busy status bit has been completed. There is therefore no need for the CPU to write “0” again.

(9) Drive DMA Address Counter Lower (08H)

(10) Drive DMA Address Counter Middle (09H)

(11) Drive DMA Address Counter Upper (0AH)
These are 20-bit registers for setting the address from which to start the DMA transfer with the CXD1186BQ. Their values are incremented each time 1 byte has been transferred by DMA.

(12) Drive DMA Transfer Counter Lower (0BH)

(13) Drive DMA Transfer Counter Upper (0CH)
These are 12-bit registers for setting the number of bytes to be transferred by DMA with the CXD1186BQ. Their values are decremented each time 1 byte has been transferred by DMA.

(14) Error Pointer DMA Address Counter Lower (0DH)

(15) Error Pointer DMA Address Counter Middle (0EH)

(16) Error Pointer DMA Address Counter Upper (0FH)
These are 20-bit registers for setting the address from which to start writing error pointers from the CXD1186BQ when Bit 3 (pointer transfer mode) of the DMA Control Register is “0”. Their values are incremented each time 8 bits (1 byte) have been transferred by DMA.

(17) Subcode P-W DMA Address Counter Lower (10H)

(18) Subcode P-W DMA Address Counter Middle (11H)

(19) Subcode P-W DMA Address Counter Upper (12H)
These are 20-bit registers for setting the address from which to start writing the channel P-W subcodes from the CXD2500. Their values are incremented each time 1 byte (1 symbol) has been transferred by DMA.

(20) Host DMA Address Counter Lower (13H)

(21) Host DMA Address Counter Middle (14H)

(22) Host DMA Address Counter Upper (15H)
These are 20-bit registers for setting the address from which to start the data transfer by DMA with the host. Their values are incremented each time 1 byte has been transferred by DMA.

(23) Host DMA Transfer Counter Lower (16H)

(24) Host DMA Transfer Counter Upper (17H)
These are 16-bit registers for setting the number of bytes transferred by DMA with the host. Their values are decremented each time 1 byte has been transferred by DMA.

(25) CPU DMA Address Counter Lower (18H)

(26) CPU DMA Address Counter Middle (19H)

(27) CPU DMA Address Counter Upper (1AH)

These are 20-bit registers for setting the address from which to start the data transfer by DMA with the CPU. Their values are incremented each time 1 byte has been transferred by DMA.

(28) Configuration Register (1BH)

Bit 0 : CDL 3 × Series
This bit is set to "1" when connected to the CDL30 or 35 series LSI.

Bit 1 : Packet Mode
When this bit is "0", transfers the decoded data in 4 packs to the DRAM for each subcode sync; when it is "1", transfers the decoded data in 4 packs starting from the pack prior to the fifth pack to the DRAM for each subcode sync.

Bit 2 : Buffer Memory Size 1

Bit 3 : Buffer Memory Size 2
Select the buffer memory size : 64 kB with (Bit 3, Bit 2) = (0, 0), 256 kB with (0, 1) and 1 MB with (1, x).

Bit 4 : Error Pointer Write Data
Sets the error pointer (DDBP) value when data is transferred by DMA from the buffer memory to the CXD1186BQ.

Bit 5 : HCLK Disable Mode
The HCLK output remains low when this bit is "1". When "0", a clock signal with half the frequency of XTL2 is output from the HCLK output.

Bit 6 : Reserved

Bit 7 : Reserved

(29) Drive Command Register (20H)

The command register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

(30) Drive Parameter Register (21H)

The parameter register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

(31) Drive Write Data Register (22H)

The write data register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

(32) Drive Control Register (23H)

The control register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

2-2. Read Registers

(1) BMM Status Register (00H)

Bit 0 : Reset Condition
This bit is set to “1” when XSRS is low and “0” when XRST is low or when “1” is written into Bit 0 (BMM Reset) of the Reset Control Register. It is used for determining whether the CPU which was reset externally was the SCSI bus or power-on.

Bit 1 : CPU Buffer Read Ready
This bit is set to “1” when the 1-byte data read from the buffer memory is provided in the CPU DMA Data Register. It returns to “0” when the data in the CPU DMA Data Register is read.

Bit 2 : CPU Buffer Write Ready
This bit is set to “0” when1-byte data is written into the CPU MDA Data Register. It is set to “1” when the data in the CPU DMA data register is written into the buffer memory.

Bit 3 : Pointer Status Flag
This bit is set to “1” when one or more error pointers were set in 1 block of data transferred from the CXD1186BQ. It is cleared to “0” by setting a value in the Drive DMA Transfer Counter.

Bit 4 : Subcode ECC Status #0
Indicates the results of the error correction in channel R-W subcode pack #0. It is set to “1” when uncorrectable data errors occur.

Bit 5 : Subcode ECC Status #1
Indicates the results of the error correction in channel R-W subcode pack #1. It is set to “1” when uncorrectable data errors occur.

Bit 6 : Subcode ECC Status #2
Indicates the results of the error correction in channel R-W subcode pack #2. It is set to “1” when uncorrectable data errors occur.

Bit 7 : Subcode ECC Status #3
Indicates the results of the error correction in channel R-W subcode pack #3. It is set to “1” when uncorrectable data errors occur.

(2) DMA Status Register-1 (01H)

The setting values of DMA Control Register-1 can be read from this register.

Bit 0 : Drive DMA Enable
Bit 1 : Drive DMA Source
Bit 2 : Pointer Transfer Enable
Bit 3 : Pointer Transfer Mode
Bit 4 : Sync Pattern Enable
Bit 5 : Reserved
Bit 6 : Reserved
Bit 7 : Reserved

(3) DMA Status Register-2 (02H)

The setting values of DMA Control Register-2 can be read from this register.

Bit 0 : Host DMA Enable
Bit 1 : Host DMA Source
Bit 2 : CPU DMA Enable
Bit 3 : CPU DMA Source
Bit 4 : Reserved
Bit 5 : Subcode P-W DMA Enable
Bit 6 : Subcode P-W ECC Enable
Bit 7 : Subcode P-W ECC Strategy

(4) CPU DMA Data Register (03H)

The data read from the buffer memory by DMA with the CPU is written into this register.

(5) Interrupt Status Register (04H)

The values of this register's bits indicate the corresponding interrupt statuses respectively.

Bit 0 : Drive DMA Complete
This is set to "1" when data transfer by DMA with the CXD1186BQ is completed.
Bit 1 : Subcode P-W DMA Complete
This is set to "1" when the channel P-W subcodes have been written into the buffer memory.
Bit 2 : Host DMA Complete
This is set to "1" when data transfer by DMA with the host is completed.
Bit 3 : Host Chip Reset Issued
This is set to "1" when the host writes "1" into Bit 7 (Chip Reset Bit) of the Host Control Register and this IC is reset.
Bit 4 : Host Command
This is set to "1" when the host writes a 1 byte command into the Host Command Register.
Bit 5 : Pointer DMA Complete
This is set to "1" when the DMA transfer of pointers is completed.
Bit 6 : Sub Q Interrupt
This is set to "1" if the falling edge of the SBSY pin (connected to the SCOR pin of the CXD2500) is detected when "1" has been written into Bit 6 (Sub Q Interrupt) of the Interrupt Mask Register.
Bit 7 : Reserved

(6) Host Command Register (05H)

This register is used to know the commands from the host when the HMDS pin is low.

(7) Host Parameter Register (06H)

This register is used to know the command parameters from the host when the HMDS pin is low. It consists of a 10-byte FIFO.

(8) Host Interface Status Register (07H)

This register is used to know the status of the host interface hardware when the HMDS pin is low. It has the same specifications as the Host Interface Control Register of the CXD1186BQ.

Bit 0 : Host Interrupt Status #1
This bit turns to "1" when the CPU writes "1" into host interrupt #1 (Host Interface Control Register Bit 0). It is set to "0" when the host writes "1" into CLRINT #1 (Control Register Bit 0). This bit is used to monitor the interrupt status to the host.

Bit 1 : Host Interrupt Status #2
This bit turns to "1" when the CPU writes "1" into host interrupt #2 (Host Interface Control Register Bit 1). It is set to "0" when the host writes "1" into CLRINT #2 (Control Register Bit 1). This bit is used to monitor the interrupts status to the host.

Bit 2 : Host Interrupt Status #3
This bit turns to "1" when the CPU writes "1" into host interrupt #3 (Host Interface Control Register Bit 2). It is set to "0" when the host writes "1" into CLRINT #3 (Control Register Bit 2). This bit is used to monitor the interrupts status to the host.

Bit 3: Parameter Read Ready
When this bit is "1", it indicates that the Parameter Register of the host is not empty and parameter data can be read from the CPU. When "0", the Parameter Register is empty.

Bit 4: Parameter Full
When this bit is "1", it indicates that the Parameter Register of the host is full.

Bit 5: Result Write Ready
When this bit is "1", it indicates that the Host Result Register is not full and result data can be written from the CPU. When "0", the Host Result Register is full and the CPU cannot write the result data into the register.

Bit 6: Result Empty
When this bit is "1", it indicates that the Host Result Register is empty.

Bit 7: Busy Status
This bit has the same value as Bit 7 of the Host Status Register. It is set to "1" when the host writes a command in the Command Register. It is set to "0" when the CPU writes "1" into the Clear Busy Bit of the Host Interface Control Register.

(9) Drive DMA Address Counter Lower (08H)

(10) Drive DMA Address Counter Middle (09H)

(11) Drive DMA Address Counter Upper (0AH)
Indicate the Drive DMA Address Counter values.

(12) Drive DMA Transfer Counter Lower (0BH)

(13) Drive DMA Transfer Counter Upper (0CH)
Indicate the Drive DMA Transfer Counter values.

(14) Error Pointer DMA Address Counter Lower (0DH)

(15) Error Pointer DMA Address Counter Middle (0EH)

(16) Error Pointer DMA Address Counter Upper (0FH)
Indicate the Error Pointer DMA Address Counter values.

(17) Subcode P-W DMA Address Counter Lower (10H)

(18) Subcode P-W DMA Address Counter Middle (11H)

(19) Subcode P-W DMA Address Counter Upper (12H)
Indicate the Subcode P-W DMA Address Counter values.

(20) Host DMA Address Counter Lower (13H)

(21) Host DMA Address Counter Middle (14H)

(22) Host DMA Address Counter Upper (15H)
Indicate the Host DMA Address Counter values.

(23) Host DMA Transfer Counter Lower (16H)

(24) Host DMA Transfer Counter Upper (17H)
Indicate the Host DMA Transfer Counter values.

(25) CPU DMA Address Counter Lower (18H)

(26) CPU DMA Address Counter Middle (19H)

(27) CPU DMA Address Counter Upper (1AH)
Indicate the CPU DMA Address Counter values.

(28) Drive Status Register (20H)
The Status Register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

(29) Drive Result Register (21H)
The Result Register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

(30) Drive Read Data Register (22H)
The Read Data Register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

(31) Drive FIFO Status Register (23H)
The FIFO Status Register for the host interface of the CXD1186BQ is mapped in the register address space of this IC.

Write Register

Reset Control Register (00H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
					SCSI IC Reset	Drive Reset	BMM Reset

DMA Control Register - 1 (01H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
			Sync Pattern Enable	Pointer Transfer Mode	Pointer Transfer Enable	Drive DMA Source	Drive DMA Enable

DMA Control Register - 2 (02H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Subcode ECC Strategy	Subcode ECC Enable	Subcode DMA Enable	Subcode Decode Enable	CPU DMA Source	CPU DMA Enable	Host DMA Source	Host DMA Enable

CPU DMA Data Register (03H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	D0

Interrupt Mask Register (04H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Sub Q interrupt	Pointer DMA Complete	Host Command	Host Chip Reset Issued	Host DMA Complete	Subcode DMA Complete	Drive DMA Complete

Clear Interrupt Register (05H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Sub Q interrupt	Pointer DMA Complete	Host Command	Host Chip Reset Issued	Host DMA Complete	Subcode DMA Complete	Drive DMA Complete

Host Result Register (06H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	D0

Host Interface Control Register (07H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Clear Busy	Clear Result				Host Interrupt #3	Host Interrupt #2	Host Interrupt #1

Drive DMA Address Counter Lower (08H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Drive DMA Address Counter Middle (09H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Drive DMA Address Counter Upper (0AH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Drive DMA Transfer Counter Lower (0BH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Drive DMA Transfer Counter Upper (0CH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A11	A10	A9	A8

Pointer DMA Address Counter Lower (0DH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Pointer DMA Address Counter Middle (0EH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Pointer DMA Address Counter Upper (0FH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Subcode P-W DMA Address Counter Lower (10H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Subcode P-W DMA Address Counter Middle (11H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Subcode P-W DMA Address Counter Upper (12H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Host DMA Address Counter Lower (13H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Host DMA Address Counter Middle (14H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Host DMA Address Counter Upper (15H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Host DMA Transfer Counter Lower (16H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Host DMA Transfer Counter Upper (17H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

CPU DMA Address Counter Lower (18H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

CPU DMA Address Counter Middle (19H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

CPU DMA Address Counter Upper (1AH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Configuration Register (1BH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		HCLK Disable Mode	Error Pointer Write Data	Buffer Memory Size 2	Buffer Memory Size 1	Packet Mode	CDL3X Series

Drive Command Register (20H)

Drive Parameter Register (21H)

Drive Write Data Register (22H)

Drive Control Register (23H)

Internal RAM-1 Write (30H)

Internal RAM-2 Write (31H)

Test Register (35H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		Reset Signal Sync	HCLK Reset	TSTE	TSTD	REF Block Test	SUB Block Test

Read register

BMM Status Register (00H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Subcode ECC Status #3	Subcode ECC Status #2	Subcode ECC Status #1	Subcode ECC Status #0	Pointer Status Flag	CPU Buffer Write Ready	CPU Buffer Read Ready	Reset Condition

DMA Status Register - 1 (01H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
			Sync Pattern Enable	Pointer Transfer Mode	Pointer Transfer Enable	Drive DMA Source	Drive DMA Enable

DMA Status Register -2 (02H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Subcode ECC Strategy	Subcode ECC Enable	Subcode DMA Enable		CPU DMA Source	CPU DMA Enable	Host DMA Source	Host DMA Enable

CPU DMA Data Register (03H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	D0

Interrupt Status Register (04H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Sub Q interrupt	Pointer DMA Complete	Host Command	Host Chip Reset Issued	Host DMA Complete	Subcode DMA Complete	Drive DMA Complete

Host Command Register (05H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	D0

Host Parameter Register (06H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	D0

Hot Interface Status Register (07H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Busy Status	Result Empty	Result Write Ready	Parameter Full	Parameter Read Ready	Host Interrupt #3	Host Interrupt #2	Host Interrupt #2

Drive DMA Address Counter Lower (08H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Drive DMA Address Counter Middle (09H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Drive DMA Address Counter Upper (0AH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Drive DMA Transfer Counter Lower (0BH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Drive DMA Transfer Counter Upper (0CH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A11	A10	A9	A8

Pointer DMA Address Counter Lower (0DH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Pointer DMA Address Counter Middle (0EH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Pointer DMA Address Counter Upper (0FH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Subcode P-W DMA Address Counter Lower (10H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Subcode P-W DMA Address Counter Middle (11H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Subcode P-W DMA Address Counter Upper (12H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Host DMA Address Counter Lower (13H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Host DMA Address Counter Middle (14H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

Host DMA Address Counter Upper (15H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Host DMA Transfer Counter Lower (16H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

Host DMA Transfer Counter Upper (17H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

CPU DMA Address Counter Lower (18H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A7	A6	A5	A4	A3	A2	A1	A0

CPU DMA Address Counter Middle (19H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A15	A14	A13	A12	A11	A10	A9	A8

CPU DMA Address Counter Upper (1AH)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				A19	A18	A17	A16

Drive Status Register (20H)

Drive Result Register (21H)

Drive Read Data Register (22H)

Drive FIFO Status Register (23H)

Internal RAM-1 Read (30H)

Internal RAM-2 Read (31H)

Internal LOG Read (32H)

Internal ALOG Read (33H)

Internal FPAL Read (34H)

3. DMA Functions

3-1. Overview

This IC accepts requests for DMA to the buffer memory from the six DMA channels of drive (CXD1186BQ), error pointer (CXD1186BQ), subcode P-W (CXD2500), host CPU and buffer memory (DRAM) refresh. Then, it generates memory cycle signals for an external buffer memory (DRAM), and executes DMA cycles.

3-2. DMA Address Counters

The DMA address counters hold the buffer memory addresses of each DMA channel, which are divided into row and column addresses as the memory addresses of the external DRAM buffer memory in accordance with the Configuration Register Bits 2 and 3 (buffer memory size) setting, and output the addresses from BA0 to 9. The address counter values for each DMA channel are incremented each time the DMA cycle is executed. The DMA address counter values of five channels (except the buffer memory refresh channel) can be set or read from the CPU.

3-3. DMA Transfer Counters

The DMA transfer counters hold the number of bytes to be transferred for each DMA channel, they are decremented each time a DMA cycle is executed, and DMA is completed when their values reach zero. The values of the DMA transfer counters for the drive (CXD1186BQ) and host DMA channels can be set or read from the CPU but the initial setting of the DMA transfer counter for the subcode P-W (CXD2500) channel is fixed and its value cannot be set or read from the CPU. The CPU and buffer memory refresh channels do not have DMA transfer counters.

3-4. Drive DMA Channel

(1) Execution of DMA cycle

DMA transfer for the drive DMA channel is requested by making the DDRQ signal activated, and the DMA cycle is executed.

(2) Procedure of control from CPU

Described below is the procedure of control exercised by this IC when DMA transfer for the drive DMA channel is to be executed.

- The number of bytes to be transferred is written into the drive DMA transfer counter.
- The head address of the buffer memory to be accessed is written into the drive DMA address counter (and also into the error pointer DMA address counter if necessary).
- “1” is written into Bit 0 (drive DMA enable) of DMA Control Register-1, and the prescribed values are written into Bits 1 to 4. (This causes the DMA cycle execution to start.)
- When the DMA transfer of the number of bytes written into the drive DMA transfer counter is completed, Interrupt Status Register Bit 0 (drive DMA complete) is set to “1”. Also, the drive DMA transfer register is zero, and the drive DMA address counter holds the address following the buffer memory address in which data was last transferred by DMA.

(3) Variations of DMA transfer for drive DMA channel

Depending on the settings of Bits 0 to 4 of DMA Control Register-1, options such as the addition of a dummy sync pattern or DMA transfer of error pointers can be selected for the DMA transfer of the drive DMA channel, as shown in the table below.

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Description of DMA transfer
0	×	×	×	×	DMA transfer prohibited
1	0	×	×	×	DMA transfer of main channel data and error pointers from buffer memory to the CXD1186BQ
1	1	0	×	0	Writing of main channel data from the CXD1186BQ into buffer memory
1	1	0	×	1	Addition of dummy sync pattern at head of above data
1	1	1	0	0	Writing of main channel data and error pointers from the CXD1186BQ into buffer memory (separated mode)
1	1	1	0	1	Addition of dummy sync pattern at head of above data
1	1	1	1	0	Writing of main channel data and error pointers from the CXD1186BQ into buffer memory (mixed mode)
1	1	1	1	1	Addition of dummy sync pattern at head of above data

(4) DMA transfer of pointers

When DMA transfer from the CXD1186BQ (9-bit data) into the buffer memory (8-bit data), the error pointers sent together with the drive main channel data are serial-to-parallel converted in the IC and the data is written one byte at a time into the buffer memory. When executing DMA for error pointers, therefore, the number of drive DMA transfer must be a multiple of 8.

When DMA transfer from the buffer memory (8-bit data) to the CXD1186BQ (9-bit data), the value selected by Bit 4 (error pointer write data) of the Configuration Register is used as the error pointer, and only the number of transferring bytes set in the drive DMA transfer counter is output from the DDBP pin along with the main channel data.

When DMA transfer from the CXD1186BQ (9-bit data) into the buffer memory (8-bit data), 8-byte of the main channel data are first written, and then 8-bit of the error pointer corresponding to this data is written as 1-byte data. As described below, there are two modes for writing the main channel data and error pointers.

- Separated mode

  The main channel data and error pointers are separated and written in different locations on the buffer memory. The write head address for each is set in the drive DMA address counter and pointer DMA address counter. The number of transferring bytes of the main channel data is set in the drive DMA transfer counter.

- Mixed mode

  8-byte of the main channel data and 1 byte of the error pointer are repeated in this sequence and written in a continuous buffer memory address. The write head address is set in the drive DMA address counter, and the pointer DMA address counter value is ignored. The number of bytes transferred of the main channel data is set in the drive DMA transfer counter.

(5) Writing of dummy sync patterns into buffer memory

If Bit 4 (sync pattern enable) of DMA Control Register-1 is set to “1” when DMA transfer from the CXD1186BQ to the buffer memory, a 12-byte dummy sync pattern is generated in the IC and written into the buffer memory prior to data transfer from the CXD1186BQ. Following the dummy sync pattern from the buffer memory address set in the drive DMA address counter, the data from the CXD1186BQ is written into the buffer memory. The number of bytes for data transferred from the CXD1186BQ must be set in the drive DMA transfer counter. (Exclude the number of dummy sync patterns.)

3-5. Subcode P-W DMA Channel

When Bit 5 (subcode P-W DMA enable) of DMA Control Register-2 is set to “1”, the channel P-W subcodes decoded in this IC are written into the buffer memory. The number of bytes transferred is fixed (at 96).

(1) Execution of DMA cycle

DMA transfer of the subcode P-W DMA channel is requested by the timing generator signal used to read the subcode P-W in this IC, and the DMA cycle is executed.

(2) Procedure for controlling IC from CPU

Described below is the procedure for controlling this IC when subcode P-W channel DMA is to be executed.

- Write “1” into Bit 4 (subcode P-W decode enable) of DMA Control Register-2 to execute DMA of the subcode P-W channel. As a result, subcode P-W decoding commences.
- Write the head address of the buffer memory to be directly accessed into the Subcode P-W DMA Address Counter.
- Write “1" into Bit 5 (subcode P-W DMA enable) of DMA Control Register-2. (As a result, the DMA cycle is executed when the decoding has been completed.)
- When the DMA transfer of 96 bytes is completed, Bit 1 (subcode P-W DMA complete) of the Interrupt Status Register is set to “1”. The Subcode P-W DMA Address Counter holds the address value following the buffer memory address which was last transferred by DMA.

(3) Subcode P-W error correction

Subcode P-W errors are corrected when “1” is written into Bit 6 (subcode P-W ECC enable) of DMA Control Register-2 at the same time as “1” is written into Bit 5 (subcode P-W DMA enable of the same register). In this case, Bit 1 (subcode P-W DMA complete) of the Interrupt Status Register-1 is set to “1” when all the operations up to the DMA transfer have been completed. Double correction is performed when “1” is written into Bit 7 (subcode P-W ECC strategy) of DMA Control Register-2.

(4) Error discrimination

Upon completion of the DMA transfer, the presence or absence of errors in each of 4 packs is written into Bits 4 to 7 of the BMM Status Register. These statuses are valid for about 13 ms after DMA transfer is completed.

3-6. Host DMA Channel

(1) Execution of DMA cycle
DMA transfer of the host DMA channel is requested when the HDRQ signal becomes activated, and the DMA cycle is executed. For further details, refer to chapter 4.

(2) Procedure for controlling IC from CPU
Described below is the procedure for controlling this IC when DMA transfer of the host DMA channel is executed.

- Write the number of bytes transferred into the Host DMA Transfer Counter.
- Write the head address of the buffer memory, to which the data is transferred by DMA, into the Host DMA Address Counter.
- Write “1” into Bit 0 (host DMA enable) of DMA Control Register-2 and “0” or “1” into Bit 1 (host DMA source) depending on the transfer direction. (When these are written, the DMA cycle execution commences.)
- When the DMA transfer of the number of bytes written into the Host DMA transfer counter is completed, Bit 3 (host DMA complete) of the Interrupt Status Register is set to “1”. Also, the Host DMA Transfer Register is zero, and the Host DMA address counter holds the value of the address following the buffer memory address which was last transferred by DMA.

3-7. CPU DMA Channel

(1) Execution of DMA cycle
DMA transfer of the CPU DMA channel is requested by read/write with the CPU DMA Data Register, and the DMA cycle is executed.

(2) Procedure for controlling IC from CPU
Described below is the procedure for controlling this IC when DMA transfer of the CPU DMA channel is executed.

- Write the head address of the buffer memory, to which the data is transferred by DMA, into the CPU DMA Address Counter.
- Write “1” into Bit 3 (CPU DMA enable) of DMA Control Register-2 and “0” or “1” into Bit 4 (CPU DMA source) depending on the direction of transfer. (When these are written, the DMA cycle execution commences.)
- In reading data from the buffer memory, Bit 1 (CPU buffer read ready) of the BMM Status Register is set to “1” when the data read from the buffer memory is written into the CPU DMA Data Register. Therefore, first check this status and then read the data from the CPU DMA Data Register. When the data is read from the CPU DMA Data Register, Bit 1 returns to “0" and the CPU DMA Address Register is incremented. When the next data is written into the CPU DMA Data Register from the buffer memory, the Bit is again set to “1”. Check this status and then read the next data from the CPU DMA Data Register.
- In writing data into the buffer memory, first check that Bit 2 (CPU buffer write ready) of the BMM Status Register is “1” and then write the data into the CPU DMA Data Register. Bit 2 (CPU buffer write ready) is set to “0” when the data is written in the CPU DMA Data Register but when this data is written into the buffer memory, it returns to “1” and the CPU DMA Address Register is incremented. Check that Bit 2 is set to “1” again and then write the next data into the CPU DMA Data Register.

4. Host Interfaces

4-1. Overview

The CXD1198AQ can be connected with the Intel 80-series host bus or SCSI control LSI (CXD1185, etc.) as the host interface. The selection can be made by the HMDS pin as follows.

When connecting with the Intel 80-series host bus, input a low logic level to the HMDS pin or leave it open; when connecting with the SCSI control LSI, input a high logic level to the HMDS pin.

Except for the fact that the XTC pin is not supported, the host interface specifications of this IC are the same as those for the CXD1186BQ.

4-2. When connecting with the Intel 80-series host bus

When connecting this IC with the Intel 80-series host bus, input a low logic level to the HMDS pin or leave it open. Fig. 4-1 shows and example of the connection.

(1) Commands/statuses transfer between host and CPU

The host can access each of the four write and read registers using the HA0, HA1, XHCS, XHRD and XHWR pins. The DMA transfer mode is also supported by the WRDATA and RDDATA registers and, regardless of the HA0, HA1 and XHCS pin values, the registers are selected by the XHAC, XHRD and XHWR pins, and DMA transfer is conducted between the host and buffer memory. The Parameter Register and Result Register are 10-byte FIFO registers.

Inputting a low logic level to both the XHAC and XHCS pins is prohibited at the same time.

∗ Write registers

- ♦ Command register (00H)

  The host writes commands into this register. When it does this, and interrupt request is applied from this IC to the CPU. Bit assignment and function attribution is performed by the drive control program.
- ♦ Parameter register (01H)

  The host writes into this register command parameters required for the CPU to execute the commands. This is a 10-byte FIFO register.
- ♦ WRDATA (write data) register (02H)

  This register is for writing data into the buffer memory from the host. Data can be written in either the I/O mode or DMA mode.
- ♦ Control register (03H)

  This register is for the direct control of the hardware in this IC by the host.

Bit 0 to 2 : INTCLR#1 to 3 (interrupt clear #1 to 3)

By writing “1” into any of these bits, the corresponding interrupt status is cleared. These bits automatically return to “0” after the interrupt status interrupt is cleared. So, there is no need to write “0” again.

Bit 3 to 5 : ENINT #1 to 3 (enable interrupt #1 to 3)

By writing “1” into any of these bits, the corresponding interrupt status is enabled. The host can also read the values of these bits from the Status register.

Writing “1" into a bit is prohibited when its corresponding interrupt status is high. Therefore, before writing “1” into any of these bits, the host must read the Status register and check its interrupt status.

Bit 6 : CLRPRM (clear parameter)

The Parameter register can be cleared by writing “1” into this bit. This bit automatically returns to “0” after the Parameter register is cleared. So, there is no need to write “0” again.

Bit 7 : CHPRST (chip reset)

This IC is internally initialized by writing “1” into this bit. This bit automatically returns to “0” upon completion of the initializing. So, there is no need to write “0” again. An interrupt request can be generated to the CPU by writing “1” into this bit.

* Read registers

♦ Status register (00H)

This register is for the host to read the statuses in this IC.

Bit 0 to 2 : INTSTS #1 to 3 (interrupt status #1 to 3)

The values of these bits correspond to that of Bits 0 to 2 in the CPU’s Host Interface Control Register respectively. When each bit is “1”, an interrupt request is generated to the host provided that the corresponding interrupt of the bit is enabled.

Bit 3 to 5 : ENINTST #1 to 3 (enable interrupt status #1 to 3)

The values of these bits correspond to that of Bits 3 to 5 in the control register.

Bit 6 : Data request status

This bit has the same value as the HDRQ pin, and it indicates that the IC has requested the host for buffer memory data transfer. When transferring data in the I/O mode, access the WRDATA or RDDATA registers after the host has checked that this bit is “1”.

Bit 7 : Busy status

This bit is set to “1” by the host writing a command in the Command register. It is set to “0” by the CPU writing “1” into the clear busy bit of the Host Interface Control Register.

♦ Result register (01H)

The host reads the results after the command execution from this register. This is a 10-byte FIFO register.

♦ RDDATA (read data) register (02H)

This register is for the host to read the data from the buffer memory. Data can be read in the I/O mode or DMA mode.

♦ FIFO status register (03H)

This register is for the host to read the status of the parameter register or the host result register.

Bit 0 : Parameter write ready

When this bit is “1”, it indicates that the Parameter register is not full and the host can write parameter data.

Bit 1 : Parameter empty

When this bit is “1”, it indicates that the Parameter register is empty.

Bit 2 : Result read ready

When this bit is “1”, it indicates that the Host Result register is not empty and the host can read result data.

Bit 3 : Result full

When this it is “1”, it indicates that the Host Result register is full.

Bit 4 to 7 : Reserved

Write registers

Command Register (00H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	0

Parameter Register (01H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	0

Write Data Register (02H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	0

Control Register (03H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Chip Reset	Clear FIFO	ENINT #3	ENINT #2	ENINT #1	INTCLR #3	INTCLR #2	INTCLR #2

Read registers

Status Register (00H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Busy Status	Data Request Status	ENINTST #3	ENINTST #2	ENINTST #1	INTSTS #3	INTSTS #2	INTSTS #1

Result Register (01H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	0

Read Data Register (02H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D7	D6	D5	D4	D3	D2	D1	0

FIFO Status Register (03H)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				Result Full	Result Read Ready	Parameter Empty	Parameter Write Ready

(2) Host and CPU control procedure

Fig. 4-2 shows and example of the host and CPU control procedure. In this example, the host gets to know the interrupt status by polling the Status register.

(3) Data transfer between host and buffer memory

This IC contains 2 × 8-bit FIFO registers (WRDATA, RDDATA), and data can be transferred at 4 MB/s maximum.

(3-1) Data transfer in DMA mode

Data is transferred between the host and this IC by means of handshaking using the HDRQ/XSAC and XHAC/SDRQ pins.

The HDRQ/XSAC pin outputs the HDRQ signal requesting data transfer from the IC to the host and the XHAC/SDRQ becomes the corresponding acknowledge signal XHAC.

- ♦ Data transfer from host to buffer memory (host DMA source bit = "1")
  When the host DMA enable bit is "1" while FIFO is not full and the XHAC pin is high, this IC sets the HDRQ pin high. When the acknowledge signal returns from the host, the HDRQ pin is set low. Data from the host is retrieved in this IC at the XHAC pin rising. The data retrieved is written in sequence into the addresses of the buffer memory selected by the Host Address Counter Register.
- ♦ Data transfer from buffer memory to host (host DMA source bit = "0")
  When the host DMA enable bit is "1", the data in the address of the buffer memory selected by the Host Address Counter Register is retrieved in this IC. When the buffer memory data is retrieved, this IC sets the HDRQ pin high if the XHAC pin is "1". When the acknowledge signal returns from the host, the HDRQ pin is set low. While this pin is low, this IC outputs the data retrieved from the buffer memory to host bus HDB0 to 7.

(3-2) Data transfer in the I/O mode

The host can transfer data with the buffer memory by writing or reading the WRDATA or RDDATA registers. In this case, the control of this IC by the CPU is not different from that in the DMA mode. Fig. 4-3 shows the host control flow when data is transferred between the host and buffer memory in the I/O mode.

(3-3) Completion of data transfer

There are two following methods to complete data transfer.

- By using the Host Transfer Counter. (This is the usual method.)
- By setting the host DMA enable bit to "0".

♦ When using the Host Transfer Counter

When transferring data using the Host Transfer Counter, the CPU should perform the following operations prior to the data transfer.

· Write the number of bytes for data transferred into the Host Transfer Counter.
· Write the data transfer direction (host DMA source) and "1" into the host DMA enable bit.
  When these are written, data transfer commences.

The Host Transfer Counter is decremented each time data is written into FIFO. When its value is reduced to zero, further data is not written into FIFO. When all the FIFO data is read out, the host DMA complete status (Interrupt Status Register Bit 2) sets on.

- When the host DMA enable bit is set to “0”
  Data transfer is stopped when the host DMA enable bit is set to “0” during actual transfer. Then the transfer of data between this IC and the host or buffer memory may be suspended so that the values of the Host Address Counter and Host Transfer Counter after suspension cannot be guaranteed.
  In this case, the host DMA complete status does not set on.

(4) Procedure for controlling IC from CPU
Described below is the procedure for controlling this IC when DMA transfer of the host DMA channel is to be executed.

- Write the number of bytes transferred into the Host DMA Transfer Counter.
- Write the head address of the buffer memory, to which the data is transferred by DMA, into the Host DMA Address Counter.
- Write “1” into Bit 0 (host DMA enable) of DMA Control Register-2 and “0” or “1” into Bit 1 (host DMA source), depending on the transfer direction. (When these are written, the DMA cycle execution commences.)
- When the DMA transfer of the number of bytes written into the Host DMA Transfer Counter is completed, Bit 3 (host DMA complete) of the Interrupt Status Register is set to to “1”. Also, the Host DMA Transfer Register is zero, and the Host DMA Address Counter holds the value of the address following the buffer memory address which was last transferred by DMA.

4-3. When connecting this IC with the SCSI control LSI
When connecting this IC to the SCSI control LSI, input a high logic level to the HMDS pin. Fig. 4-4 shows an example of the connections.

(1) Data transfer between SCSI control LSI and buffer memory
Data is transferred between the SCSI control LSI and this IC by means of handshaking using the HDRQ/XSAC and XHAC/SDRQ pins.
The XHAC/SDRQ pin outputs the SDRQ signal requesting data transfer from the SCSI control LSI to this IC, and the HDRQ/XSAC pin becomes the corresponding acknowledge signal XSAC.

- Data transfer from SCSI control LSI to buffer memory (host DMA source bit = “1”)
  When the host DMA enable bit is “1”, and the SDRQ signal is input, this IC outputs a low-level signal from the XSAC pin provided that FIFO is not full. The data is retrieved in this IC at the XHWR pin rising. The data retrieved is written in sequence into the addresses of the buffer memory selected by the host address counter.
- Data transfer from buffer memory to SCSI control LSI (host DMA source bit = “0”)
  When the host DMA enable bit is “1”, the data in the address of the buffer memory selected by the Host Address Counter is retrieved in this IC. When, with the buffer memory data retrieved, the SDRQ signal X is input, this IC outputs a low-level signal from the XSAC pin and, while this pin is low, the IC outputs the data retrieved from the buffer memory to host bus HDB0 to 7.

(2) Completion of data transfer

For details on how to complete the data transfer, refer to section “(3-3) Completion of data transfer” on the previous page.

(3) Procedure for controlling IC from CPU

When data is to be transferred between the SCSI control LSI and buffer memory, the procedure for controlling this IC from the CPU is the same as for the Intel 80-series host bus described in the previous section. Refer to “(4) Procedure for controlling IC from CPU” in the previous section.

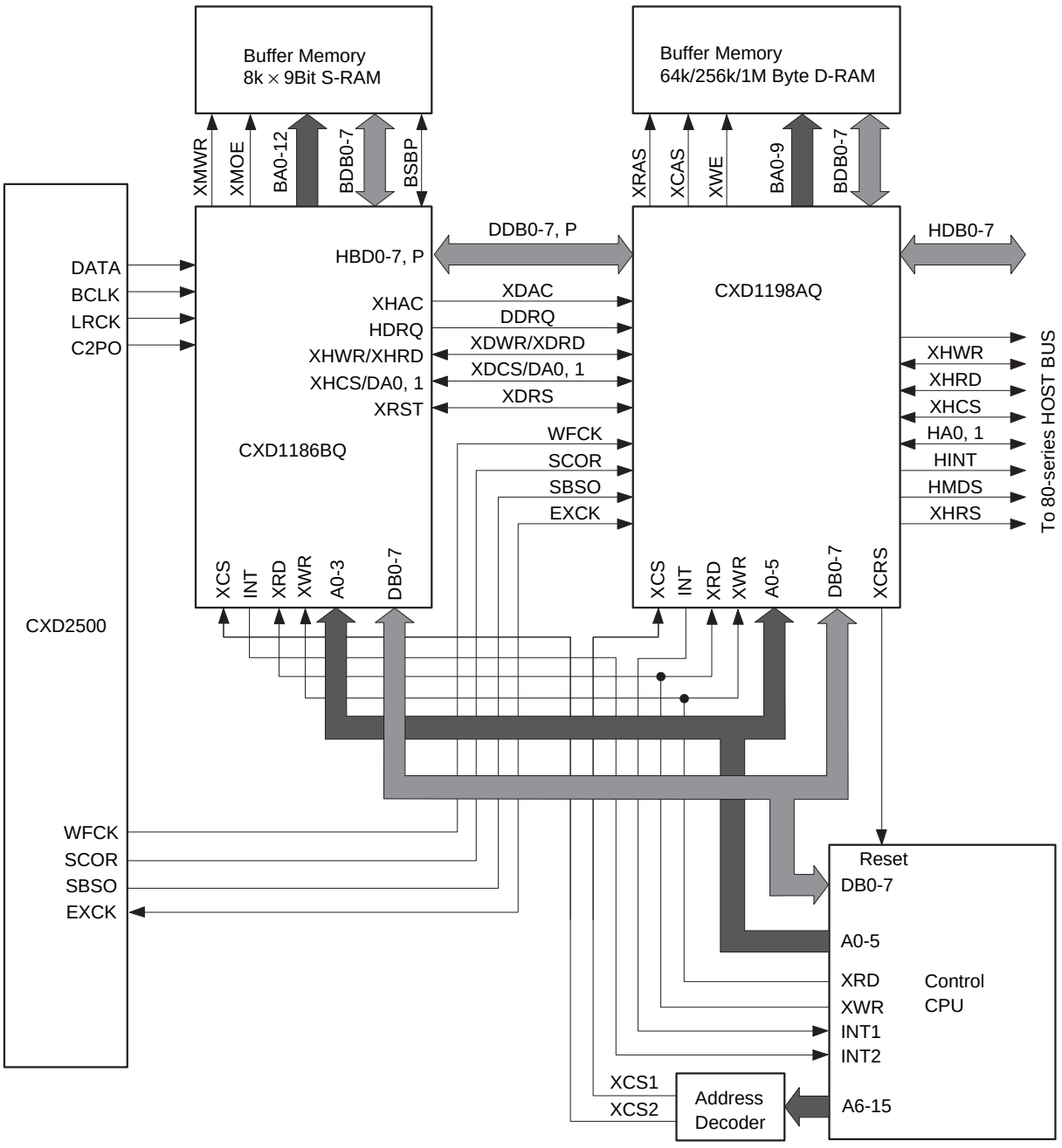


Fig. 4-1 Example of connection with Intel 80-series host bus

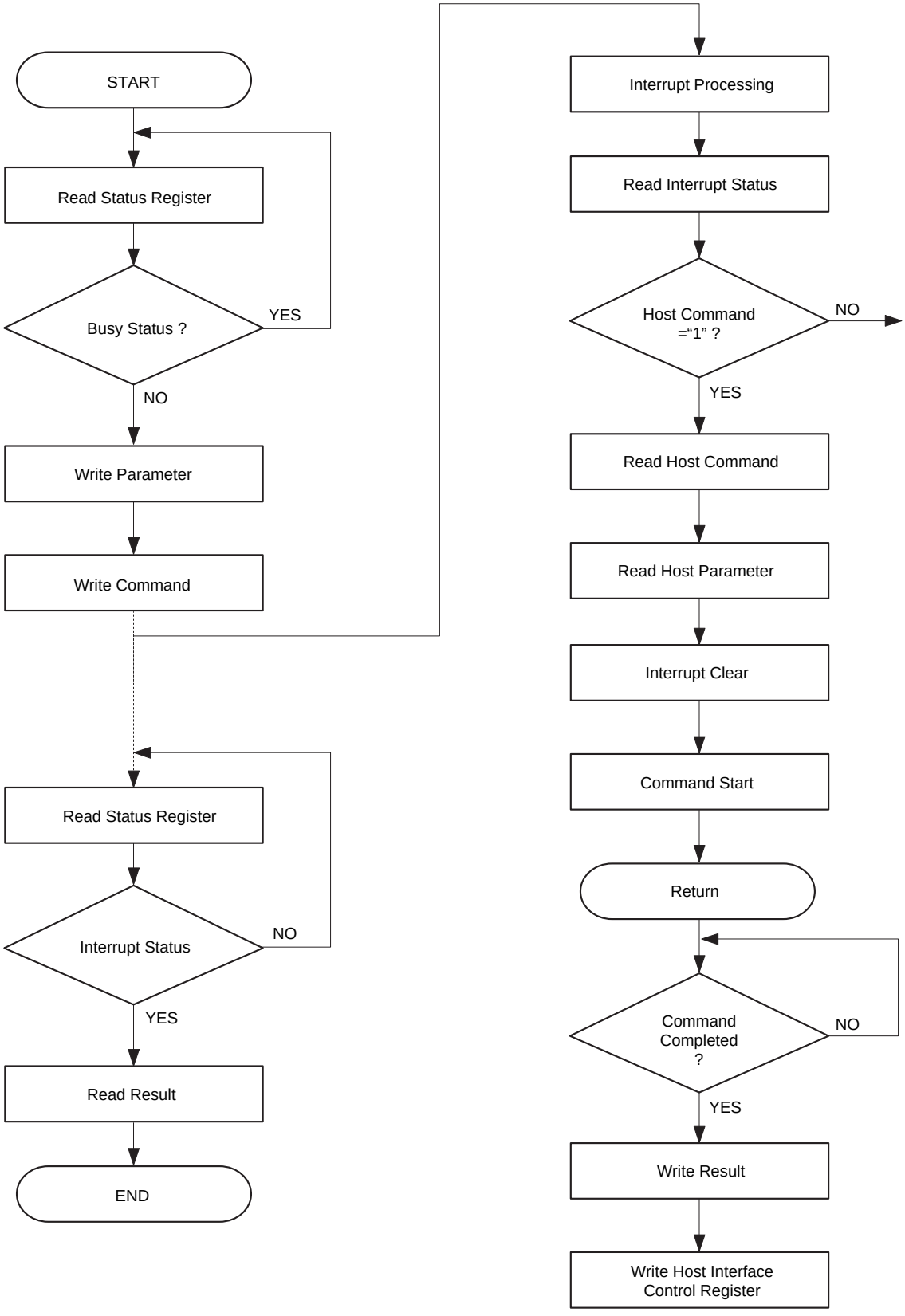


Fig. 4-2 Example of commands/statuses transfer between host and CPU

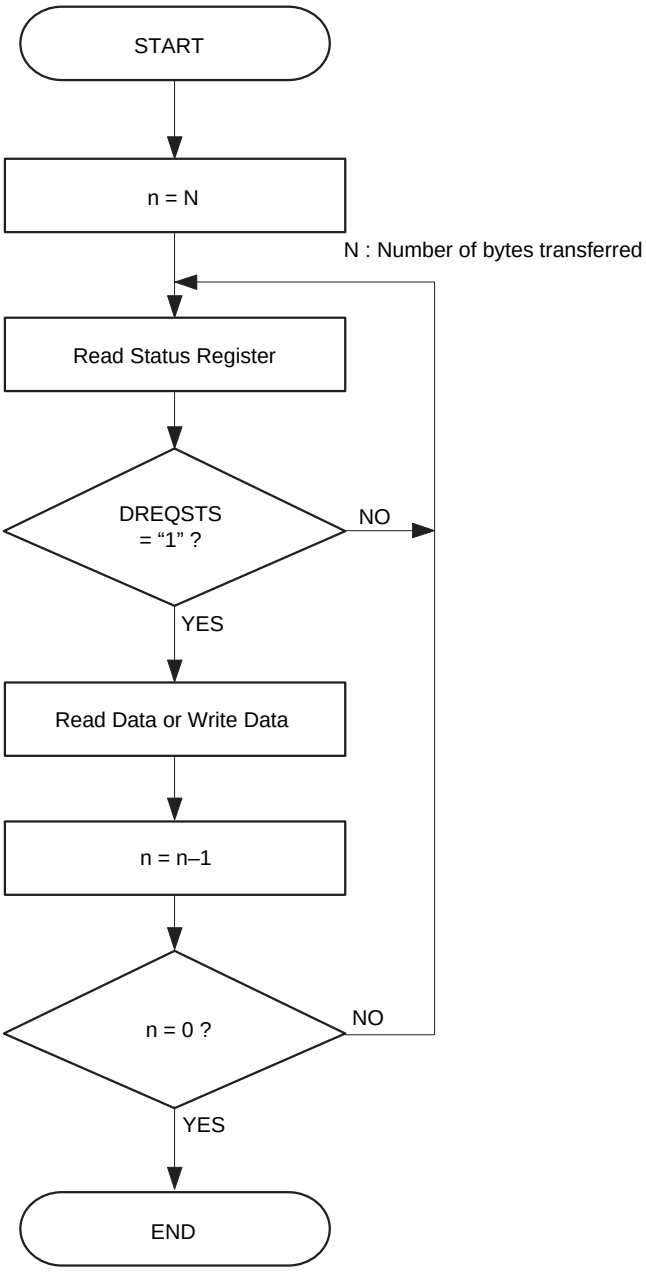
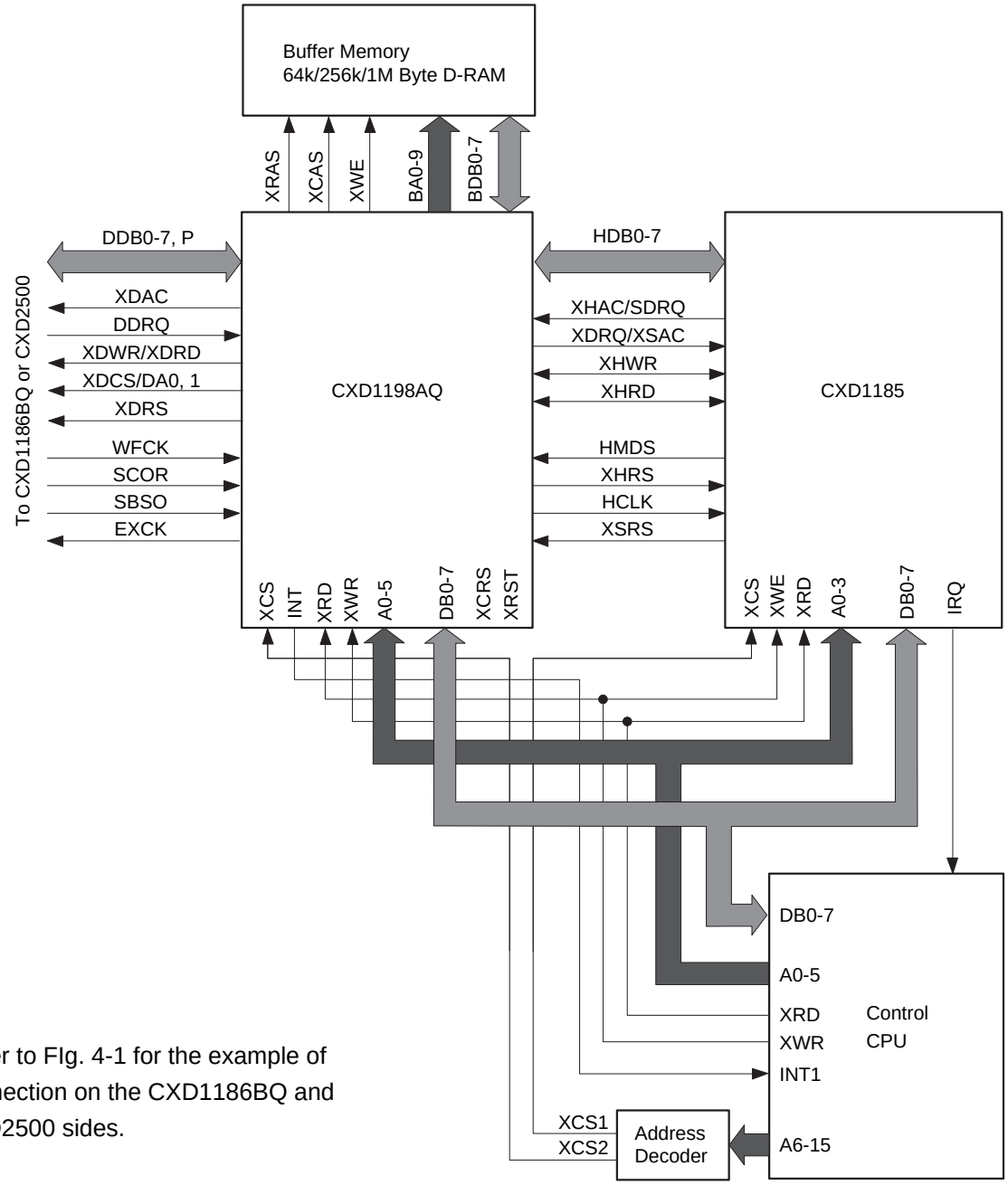


Fig. 4-3 Example of data transfer control in I/O mode

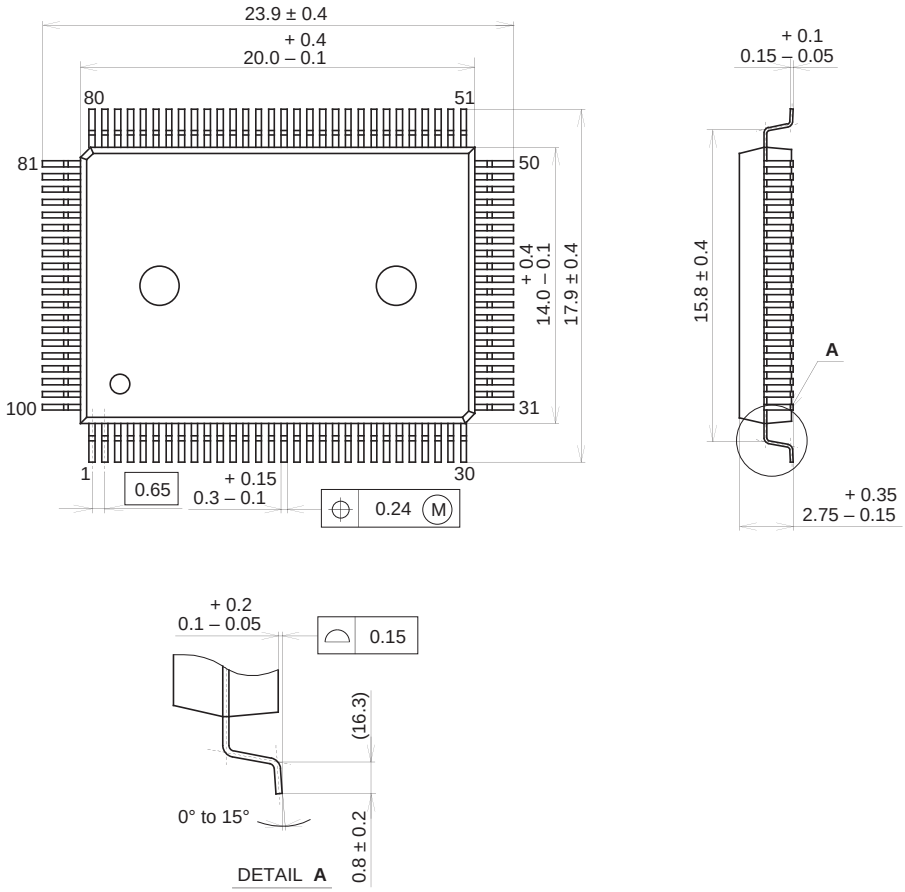


Refer to FIg. 4-1 for the example of connection on the CXD1186BQ and CXD2500 sides.

Fig. 4-4 Example of connection with SCSI control LSI

Package Outline Unit : mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g