HFC0300

Variable Off Time Controller

The Future of Analog IC Technology

DESCRIPTION

HFC0300 is a variable off-time controller that uses a fixed-peak–current technique to decrease its frequency as the load lightens. As a result, it offers excellent efficiency at light-load while optimizing the efficiency under other load conditions.

When the frequency decreases to threshold, the peak current decreases with the decreasing load to prevent mechanical resonance in the transformer. The controller enters burst mode when the output power falls below a given level.

The HFC0300 features various protections such as thermal shutdown, V_{CC} under-voltage lockout, overload protection, short-circuit protection, and over-voltage protection.

The HFC0300 is available in SOIC-7 package.

FEATURES

- Variable Off-Time, Current Mode Control
- Universal Main Supply Operation (85VAC to 265VAC)
- Frequency Foldback as Load Lightens
- Peak-Current Compression to Reduce Transformer Noise
- Active-Burst Mode for Low Standby Power Consumption
- Internal High-Voltage Current Source
- Internal 200ns Leading Edge Blanking
- Thermal Shutdown (Auto Restart with Hysteresis)
- VCC Under-Voltage Lockout with Hysteresis
- Over-Voltage Protection on VCC Pin
- Timer-Based Overload Protection
- Short-Circuit Protection
- Natural Spectrum Shaping for Improved EMI Performance

APPLICATIONS

- Battery Charger for Portable Electronics
- Standby Power Supply
- Switched-Mode Power Supplies

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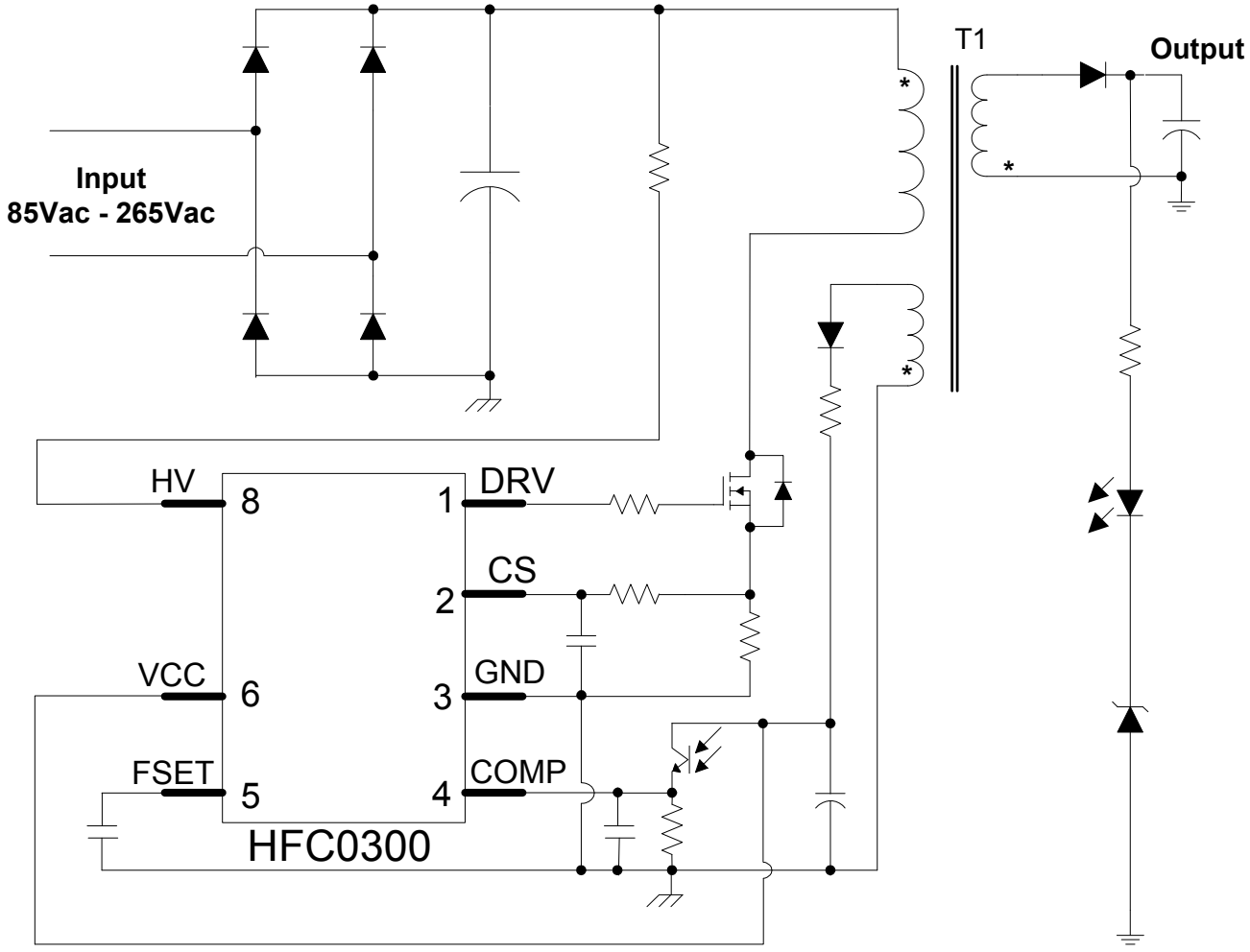
TYPICAL APPLICAION



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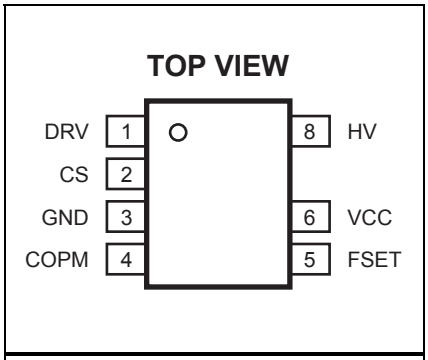
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
HFC0300HS	SOIC-7	HFC0300	-40°C to +125°C

For Tape & Reel, add suffix –Z (e.g. HFC0300HS–Z);
For RoHS compliant packaging, add suffix –LF (e.g. HFC0300HS–LF–Z)

PACKAGE REFERENCE



SOIC-7

ABSOLUTE MAXIMUM RATINGS (1)

HV Breakdown Voltage..... -0.7V to +700V
VCC, DRV to GND.....-0.3V to +30V
DRV to GND .....-0.3V to +18V
FSET, COMP, CS to GND.....-0.3V to +7V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC-7.....1.3W
Junction Temperature.....150°C
Thermal Shut Down .....150°C
Thermal Shut Down Hysteresis .....25°C
Lead Temperature .....260°C
Storage Temperature ..... -60°C to +150°C
ESD Capability Human Body Model (All Pins except Drain) 2.0kV
ESD Capability Machine Model 200V

Recommended Operation Conditions (3)

Maximum Junction Temp. (T_J)..... +125°C
Operating Vcc range.....8.2V to 20V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC-7	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-up Current Source (Pin HV)						
Supply Current from Pin HV	I_{HV}	V_{HV}=400V, Vcc=6V		2		mA
Break-Down Voltage	V_{BR}		700			V
Off-State HV Leakage Current	I_{Leak}	V_{HV}=400V, Vcc=10V		10	17	µA
Supply Voltage Management (Pin VCC)						
VCC Increasing Level where the Current Source Turns Off	VCC_{OFF}		10.7	11.7	12.7	V
VCC Decreasing Level where the Current Source Turns On	VCC_{ON}		7.6	8.2	8.8	V
Vcc Re-Charge Level where Protections Occurs	V_{CCR}		5.0	5.5	6.0	V
VCC Decreasing Level where Latch-Off Phase Ends	VCC_{latch}			3.0		V
Internal IC Consumption ,1nF Load on DRV Pin	Icc	fs=65kHz, Vcc=12V		1.3		mA
Internal IC Consumption, Latch off Phase	Icc_{latch}	Vcc=6V		500		µA
Rising Voltage Threshold on VCC where Controller Latches Off (OVP)	V_{OVP}		22.5	24	25.5	V
Integration Time Constraint on the OVP Comparator	t_{INT}			20		µs
Timing Capacitor(Pin FSET)						
Minimum Voltage on FSET Capacitor	$V_{FSETmin}$		0.82	0.88	0.94	V
Maximum Voltage on FSET Capacitor	$V_{FSETmax}$			3.2		V
Source Current	I_{FSET}		23	28	33	µA
FSET Capacitor Discharge Time (Active at Drive Turn-On)	t_{DISCH}			0.6		µs
Feedback Management (Pin COMP)						
Over Load Protection Set Point	V_{OLP}		0.80	0.85	0.90	V
Over Load Protection Delay Time	t_{OLP}	C_{FSET}=330pF		74		ms
COMP Decreasing Level where the Controller Enters the Burst Mode	V_{BURH}		3.0	3.2	3.4	V
COMP Increasing Level where the Controller Leaves the Burst Mode	V_{BURL}		2.9	3.1	3.3	V
Current Sampling Management (Pin CS)						
Short-Circuit Comparator Leading-Edge Blanking	t_{LEB1}			150		ns
Current-Sense Comparator Leading-Edge Blanking	t_{LEB2}			200		ns
Maximum Current-Sense Comparator Limit	V_{Limit}	V_{COMP}=1V	0.45	0.5	-0.55	V
Short-Circuit Protection Point	V_{SCP}	V_{SCP}		1.0		V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC}=12V, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Driving Signal (Pin DRV)						
Sourcing Resistor	R_H			10		Ω
Sinking Resistor	R_L			3		Ω
V_{DRIVE} Clamp	V_{DRIVE}	Vcc=18V		13.7		V

PIN FUNCTIONS

SOIC-7 Pin #	Name	Description
1	DRV	Drive. Output of the drive signal.
2	CS	Current Sense Input.
3	GND	Ground.
4	COMP	Switching Frequency Set. A feedback voltage of 0.85V will trigger overload protection, and a feedback voltage of 3.1V will trigger a burst mode operation.
5	FSET	Frequency Set. Maximum switching frequency set by a capacitor.
6	VCC	IC Supply. Connected to an external bulk capacitor. If an auxiliary winding brings this pin above 24V, the controller latches off.
8	HV	High-Voltage Source. Input for the start-up high voltage current source.

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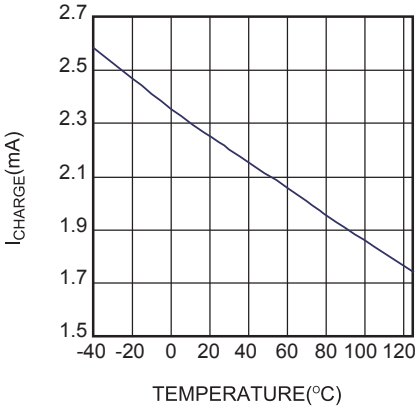
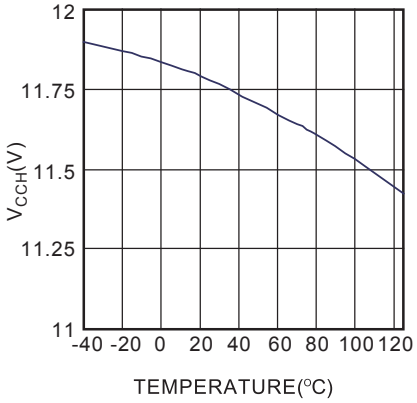
TYPICAL PERFORMANCE CHARACTERISTICS

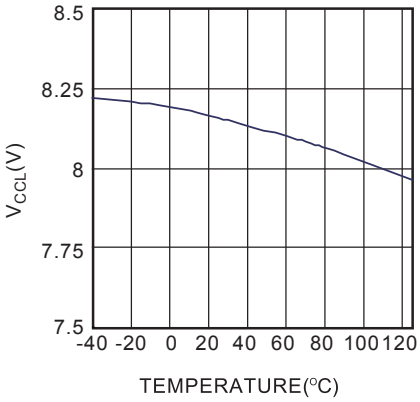
Charge Current from Pin HV (V_{CC}=6V,V_{HV}=400V) vs. Temperature



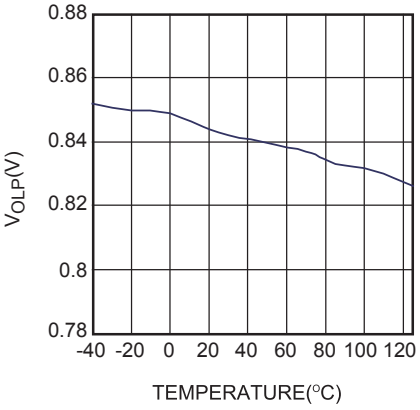
V_{CC} Upper Level at which the Internal High Voltage Current Source stops vs. Temperature



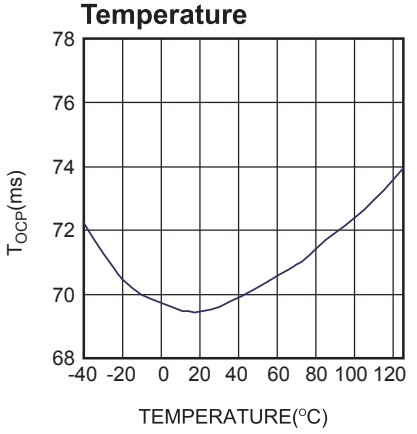
V_{CC} Lower Level at which the Internal High Voltage Current Source Triggers vs. Temperature



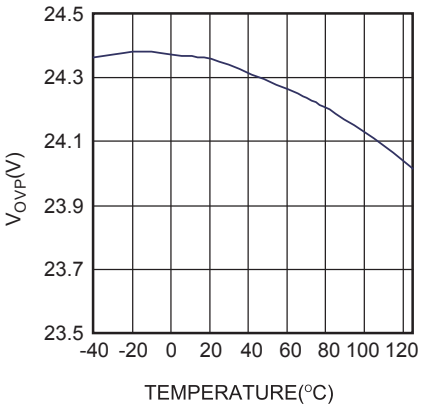
Over Load Set Point vs. Temperature



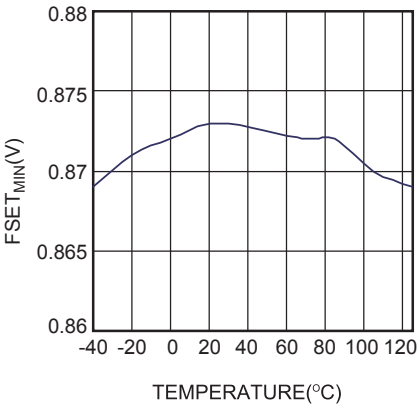
Over Load Delay Time @C_{FSET}=330pF vs. Temperature



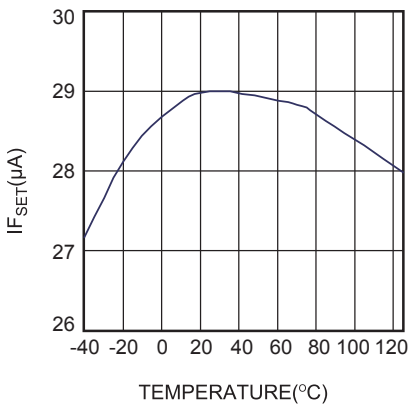
OVP Point vs. Temperature



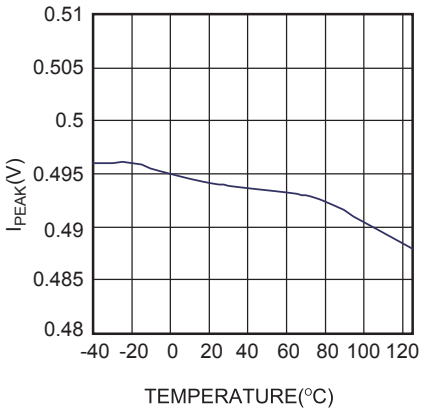
Pin FSET Minimum Voltage vs. Temperature



Pin Fset Source Current vs. Temperature



Pin CS Maximum Peak Current vs.Temperature



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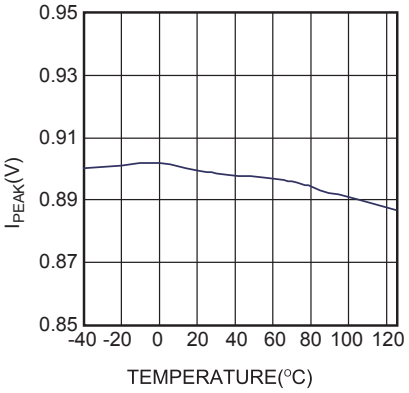
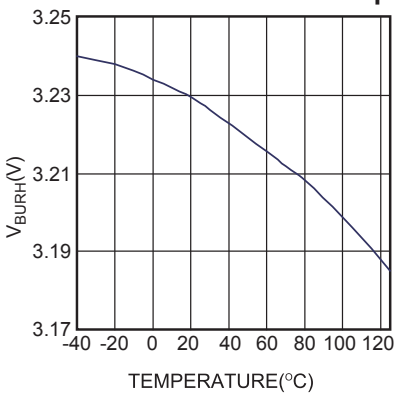
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

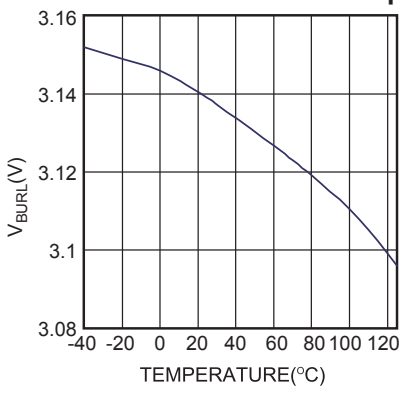
SCP Point vs. Temperature



Comp Increasing Level at which the Controller Enters the Burst Mode vs. Temperature



Comp Decreasing Level at which the Controller Leaves the Burst Mode vs. Temperature



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BLOCK DIAGRAM

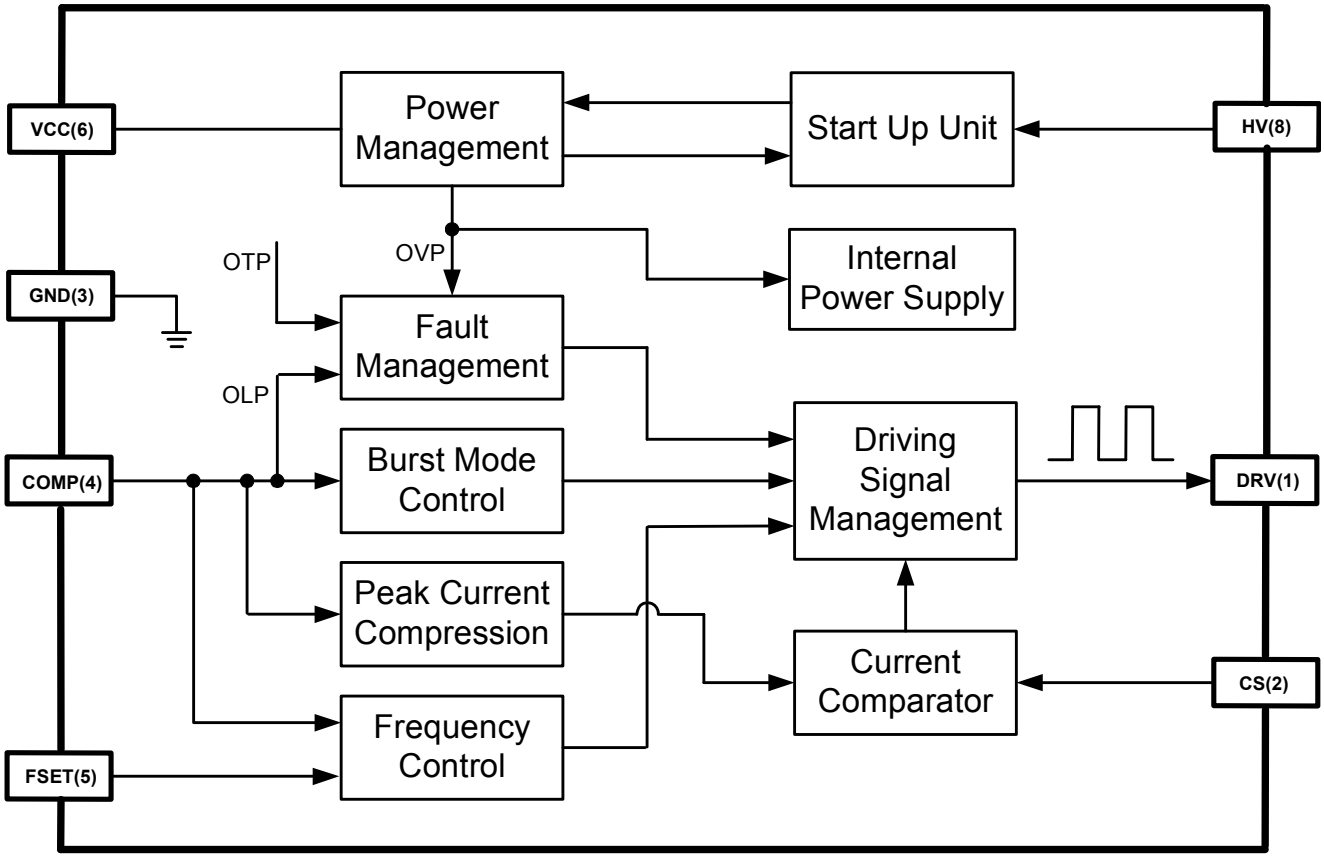

Figure 1: Functional Block Diagram

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OPERATION

The HFC0300 incorporates all the necessary features to build a reliable Switched-Mode Power Supply (SMPS). Its high level of integration requires few external components. Based on a fixed peak current technique, the controller decreases its frequency with the decreasing load to minimize switching loss. When the output power falls below a given level, the controller enters burst mode. It also has better EMI performance because the switching frequency varies with the natural bulk ripple voltage.

Frequency Foldback

A capacitor connected to the FSET pin sets the frequency at the end of charging. This capacitor charges from a constant current source and its voltage is compared with an internal threshold fixed by COMP voltage (see Figure 2). When this capacitor voltage reaches threshold, the capacitor discharges rapidly down to 0V, and a new period starts after a 0.6μs delay (see Figure 3).

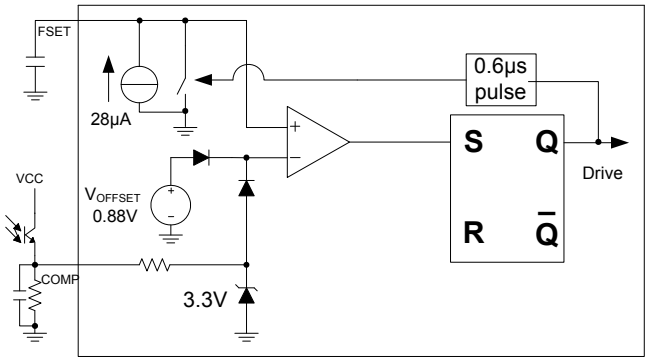

Figure 2: Voltage-Controlled Oscillation

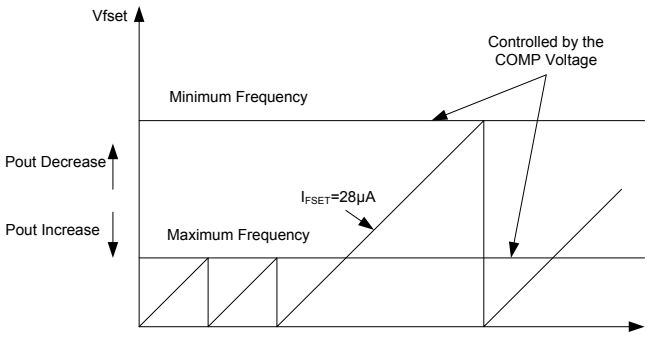

Figure 3: COMP-Voltage–Adjusted Switching Frequency

Start-up and Under Voltage Lock-out

Initially, the internal high voltage current source drawn from the high-voltage (HV) pin powers the IC. The IC starts switching and the internal high-voltage current source turns off as soon as the voltage on VCC reaches 11.7V. Then the auxiliary winding of the transformer supplies the IC before the VCC voltage falls back below 8.2V. Otherwise, the switching pulse stops and the high-voltage current source turns on again.

Figure 4 shows the typical waveform with VCC under-voltage lockout (UVLO).

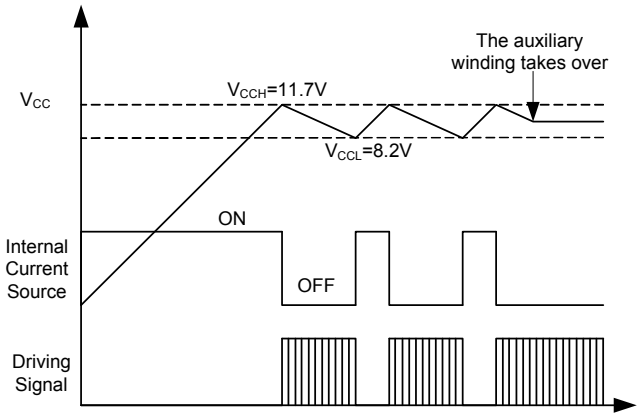

Figure 4: VCC Under-Voltage Lockout

The lower threshold of VCC UVLO goes from 8.2V to 5.5V when fault conditions happen, such as over-load protection (OLP), over-voltage protection (OVP), and over-temperature protection (OTP).

Over-Voltage Protection

By monitoring the VCC pin with a 20μs time-constant filter, the HFC0300 goes into latched fault condition whenever an over-voltage condition occurs—if VCC goes above 24V, typically. The controller stays fully latched in this position until the VCC is cycled down to 3.0V, e.g. when the user unplugs the power supply from the main input and re-plugs it.

Over-Load Protection

In a flyback converter, the maximum output power is limited by the maximum switching frequency and primary peak current. As the primary peak current is constant, the maximum power is limited by maximum frequency. When the switching frequency reaches the maximum,

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the output voltage decreases if the load continues to increase. COMP then drops below the over-load protection (OLP) point because feedback is equivalent to an open circuit.

By continuously monitoring the COMP, when the COMP voltage drops below 0.85V—which is considered an error—the timer starts counting. If the error flag is removed, the timer resets. If the timer reaches completion at the delay time determined by the FSET capacitor (for example, 74ms at C_{FSET}=330pF), OLP takes place. This timer avoids triggering OLP when the power supply is at start-up or load transition phase. Therefore the power supply should start-up in less than over load protection delay time, as determined by the following equation:

$$t_{delay} \approx 74ms \times \frac{C_{FSET}}{330pF}$$

Short Circuit Protection

The HFC0300 shuts down when the CS voltage rises higher than 1V using short-circuit protection (SCP). As soon as the fault disappears, the power supply resumes operation. During SCP, the VCC UVLO lower threshold goes from 8.2V to 5.5V.

Thermal Shutdown

The HFC0300 shuts down switching when the inner temperature exceeds 150°C to prevent damaging high temperatures. As soon as the inner temperature drops below 125°C, the power supply resumes operation. During the thermal shutdown (TSD), the VCC UVLO lower threshold goes from 8.2V to 5.5V.

Peak current compression

As the load becomes lighter, the frequency decreases and may enter the audible range. To avoid exciting mechanical resonances in the transformer and generating acoustic noise, the HFC0300 reduces the peak current as power goes down and thus reduces noise issues.

Figure 5 shows the curve of peak current versus COMP.

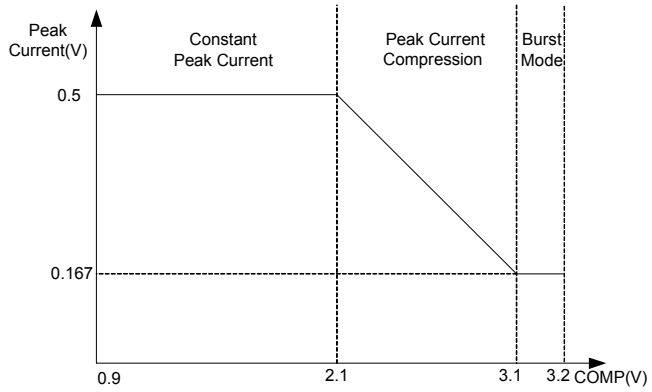

Figure 5: Peak Current vs. COMP

Burst Operation

The HFC0300 enters burst-mode operation to minimize power dissipation in no load or light load conditions. As the load decreases, the COMP voltage increases; The IC stops switching when the COMP voltage increases over the threshold, V_{BRUH} = 3.2V. The output voltage then drops, which causes the COMP voltage to decrease further. Once the COMP voltage falls below the threshold V_{BRUL} = 3.1V, switching resumes and the COMP voltage then oscillates. The burst mode operation alternately enables and disables switching cycle of the MOSFET.

Leading-Edge Blanking

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) unit is employed between the CS pin and the current comparator input. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure 6 shows the leading-edge blanking.

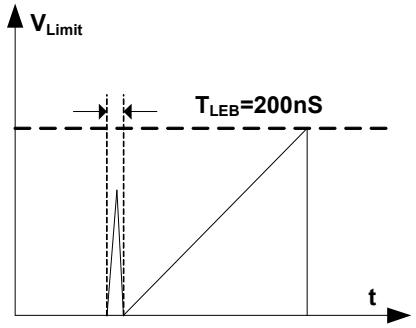

Figure 6: Leading-Edge Blanking

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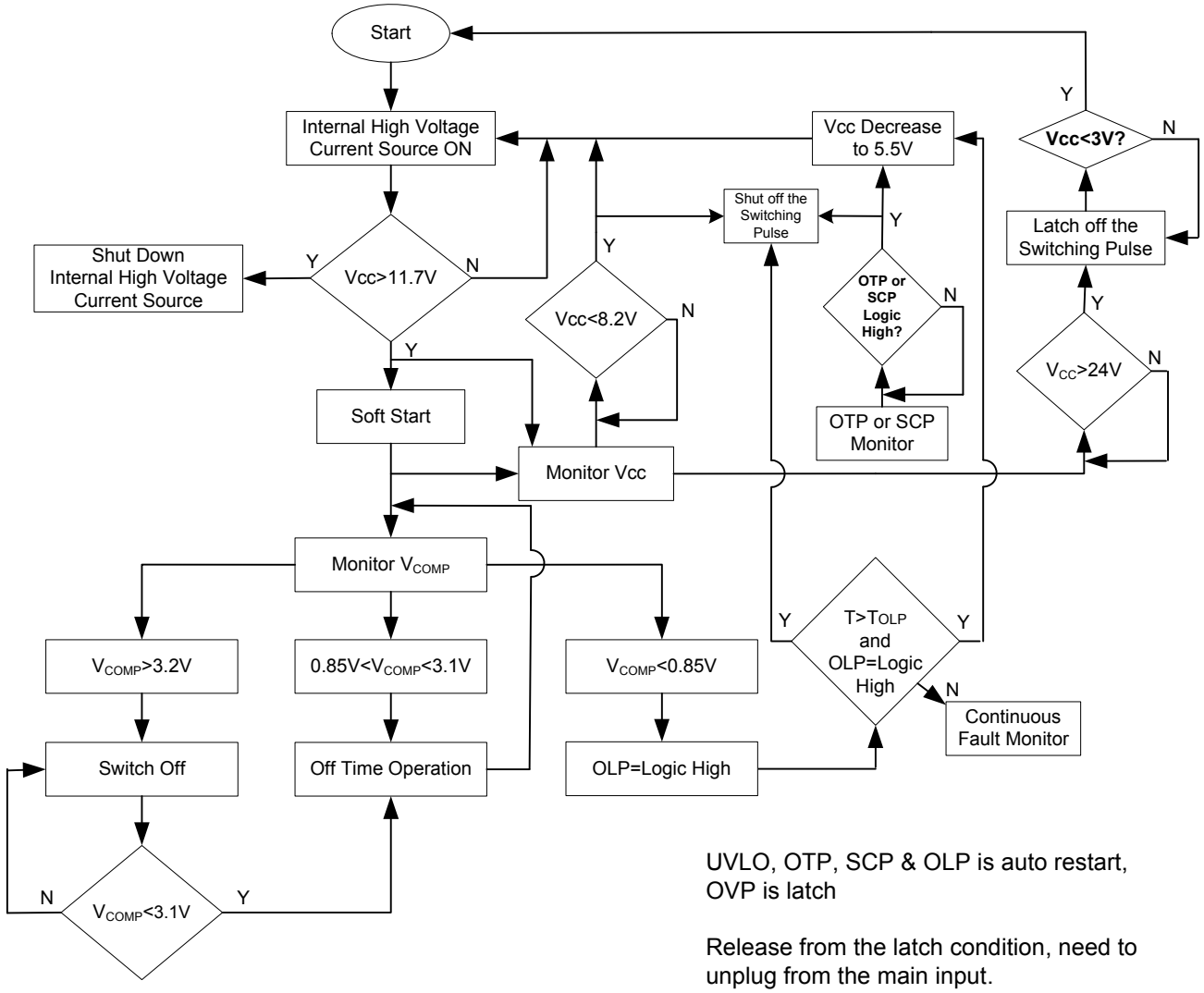

Figure 7: Control Flow Chart

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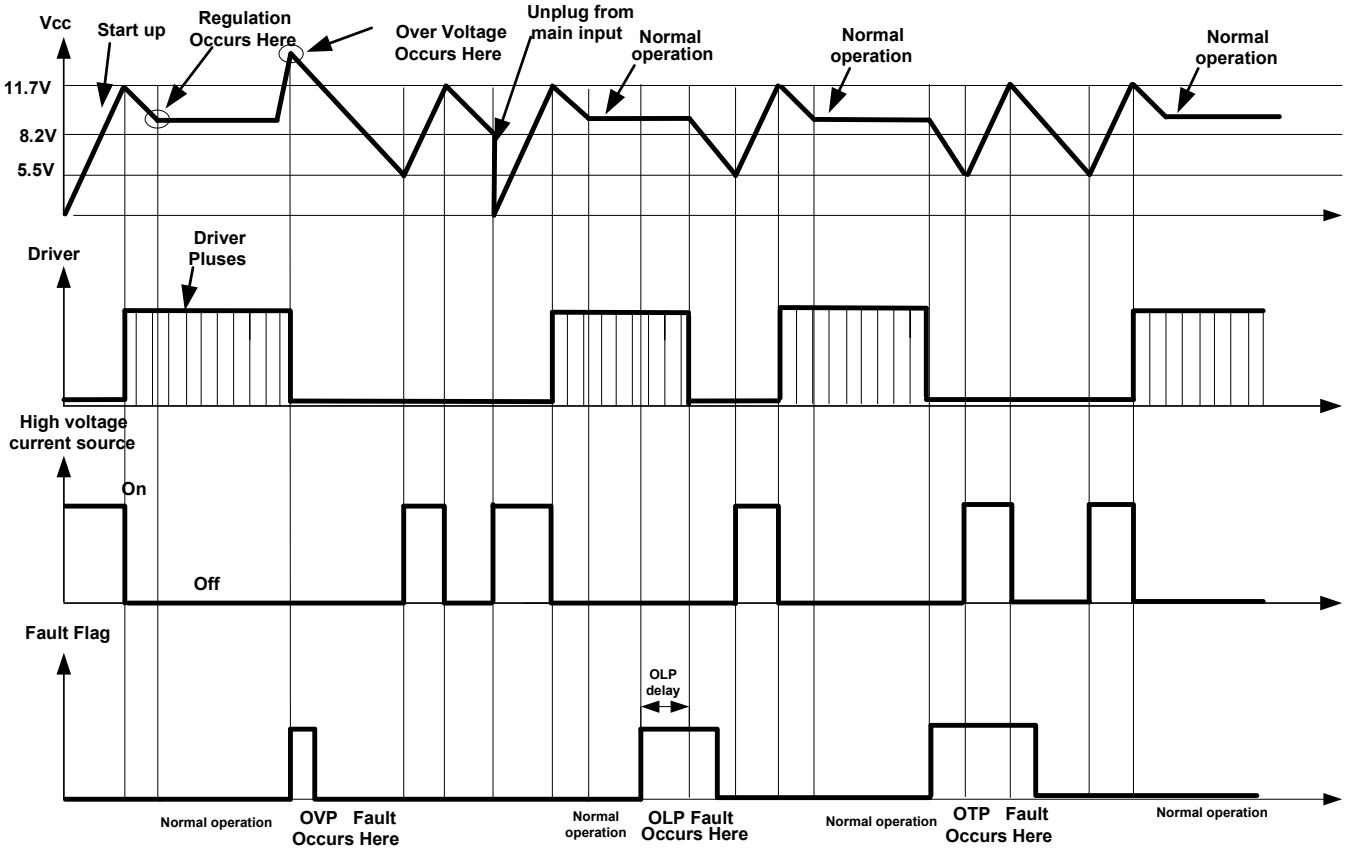

Figure 8: Signal Changes in the Presence of Different Faults

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APPLICATION INFORMATION

Design Keys of HFC0300

Current Sense Resistor Section

The peak current level is internally set to 0.5V, so the current-sense resistor sets the primary-side peak current, which determines the operation mode of the converter—such as CCM, BCM or DCM. If power supply is designed to operate at BCM at low-line input, it will operate at DCM at the high line and the same load condition. The magnetizing inductor current (reflected on the primary side) and the drain-source voltage (V_{DS}) of the primary MOSFET is shown in Figure 9.

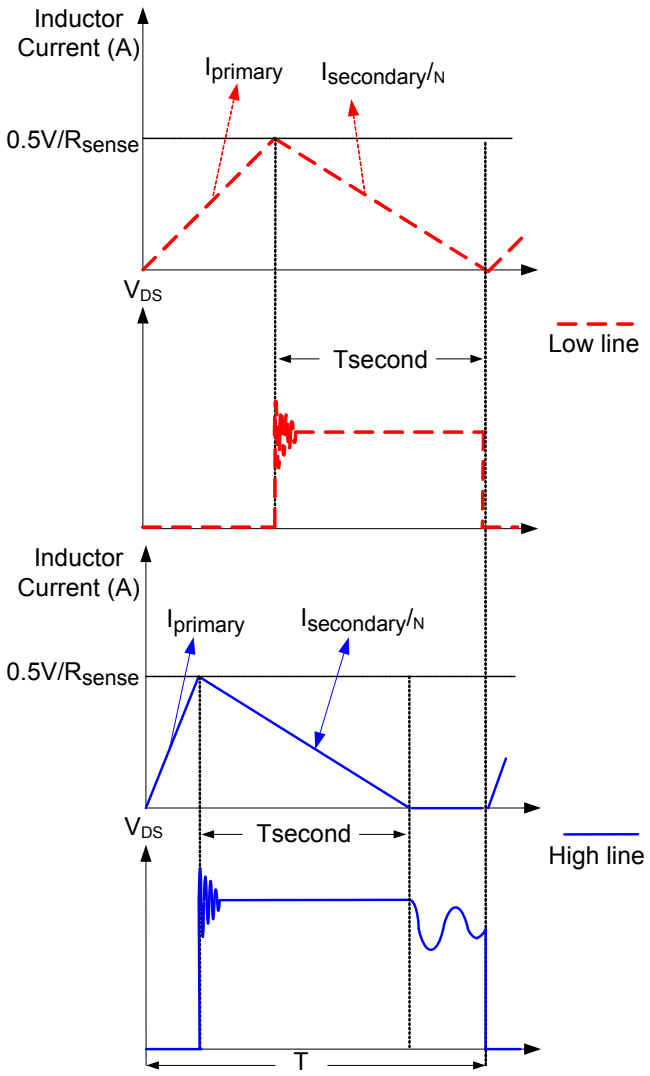

Figure 9: Inductor Current and Voltage of Primary MOSFET

The time duration of the secondary current can be determined by equation (1):

$$t_{sec} = \frac{L_m \times I_{peak}}{N \times V_o} \quad (1)$$

Where L_m is the primary magnetizing inductance, I_{peak} is the primary peak current, and N is the turn ratio of the transformer. I_{peak} remains the same at under different inputs and with the same output, so the time duration of secondary current is the same.

The switching period can be calculated by:

$$t = \frac{N \times I_{peak} \times t_{sec}}{2 \times I_o} \quad (2)$$

From equation (2), the switching period remains the same at different inputs with the same output condition. Since the primary-side switch ON time decreases with the increasing input voltage, then the higher the input line voltage, the deeper discontinuous current mode (DCM) it will enter. Usually, the parameters are designed for the minimum input condition to guarantee that the converter can deliver the required maximum output power.

Since N is pre-determined, if the power supply is designed to operate at boundary current mode (BCM) at the low line, the peak current can be calculated as:

$$I_{peak_BCM} = \frac{2 \times I_o}{N \times (1-D)} \quad (3)$$

Where D is the duty ratio of the switching. Then:

$$D = \frac{(V_o + V_F) \times N}{V_{in} + (V_o + V_F) \times N} \quad (4)$$

If the peak current set by the current-sense resistor is larger than I_{peak_BCM}, the power supply will enter DCM. On the other hand, if the peak current set by current sense resistor is less than I_{peak_BCM}, the power supply will enter CCM, as shown as Figure 10. Here, we define K_{depth} as the depth of CCM.

$$K_{depth} = \frac{I_{valley}}{I_{peak}} \quad (5)$$

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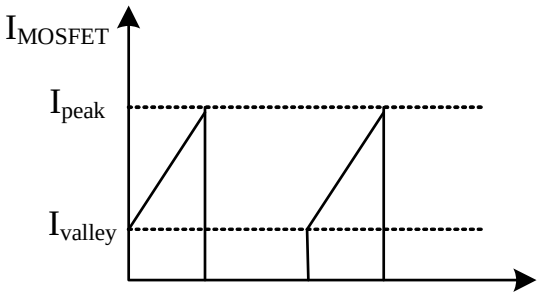

Figure 10: Primary Current at CCM

So the peak current can be determined as:

$$I_{peak_CCM} = \frac{2 \times I_o}{(1-D) \times (1+K_{depth}) \times N} \quad (6)$$

Usually, BCM is preferable at power levels below 40W, and CCM is preferable at power levels higher than 40W: The higher the power delivered, the deeper the CCM adopted for higher efficiency and better thermal performance at full load. For example, for a 90W power supply, K_{depth} should be around 0.5.

The converter operation mode must be determined with each power supply specification given; i.e. determine the K_{depth}. I_{peak} and I_{valley} as calculated by equations (3) through (6). Select the current sense resistor using equation (7).

$$R_{sense} = \frac{V_{peak}}{I_{peak}} \quad (7)$$

Where V_{peak} is the peak voltage threshold of the current resistor; a constant 0.5V for HFC0300.

Chose the current resistor with the proper power rating based on the power loss given in equation (8)

$$P_{sense} = [(\frac{I_{peak} + I_{valley}}{2})^2 + \frac{1}{12} \times (I_{peak} - I_{valley})^2] \times D \times R_{sense} \quad (8)$$

Design of C_{FSET} and OLP Function

The capacitor C_{FSET} sets the maximum frequency as shown in equation (9). This capacitor is charged by a constant-current source shortly after the primary side switch turns on (about 0.6μs delay), and its voltage is compared with the COMP voltage from feedback loop (see Figure 11).

When the capacitor voltage reaches threshold, the capacitor rapidly discharges down to 0V, and a new period starts. An internal delay of about 0.6μs delay before C_{FSET} charges again fully discharges the voltage at the FSET pin, (see Figure 12). Thus the switching frequency is regulated by the feedback loop like a voltage-controlled oscillation (VCO).

$$C_{FSET} = \frac{28uA \times (\frac{1}{f_{max}} - 0.6us)}{0.88V} \quad (9)$$

Where f_{max} is the maximum frequency set by the capacitor connected to FSET pin.

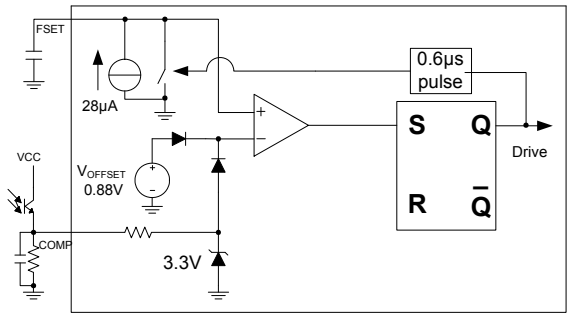

Figure 11: Schematic for Voltage-Controlled Oscillation

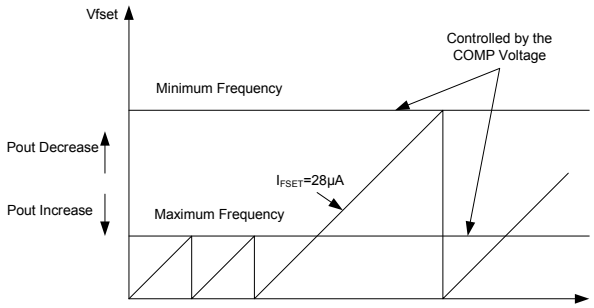

Figure 12: Switching Frequency as Adjusted by COMP Voltage

As described in the section above, the switching frequency reaches its maximum at low line and full load. This frequency, defined as f_s (65kHz in this case). Set the maximum frequency (f_{max}) at 110% f_s. The frequency increases with the increasing output power. When the frequency reaches its maximum—set by C_{FSET}—the over-power limit drops the output voltage, saturating COMP, and drops the OLP threshold (0.85V).

The OLP uses a unique digital timer method: When COMP is less than 0.85V and raises an error flag, the timer starts counting. If the error flag is removed, the timer resets. If the timer overflows after reaching 6000, OLP triggers. This timer duration avoids triggering the OLP when

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the power supply is at start-up or load transition phase. Therefore, set the output voltage in less than 6000 switching cycles during start-up.

Ramp Compensation Circuit

If the power supply operates in CCM and the duty cycle is larger than 0.5, add a ramp compensation circuit to avoid harmonics in peak current mode control. Usually, the ramp compensation rate is selected as per equation (10)

$$k = \alpha \times \frac{V_O \times N \times R_{sense}}{L_m} \quad (10)$$

Where:

- α is the coefficient which is usually 0.5 to 1.0
- R_{sense} is the value of primary sense resistor

For applications using the HFC0300, use the ramp compensation circuit shown in Figure 13 .

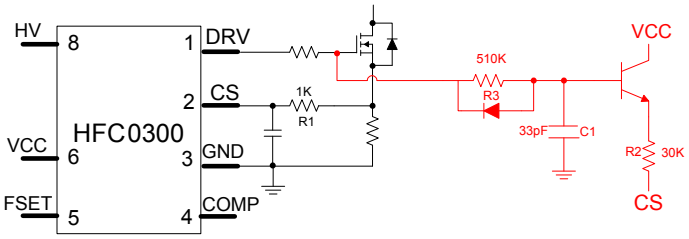

Figure 13: Ramp Compensation Circuit

Equation (11) estimates the compensation rate of the above circuit :

$$k \approx \frac{V_{DRV}}{\tau} * \frac{R_1}{R_2} \quad (11)$$

Where V_{DRV} is the drive voltage

$$\tau = R_3 * C_1$$

Select τ to be larger than the switching period so that the ramp is approximately linear.

Design Summary

Figure 14 shows a detailed reference design of the off-time controlled flyback converter using the HFC0300. The input voltage is 90VAC to 265VAC and the output is 24V/1.5A.

The transformer used in this design has a turn ratio of 84:14:8 (N_p: N_s: N_{aux}) with a primary inductance of 818μH. The core is EE25. Figure 15, Figure 16, and Table 1 Winding Ordershow wiring schematics.

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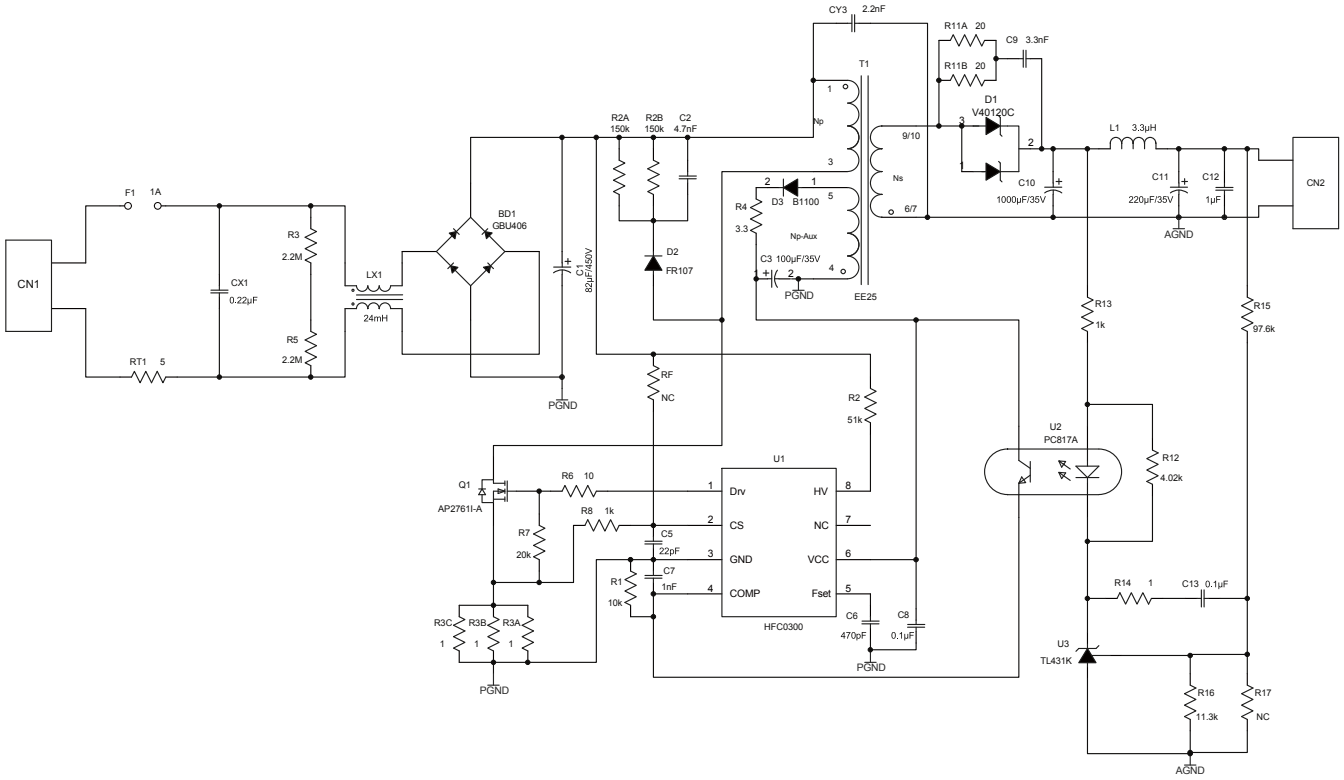

Figure 14: Schematic of Off-Time Flyback Converter with HFC0300

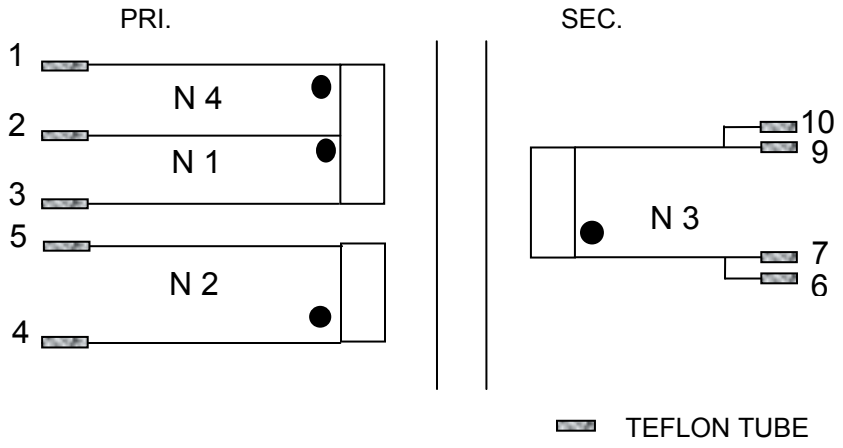

Figure 15: Connection Diagram

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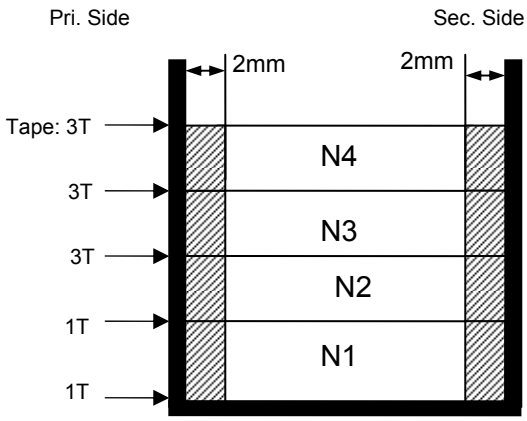

Figure 16: Winding Diagram

Table 1 Winding Order

Tape(T)	Winding	Edge Tape (Pri.)	Terminal (start-end)	Edge Tape (Sec.)	Wire size (φ)	Turns (T)
1	N1	2mm	3->2	2mm	0.3mm*1	42
1	N2	2mm	5->4	2mm	0.2mm*1	8
3	N3	2mm	9,10->6,7	2mm	0.3mm*5	14
3	N4	2mm	2->1	2mm	0.3mm*1	42
3						

Experimental Verification

A physical prototype based on Figure 13 was used to verify both the design procedure presented in this application note, and the performance. The input ranged between 90VAC and 265VAC, and the output was at 24V/1.5A. The converter operates in BCM at 90VAC input and full load. Figure 17 and Figure 18 the current and drain voltage waveforms of the primary MOSFET. Figure 19 shows the burst mode function of the controller at light load.

To minimize power dissipation at no load or light load, the HFC0300 enters burst-mode operation. As the load decreases, the COMP voltage increases. The HF0300 skips switching cycles when the COMP voltage increases over the threshold V_{BURH} = 3.2V. The output voltage drops, causing the COMP voltage to decrease again.

Once the COMP voltage falls below the threshold V_{BURL} = 3.1V, switching resumes. The COMP voltage then rings. The burst mode operation alternately enables and disables switching cycles of the MOSFET thereby reducing switching loss in the no load or light load conditions.

Figure 20 shows over-load protection. When COMP is low, the controller stops switching after 6000 switching cycles (about 100ms for this application)

Figure 21 shows the measured efficiency. From the efficiency curve, the efficiency is still high at light load condition due to decreased switching frequency. Also the power consumption at no load is given in Table 2. In burst mode, the power loss with no load is very small, even with high line input.

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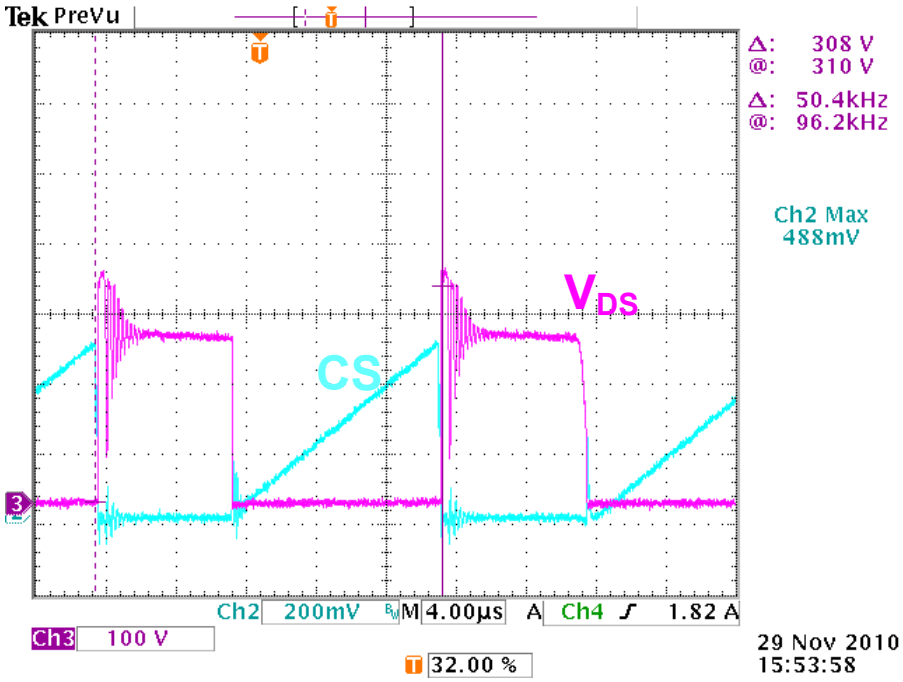

Figure 17: Drain Current and Voltage of MOSFET at Low-Line Input (90VAC); CH2 - CS, CH3, V_{DS}

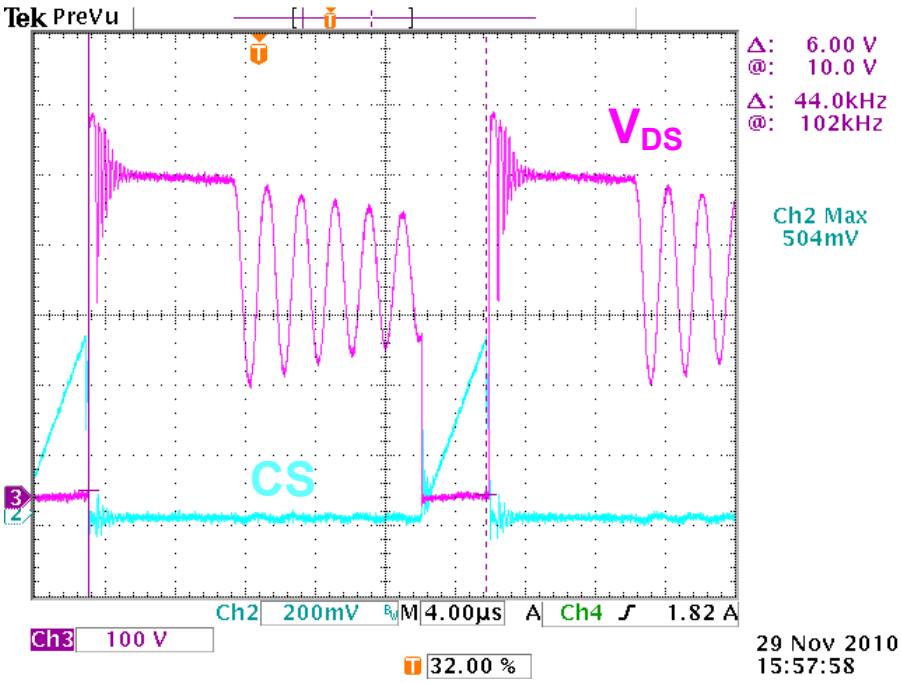

Figure 18: Drain Current and Voltage of MOSFET at High-Line Input (230VAC); CS2 - CS, CH3 - V_{DS}

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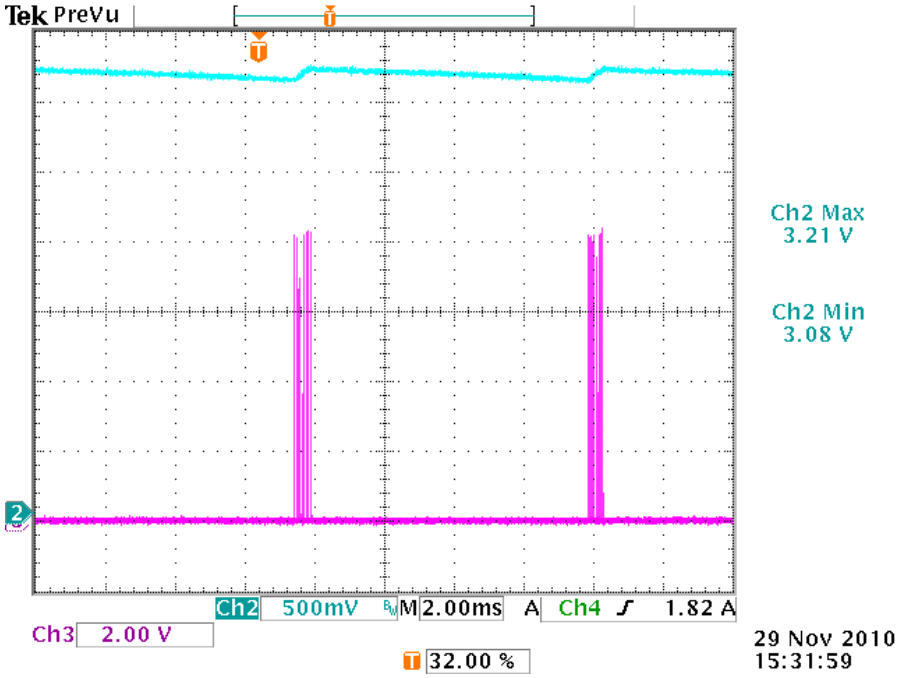

Figure 19: Burst Mode; CH2 - COMP, CH3 - DRV

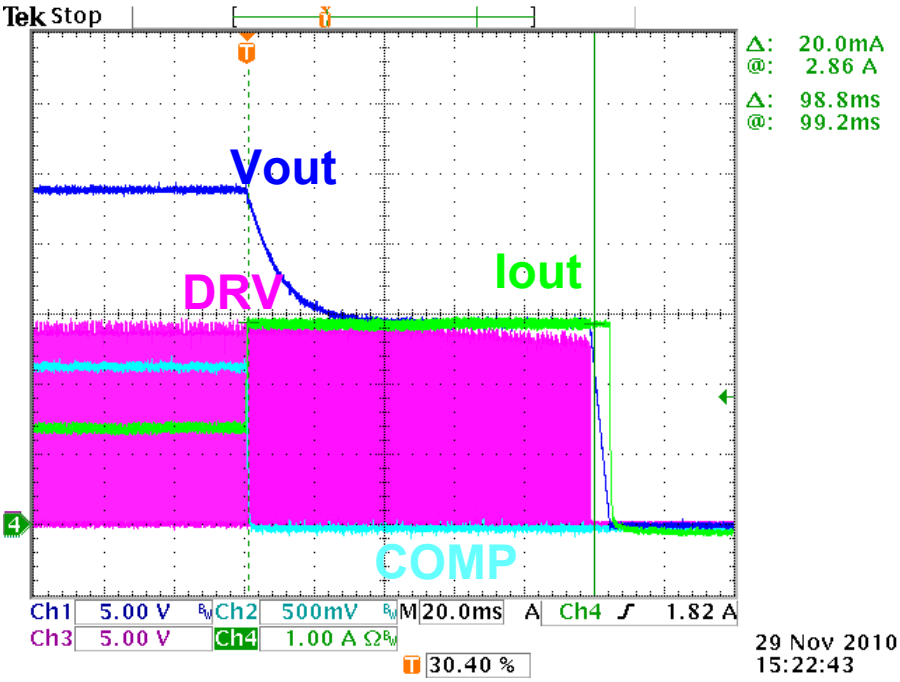

Figure 20: Overload Protection; CH1 - V_{OUT}, CH2 - DRV, CH4 - I_{OUT}

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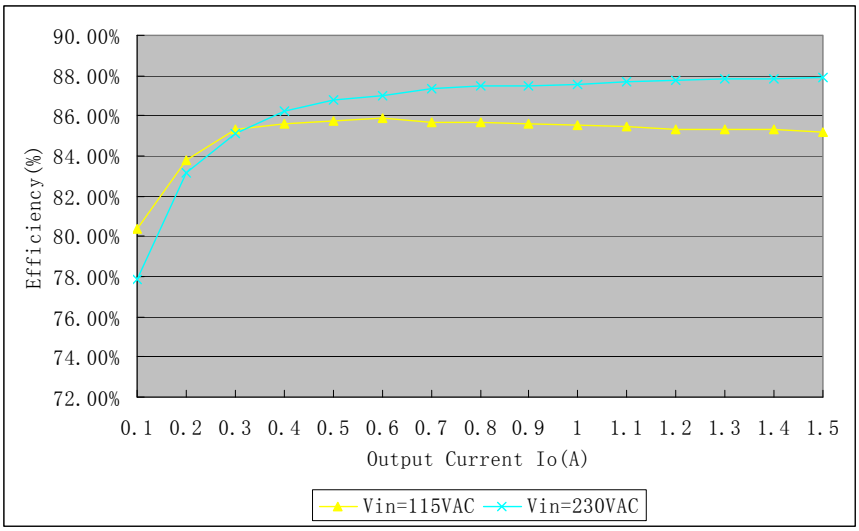

Figure 21: Measured Efficiency

Table 2: No-Load Loss at Different Line Voltages

Input voltage (V_{AC}, RMS)	90	115	230	265
Power loss (mW)	74.4	77.2	110.1	121.9

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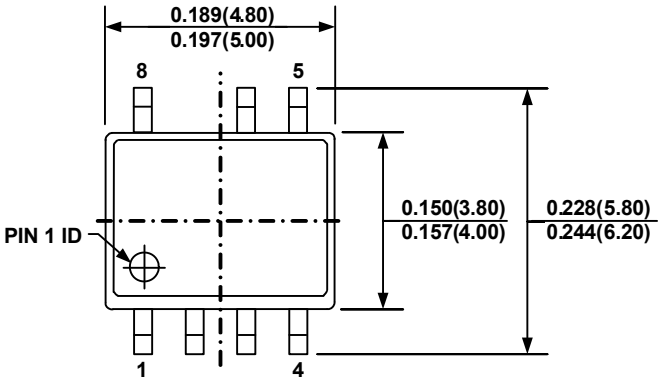
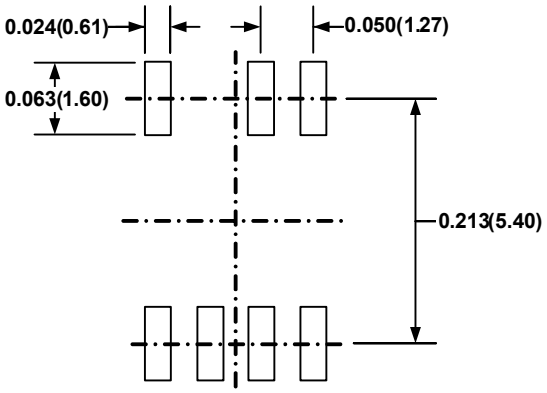
PACKAGE INFORMATION

SOIC-7



TOP VIEW



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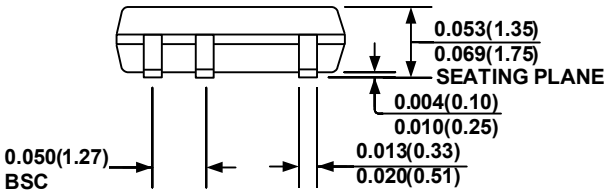
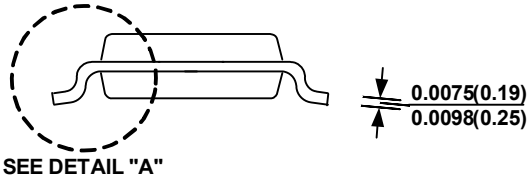
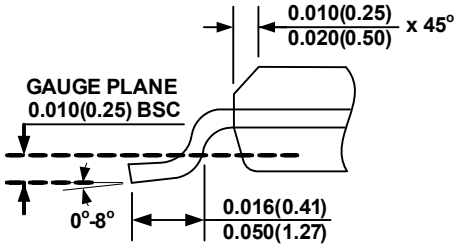


FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE

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