OVERVIEW

The SM8212B is a POCSAG-standard (Post Office Code Standardization Advisory Group) signal processor LSI, which conforms to CCIR recommendation 584 concerning standard international wireless calling codes.

The SM8212B supports call messages in either tone, numerical or character outputs at signal speeds of 512, 1200 or 2400 bps. The signal input stage features a built-in filter.

Each of the addresses (max. 8) can be assigned to any frame, which also makes the device configurable for many additional services. Each address can be independently set ON/OFF.

Furthermore, built-in buffer memory means decoded information can be fetched in sync with the microcontroller clock, thereby reducing the microcontroller CPU time required.

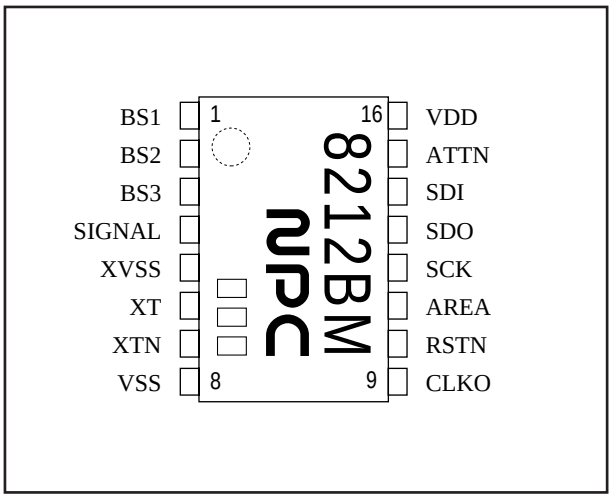
Intermittent-duty method (battery saving (BS) method) control signals, compatible with PLL operation, and Molybdenum-gate CMOS structure makes possible the construction of low-voltage operation, low power dissipation systems.

The SM8212B is available in 16-pin SSOPs.

FEATURES

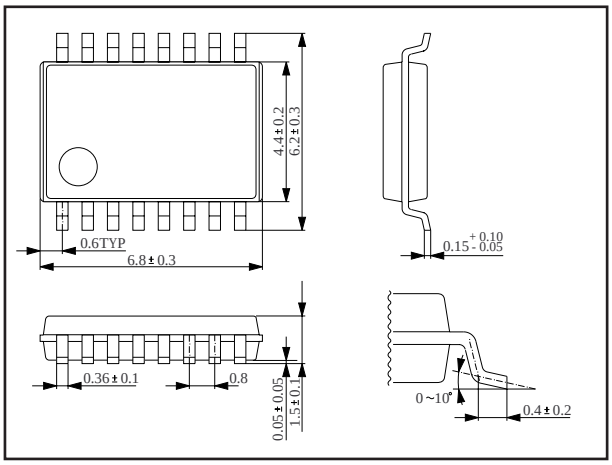
- Conforms to POCSAG standard for pagers
- 512, 1200 or 2400 bps signal speed
- Multiframe compatible (each address individually controllable)
- 8 addresses × 4 sub-address (total of 32 addresses) control
- Built-in buffer memory
- Supports tone, numeric or character call messages
- Built-in input signal filter, with filter ON/OFF and 4 selectable filter characteristics
- PLL-compatible battery saving method (BS1, BS2, BS3 outputs)
- BS1 (RF control main output signal) 61-step setup time setting
- BS3 (PLL setup signal) 61-step setup time setting
- BS2 (RF DC-level adjustment signal) before/during reception selectable adjustment timing
- 1-bit and 2-bit burst error auto-correction function
- 25 to 75% duty factor signal coverage
- 8 rate error detection condition settings
- 76.8 kHz system clock (crystal oscillator)
- 76.8 or 38.4 kHz clock output pin
- Built-in oscillator capacitor and feedback resistor
- 2.0 to 3.5 V operating supply voltage
- Molybdenum-gate CMOS process realizes low power dissipation
- 16-pin SSOP

PINOUTS (16-pin SSOP)

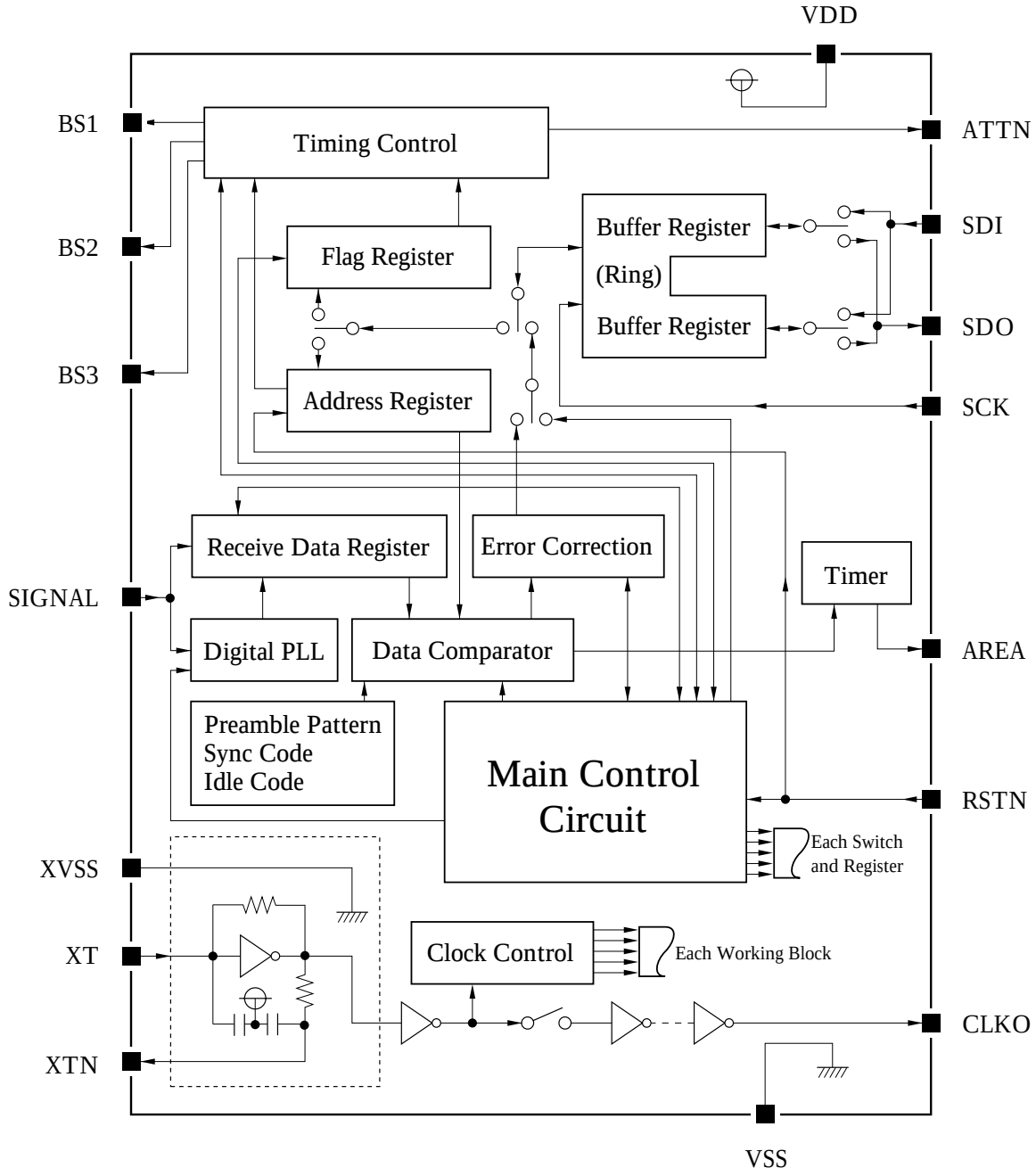


PACKAGE DIMENSIONS (Unit: mm)

16-pin SSOP (SM8212BM)



BLOCK DIAGRAM

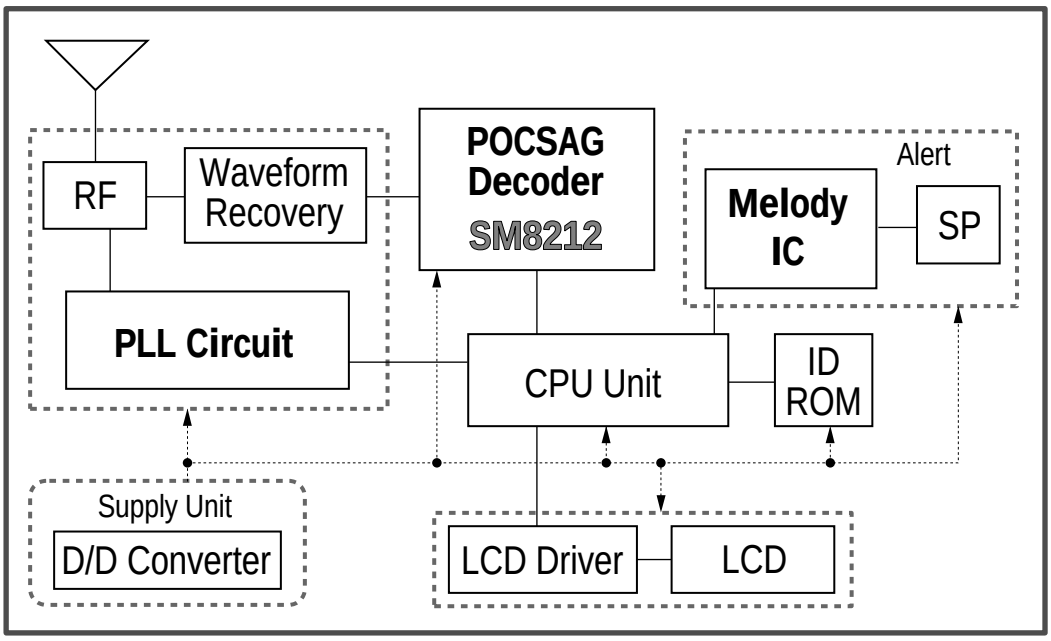


PIN DESCRIPTION

Pin number	Pin name	i/o	Description
1	BS1	o	RF control main output signal
2	BS2	o	RF DC-level adjustment signal
3	BS3	o	PLL setup signal
4	SIGNAL	i	NRZ signal input pin
5	XVSS	-	Crystal oscillator ground. Capacitor connected between XVSS and VDD
6	XT	i	Oscillator input pin
7	XTN	o	Oscillator output pin
8	VSS	-	Ground
9	CLKO	o	76.8 or 38.4 kHz clock output
10	RSTN	i	Hardware clear (reset)
11	AREA	o	Sync code detection output (HIGH for minimum 1 sec. on detection)
12	SCK	i	CPU-to-decoder data transfer sync clock
13	SDO	o	Status and received data output to CPU
14	SDI	i	Data input from CPU (including ID data)
15	ATTN	o	Interrupt detect signal output pin (Ready for data transmission when LOW)
16	VDD	-	Supply voltage

i = Input, o = Output

SM8212B Paging Receiver Block Diagram



SPECIFICATIONS

Absolute Maximum Ratings

(V_{SS}=0V)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		-0.3 to 7.0	V
Input voltage range	V_{IN}		V_{SS}-0.3 to V_{DD}+0.3	V
Storage temperature range	T_{STG}		-40 to 125	°C
Power dissipation	P_W		250	mW
Soldering temperature	T_{SLD}		255	°C
Soldering time	t_{SLD}		10	sec.

Recommended Operating Conditions

(V_{SS}=0V)

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Supply voltage	V_{DD}		2.0	-	3.5	V
Operating temperature	T_{OPR}		-20		70	°C

DC Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter	Pin	Symbol	Condition	Rating			Unit
				MIN	TYP	MAX	
Operating current consumption (IDLE mode)	VDD	I_{DD1}	V_{DD}=3.0V (Note1)		3.0	6.0	µA
			V_{DD}=2.0V (Note 1)		2.0	4.0	
Standby supply current	VDD	I_{DD2}	V_{DD}=3.0V (Note 2)		2.0	4.0	µA
			V_{DD}=2.0V (Note 2)		1.5	3.0	
Input voltage	All input pins	V_{IH}		0.8*V_{DD}			V
		V_{IL}				0.2*V_{DD}	
Output current	All outputs except XTN	I_{OH}	V_{OH}=2.6V, V_{DD}=3.0V	0.6	1.4		mA
		I_{OL}	V_{OL}=0.4V, V_{DD}=3.0V	1.0	2.2		
Output current	All outputs except XTN	I_{OH}	V_{OH}=1.6V, V_{DD}=2.0V	0.3	0.7		mA
		I_{OL}	V_{OL}=0.4V, V_{DD}=2.0V	0.7	1.5		

(Note 1) When killed CLKO output

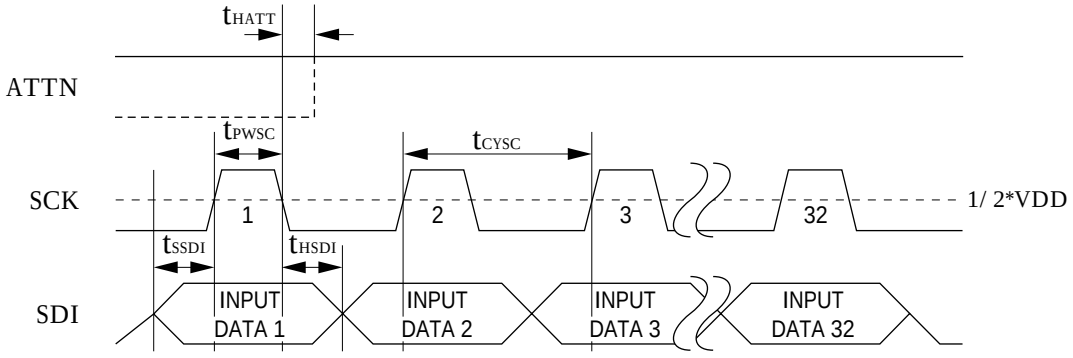
(Note 2) Oscillator circuit is working

The consumption current is slightly higher when RSTN is going LOW.

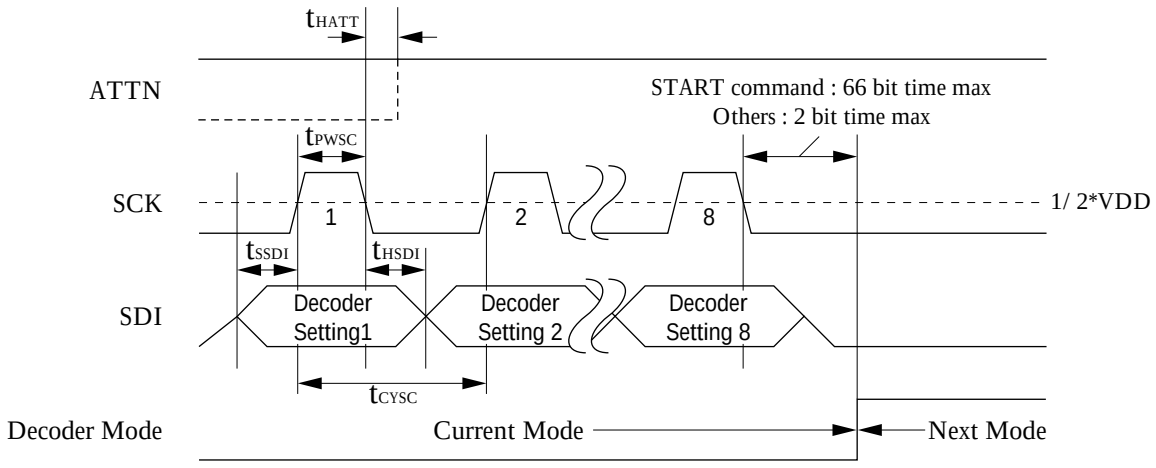
AC Characteristics

(Recommended operating conditions unless otherwise noted)

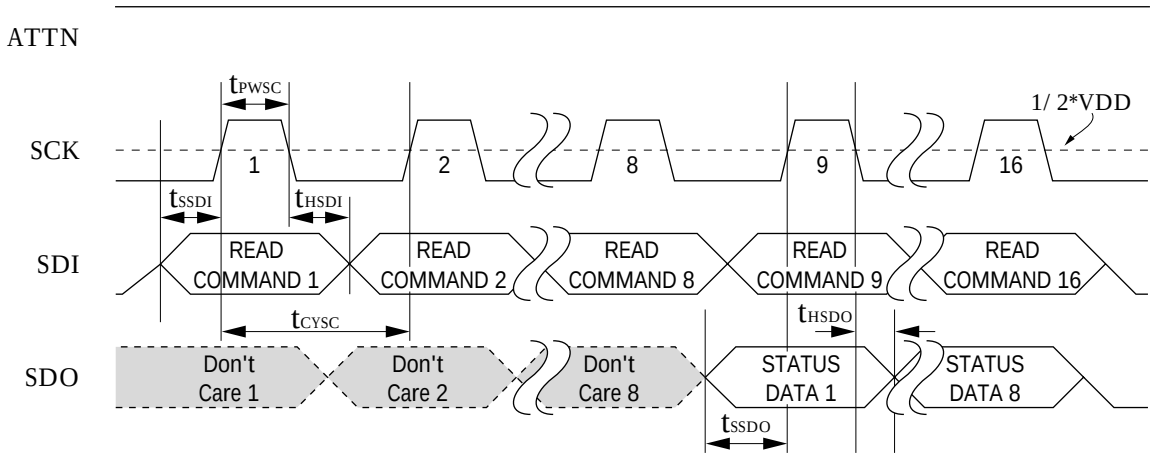
Parameter	Symbol	Rating MIN	Rating TYP	Rating MAX	Unit	Condition
XT clock frequency	f_{CYXT}	-250ppm	76.8	+250ppm	kHz	
XT clock duty cycle	D_{XT}	25		75	%	
SCK clock pulsewidth	t_{PWSC}	2		150	µs	
SCK clock interval (except WRITE mode)	t_{CYSC}	5		1900	µs	512bps
		5		830	µs	1200bps
		5		415	µs	2400bps
SCK clock interval (WRITE mode)	t_{CYSC}	5		830	µs	
SDI data setup time	t_{SSDI}	1			µs	
SDI data hold time	t_{HSDI}	1			µs	
SDO data setup time	t_{SSDO}	3			µs	
SDO data hold time	t_{HSDO}			0	µs	
ATTN signal setup time	t_{SATT}	0			µs	
ATTN signal hold time	t_{HATT}	1			µs	
CLKO clock rise time	t_{RCLK}			500	ns	No load
CLKO clock fall time	t_{FCLK}			500	ns	No load
CLKO clock delay time	D_{CLKO}			1	µs	
RSTN pulsewidth	t_{PWRS}	1			ms	



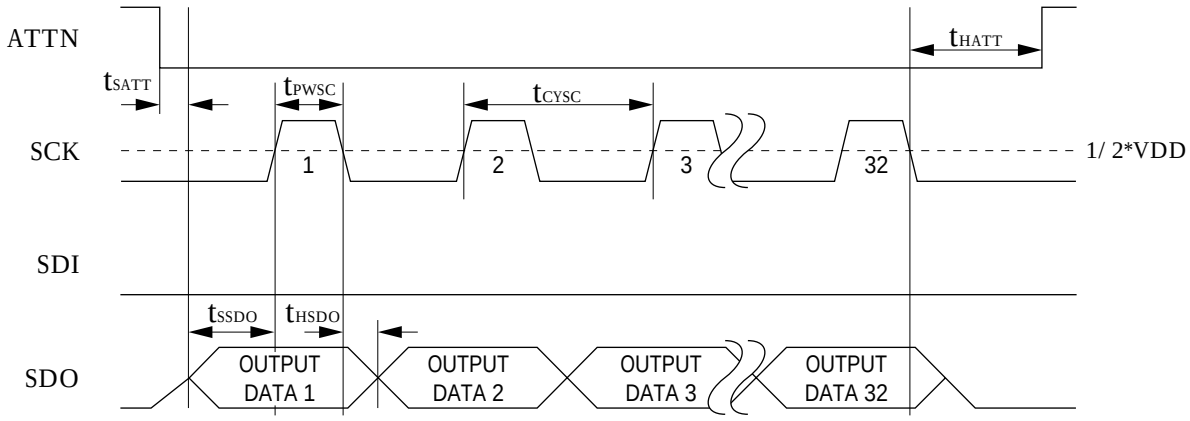
Parameter/address set timing



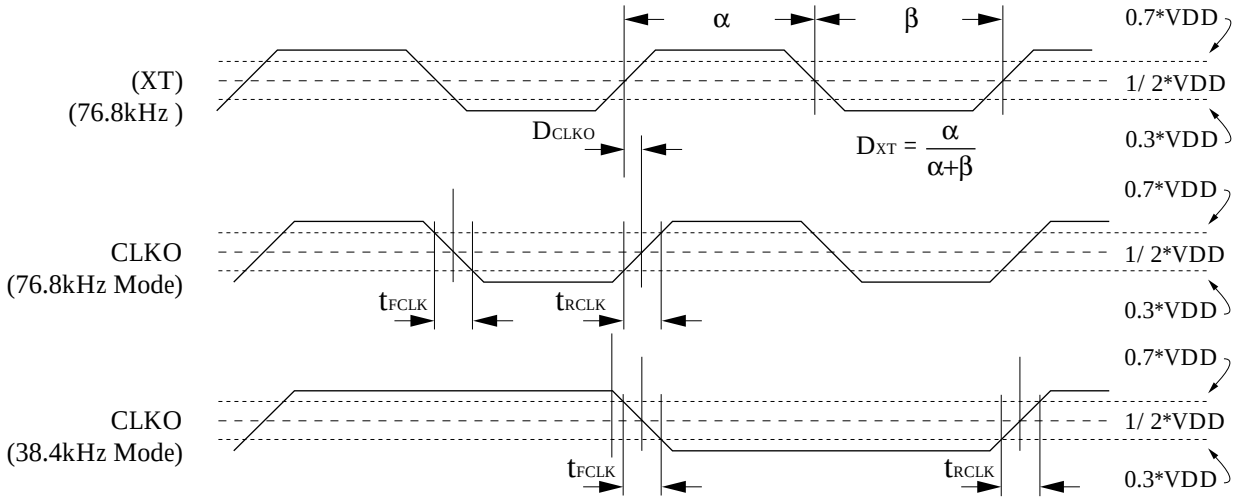
Auxiliary operating mode set timing



Status data read timing



Received data transfer timing



CLKO clock output timing

FUNCTIONAL DESCRIPTION

Unless otherwise specified, values in diagrams without parentheses are for 512 bps, in ( ) are for 1200 bps, and in [ ] are for 2400 bps. “M” represents the value of PL5 (MSB) to PL0 (LSB), and “N” represents the value of RF5 (MSB) to RF0 (LSB).

1. Receive Format

The receive format conforms to CCIR RPC No. 1 (POCSAG).

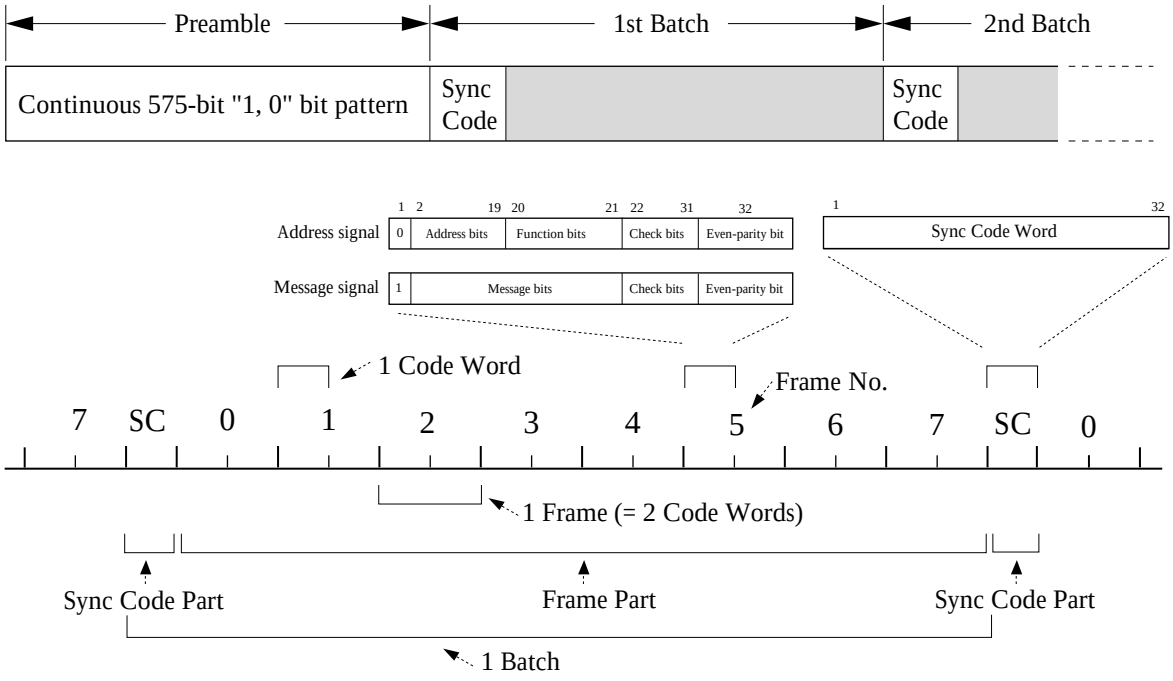


Figure 1. Receive signal format

(1) Sync signal (SC)

The sync signal is a continuous code word in the received signal, used for word synchronization. It comprises 31 bits in an M-series bit pattern plus one even-parity bit, making a 32-bit signal. The sync code word pattern is shown in table 1.

Table 1. Sync code format

Bit number	Bit value	Bit number	Bit value	Bit number	Bit value	Bit number	Bit value
1	0	9	1	17	0	25	1
2	1	10	1	18	0	26	1
3	1	11	0	19	0	27	0
4	1	12	1	20	1	28	1
5	1	13	0	21	0	29	1
6	1	14	0	22	1	30	0
7	0	15	1	23	0	31	0
8	0	16	0	24	1	32	0

(2) Code words (address and message signals)

Each code word comprises 32 bits as shown in table 2.

Table 2. Code word format

<table>
<tr><th rowspan="2">Code word</th><th colspan="5">Bit number</th></tr>
<tr><th>1 (MSB)</th><th>2 to 19</th><th>20 to 21</th><th>22 to 31</th><th>32 (LSB)</th></tr>
<tr><td>Address Signal</td><td>0</td><td>Address bits</td><td>Function bits
<table><tr><th>20</th><th>21</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>A call</td></tr><tr><td>0</td><td>1</td><td>B call</td></tr><tr><td>1</td><td>0</td><td>C call</td></tr><tr><td>1</td><td>1</td><td>D call</td></tr></table></td><td>Check bits</td><td>Even-parity bit</td></tr>
<tr><td>Message Signal</td><td>1</td><td colspan="2">Message bits</td><td>Check bits</td><td>Even-parity bit</td></tr>
</table>

1. The MSB is the address/message code word control bit. It is 0 for an address signal, and 1 for a message signal.
2. Bits 2 to 21 contain the address or message information.
3. Bits 22 to 31 are BCH(31,21) format generated check bits, where BCH(n,k) = BCH(word length, number of information bits).
4. The LSB is an even-parity bit for bits 1 to 31.

(3) Call number to call sign conversion

This conversion expands a 7-digit decimal call number into a 21-bit binary call sign, as shown in figure 2.

After expansion, the high-order 18 bits are assigned to bits 2 to 19 (address signal), and the low-order 3 bits are the user-defined frame identification pattern, which is stored in ID-ROM. The two function bits define which of four call functions is active.

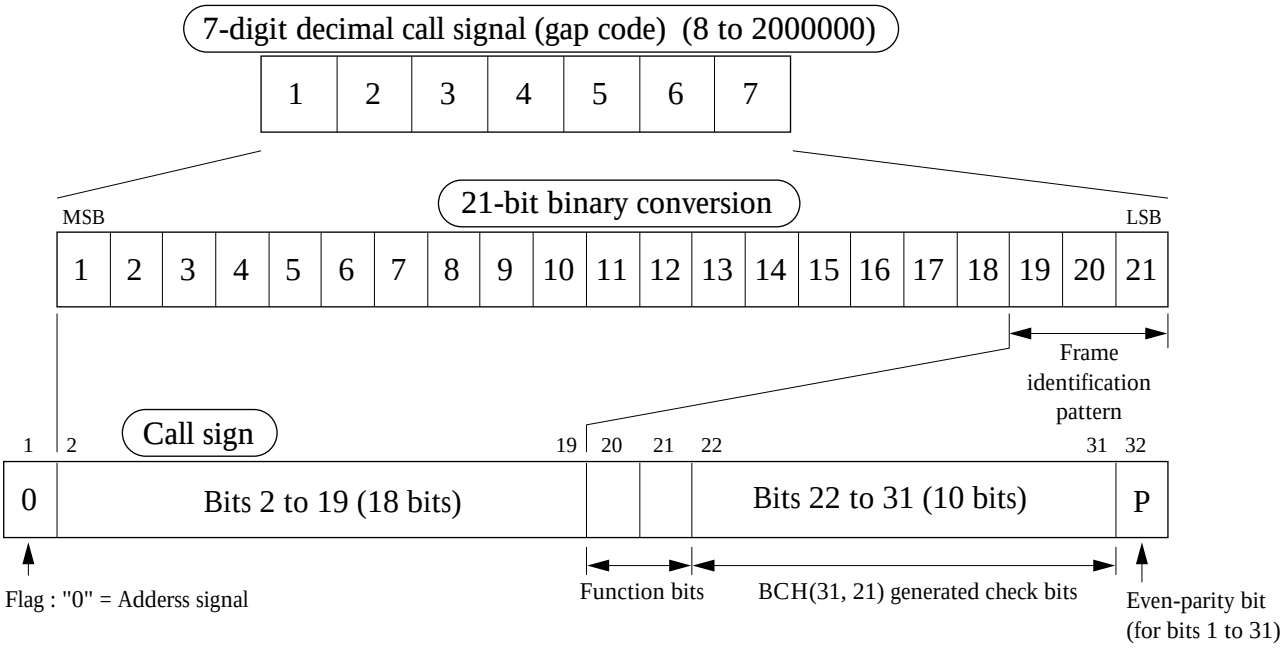


Figure 2. Call number to call sign conversion

(4) Idle signal

In the POCSAG format, for pager systems that send numeric data, the message information content varies and as a result an idle signal or another address signal is inserted after the message to indicate the end of the message.

That is, if no address word or message word exists for a frame within a batch or for a code word within a frame, the idle pattern, shown in table 3, is transmitted in its place. Then during message signal reception, the message ends when the idle signal is detected.

The SM8212B, however, supports 2 methods of determining the end of message. Namely, message ends when either an idle signal or another address is received (POCSAG format), or solely by an interrupt signal from the CPU.

Table 3. Idle code format

Bit number	Bit value	Bit number	Bit value	Bit number	Bit value	Bit number	Bit value
1	0	9	1	17	1	25	1
2	1	10	0	18	1	26	0
3	1	11	0	19	0	27	0
4	1	12	0	20	0	28	1
5	1	13	1	21	0	29	0
6	0	14	0	22	0	30	1
7	1	15	0	23	0	31	1
8	0	16	1	24	1	32	1

(5) Receive signal duty factor

During preamble detection, the preamble pattern (1,0) is recognized at duty factors from 25% (min) to 75% (max) of the (1,0) preamble cycle.

(6) Error Correction and Detection

The SM8212B performs error correction (or detection) on each code word as described in table 4. Note that there are 8 selectable error correction conditions for the preamble pattern.

Table 4. Error correction

Item	Description
Preamble Pattern Detection	Selectable 1 to 8 rate errors in 6 to 544 bits
Synchronization Code word Detection	2 random errors in 32 bits
Self Address Code word Detection	2 random errors in 32 bits
Message Code word	1-bit and 2-bit burst errors in 31 bits

An error is deemed to have occurred when 2 or more signal edges occur within 1-bit unit time, and a rate error is deemed to have occurred when the number of errors exceeds the counter value. Refer to the “Preamble Mode” section for a discussion of the error counter.

2. Battery Saving (BS1, BS2, BS3)

The SM8212B controls the intermittent-duty operation of the RF stage, which reduces battery consumption, and outputs three control signals (BS1, BS2, BS3). The function each signal controls in each mode is described below.

BS1 (RF-control main output signal)

The RF stage is active when BS1 is HIGH. The rising-edge setup time for receive timing is set by flags RF0 to RF5 (61 steps). The maximum setup time is 25.417 ms at 2400 bps, 50.833 ms at 1200 bps and 119.141 ms at 512 bps. Note that 3E and 3F are invalid settings for BS1.

BS2 (RF DC-level adjustment signal)

BS2 is used to control the discharge of the receive signal DC-cut capacitor. The function of BS2 is determined by flag BS2, as described below.

-When flag “BS2 option” is 0, pin BS2 goes HIGH together with BS1 and then goes LOW again after the BS1 setup time in idle mode. In preamble and lock (during address/message reception) mode, it keeps LOW.

-When flag “BS2 option” is 1, pin BS2 goes HIGH during lock mode sync code receive timing and idle mode signal receive timing. In preamble mode, it keeps LOW.

BS3 (PLL setup signal)

BS3 is used to control PLL operation when the PLL is used. The rising-edge setup time for receive timing is set by flags PL0 to PL5 (61 steps). The maximum setup time is 25.833 ms at 2400 bps, 51.667 ms at 1200 bps and 121.094 ms at 512 bps. Note that 3F is an invalid setting for BS3.

Note also that the setup times should be set such that (BS3 rising-edge setup time) > (BS1 rising-edge setup time).

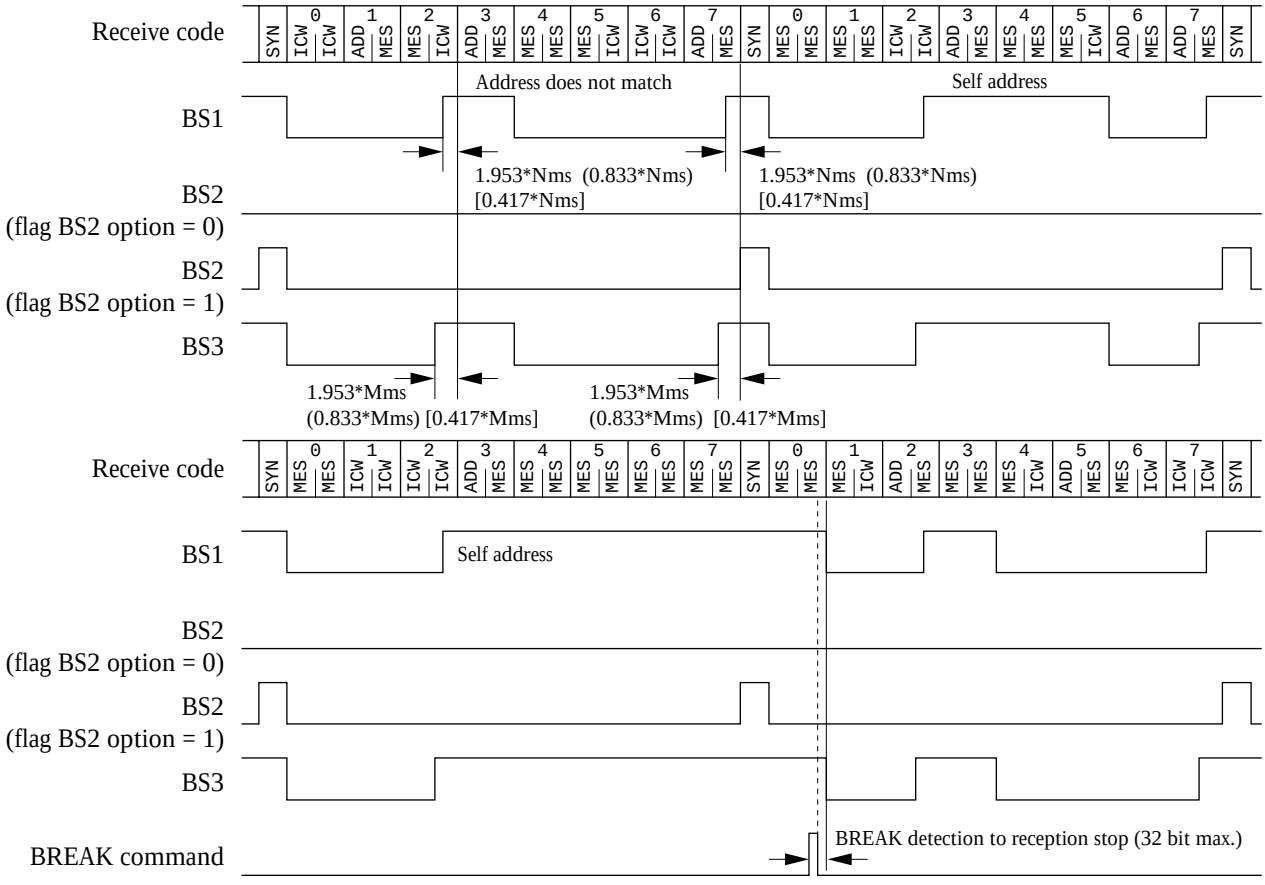


Figure 3. BS1, BS2 and BS3 timing (LOCK mode, frame 3)

3. Operating Modes

The SM8212B has four operating modes: Power-ON (Write), Preamble, Idle and Lock modes.

(1) Power-ON mode

After power is applied, the internal registers should be reset using RSTN.

When ATTN goes HIGH, the decoder sends a write request for a decoder set read command and then waits for the microcontroller (decoder set write command timing starts approximately 50 ms after reset, but for safety, wait minimum 900ms when Power-ON mode). The internal operation in write mode takes place at the same timing as for 1200 bps speed mode.

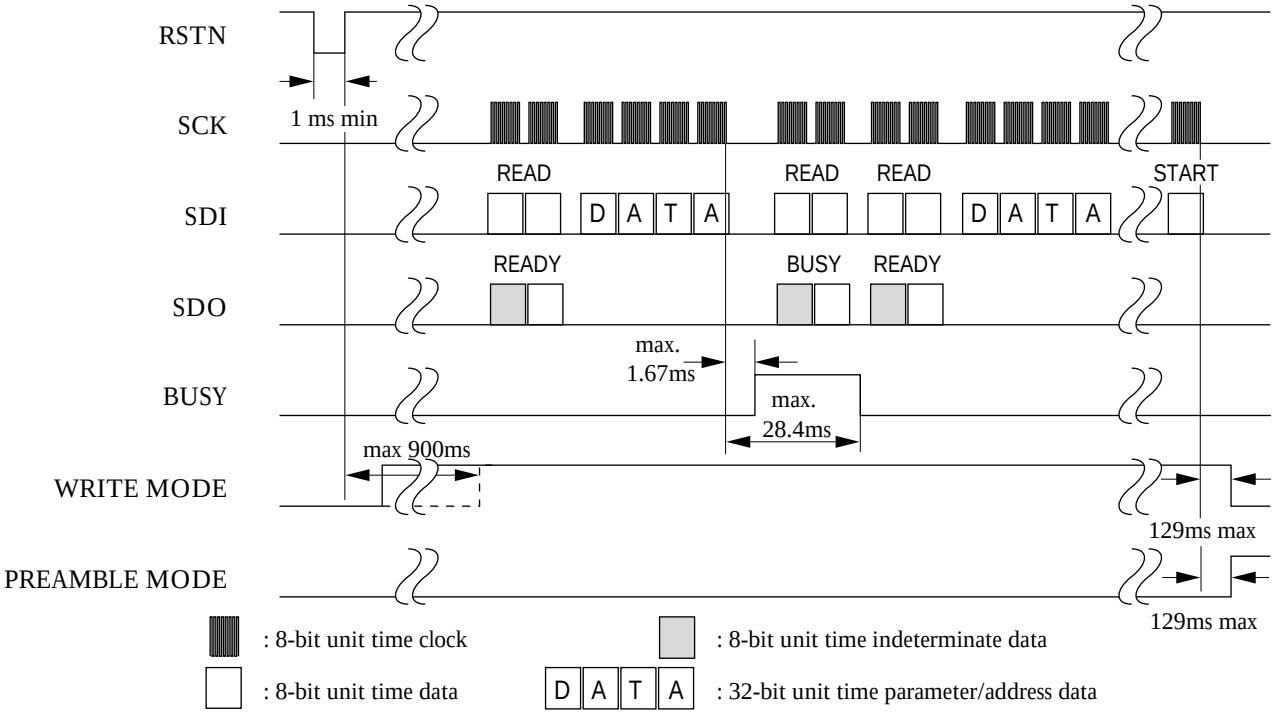
Write data is prepared in 32-bit batches of 1 parameter batch and 8 address data batches for a total of 9 batches.

The parameter and address set commands are processed in sync with the decoder internal clock (1200 Hz). As a consequence, a gap of 28.4 ms minimum should be left between batches to provide time for processing. Alternatively, data can be written by first using the decoder set read command to confirm whether or not processing is still in progress (BUSY) before writing each batch. If the time gap is 28.4 ms or greater, confirmation (READY) is not required.

After parameters and all addresses have been written and after decoder processing, the decoder set start command transfers operation from write mode and starts preamble mode operation.

When setting parameters and addresses in write mode, the SCK clock frequency should not be less than 1200 Hz. If this occurs, the SCK counter is reinitialized. This function, however, does make restoring operation easy even if this or another clock is accidentally input.

In write mode, after power is applied and after reset initialization, all 9 batches (1 parameter and 8 address batches) should be set. If not all batches are set, subsequent operation may become unstable.



Refer to the AC Characteristics section for detailed timing specifications.

Figure 4. Power-ON (WRITE) mode timing

(2) Preamble mode

Preamble mode is a continuous 544-bit long period. If neither a preamble pattern, rate error nor sync code is detected during this period, operation transfers to idle mode.

(a) If a preamble pattern is detected, the preamble mode 544-bit long period is recommenced.

(b) If the sync code is detected, AREA goes HIGH and operation transfers to lock mode. If an error of 2 bits or less occurs, the detected word is recognized as the sync code. During the preamble mode interval, BS1 and BS3 are held HIGH. BS2 keeps LOW.

* A single error occurs when two active edges occur in the received signal on SIGNAL within 1-bit unit time. A rate error occurs when the number of errors in the error counter equals the error threshold set by flags ER0 to ER2. The error counter is reset when a preamble pattern is detected.

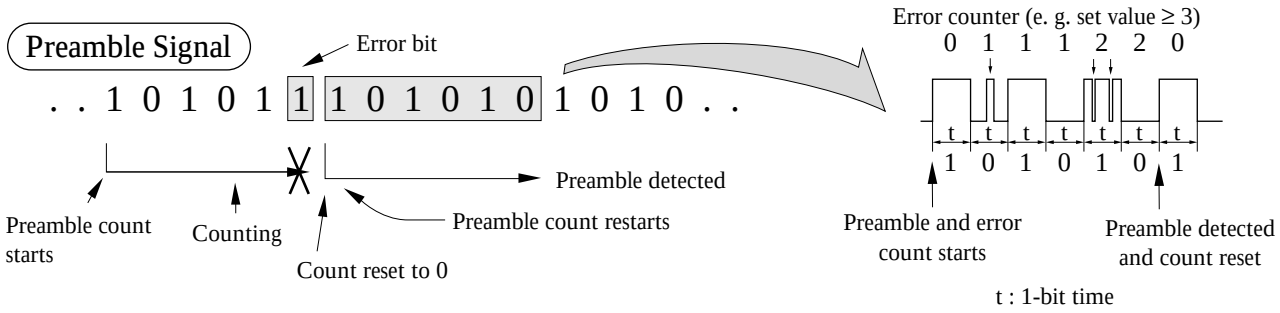


Figure 5. PREAMBLE mode internal operation

(3) Idle mode

In idle mode, a check is made for the presence of a preamble signal when the RF intermittent-duty control signals (BS1, BS2, BS3) for battery saving are active. If a preamble pattern is detected, operation immediately transfers to preamble mode. If a preamble pattern is not detected, intermittent-duty operation continues.

A preamble pattern is detected when either a 101010 or 010101 6-bit pattern is detected. Since there is a reasonable probability that this simple pattern can occur during a valid communicated signal (data, not preamble), this 6-bit pattern makes returning to preamble mode easier. This is useful for cases where weak electric fields, noise or other temporary interference cause device operation to transfer to idle mode.

Further, the idle mode receive timing immediately after transfer from lock mode is the same as the original sync code receive timing. As a result, if a sync code is detected, operation returns to lock mode.

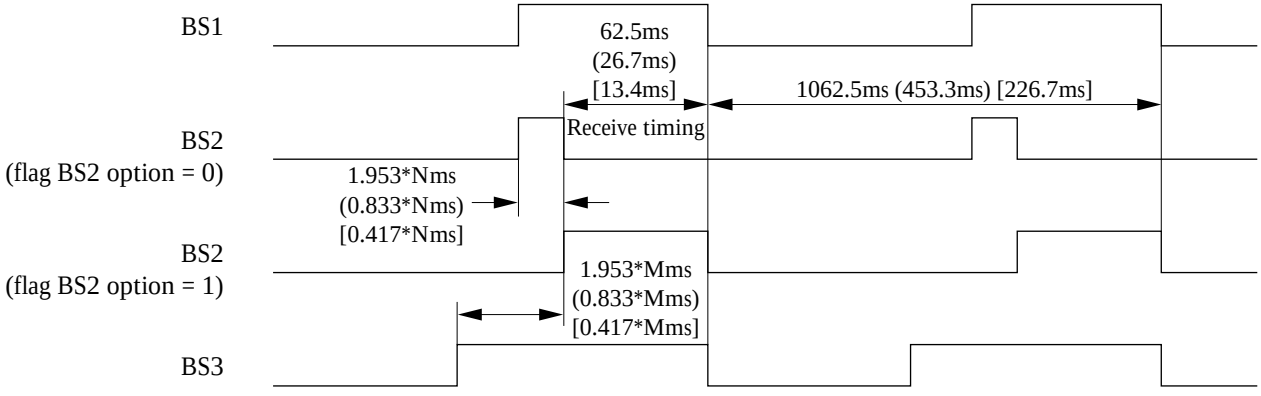


Figure 6. IDLE mode timing

(4) Lock mode

If the sync code is detected during the preamble period, device operation transfers to lock mode and BS1 goes LOW. BS1 then goes HIGH again under frame timing, where the frame number is set by flags FF0 to FF2, and the 32 addresses are compared with ID-ROM (If the frame number is 0, BS1 stays HIGH). If errors of 2 bits or less occur, the address is still recognized. Since there are two code words per frame, this check is done twice.

When one of the 32 addresses does not match, BS1 goes LOW and the device waits for the next frame or sync code receive timing. If the sync code is still not detected after two consecutive attempts, device operation transfers to idle mode, except during message reception where operation stays in lock mode. If the sync code is not detected on the second attempt, but instead a pattern forming a preamble is detected, device operation transfers to preamble mode and not idle mode (preamble mode is more advantageous for sync code detection).

When one of the 32 addresses does match, ATTN goes LOW and the address information (see “Data/Flags” section) is transmitted to the CPU on SDO in sync with the SCK clock.

When the address information is confirmed to be a message, BS1 is held HIGH and the message is received. The received message is stored in a buffer as 32-bit error-corrected information (see “Data/Flags” section), then ATTN goes LOW and the data is transmitted to the CPU on SDO in sync with the SCK clock.

When the address and message is received, ATTN should be held LOW while the data is output on SDO.

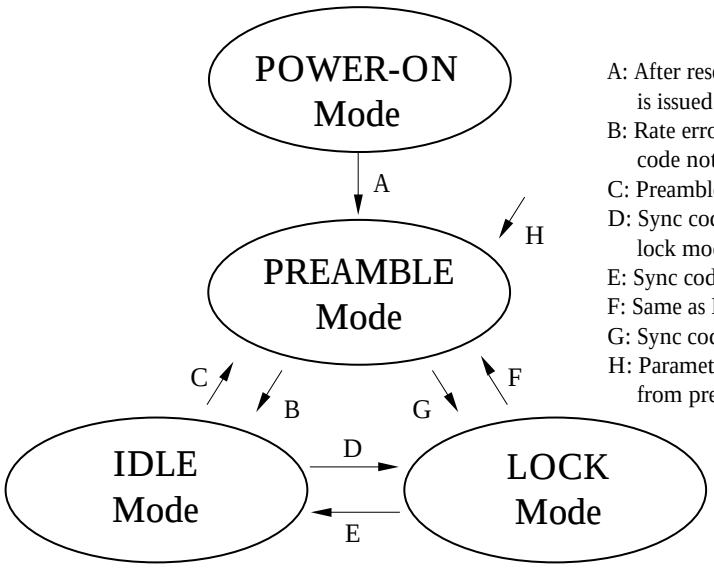
When an incoming message spans two or more batches, additional sync code detection occurs during sync code receive timing.

Message reception can be selected to end when either an address code or idle code is detected, or when interrupted using the decoder set command BREAK input. This selection is made when setting parameters that will not cause the message to terminate. If the BREAK mode is selected, even if an address other than the self address (MSB = 0) is received during message reception, reception continues without interruption and address data is sent to the microcontroller using the same data handling as for a message. In this case, reception can only be interrupted by a BREAK input signal from the microcontroller.

In either of the above cases, message reception ends if an end-of-message signal is sent. (Except MSB=0 but self address, no BREAK input)

When message reception ends, BS1 goes LOW and the device waits for either the address detect timing of the next frame or the sync code receive timing.

When sending data from the decoder to the microcontroller, the SCK clock frequency should not be less than 512, (1200), [2400] Hz. If this occurs, the SCK counter is reinitialized. This function, however, does make restoring operation easy even if this or another clock is accidentally input.



A: After reset, parameters/addresses are set and start command is issued.
B: Rate error or, within a fixed period, preamble pattern/sync code not detected.
C: Preamble pattern detected.
D: Sync code detected 1 cycle immediately after transfer from lock mode.
E: Sync code not detected on 2 consecutive attempts
F: Same as E, but preamble detected on the second attempt.
G: Sync code detected.
H: Parameters/addresses are set and start command is issued from preamble/idle/lock mode.

Figure 7. Operating mode transition diagram

4. Address/Parameter Data Transmission (CPU to SM8212B)

After device reset initialization, the address and parameter data is transmitted from the CPU in 32-bit batches, 1 parameter batch and 8 address batches for a total of 9 batches (288 bits), on SDI in sync with the falling edge of the SCK clock (see “Power-ON Mode” section).

The SM8212B supports 8 independent addresses (identified as A, B, C, D, E, F, G and H). Also, each address can be assigned a frame number to cover all kinds of group calls or subsidiary services.

Any of the 8 addresses can be individually disabled. In this case, the address can be disabled using the “ADDRESS ENABLE” flag when setting the addresses.

The address data for each of the 8 addresses comprises an 18-bit address plus two function bits used to select one of four sub-addresses. Then, one MSB bit (0 for address signals), ten BCH(31,21) format generated check bits and an even-parity bit are added to form 32-bit code words representing the address information which is then stored in RAM. This address information is then compared with the received data to determine correct addressing.

Even if the number of addresses used is less than 8, all addresses should be set immediately after power is applied and immediately after reset. If not all addresses are set, subsequent operation may become unstable.

Each address is 18 bits long and should be input MSB first. Refer to the “AC Characteristics” section for SCK and data specifications, and the “Data/Flags” section for data and flag functions.

When setting parameters and addresses in write mode, the SCK clock frequency should not be less than 1200 Hz. If this occurs, the SCK counter is reinitialized. This function, however, does make restoring operation easy even if this or another clock is accidentally input.

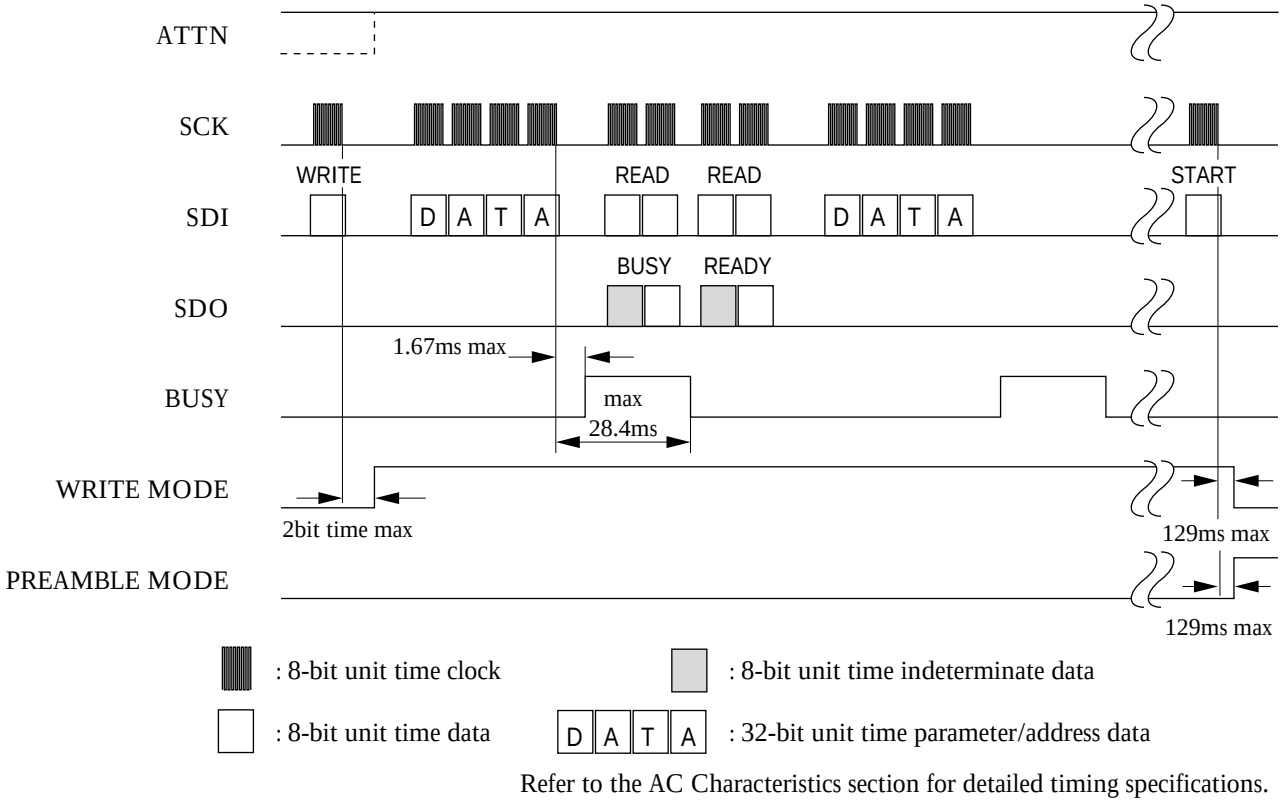


Figure 8. Address/parameter transmit timing

5. Received Data Transmission (SM8212B to CPU)

In lock mode, if the receive data for the frame is recognized as one of the 32 addresses with 2 bit errors or less, then the data is temporarily stored in the transmit buffer and then error correction and other processing takes place.

After processing, ATTN goes LOW to inform the CPU that transmit ready data is available.

The SM8212B switches the data internally and then outputs 32-bit data, shown in table 6, on SDO in sync with the falling edge of the SCK clock. The CPU can then read the data on either the SCK rising edge or the falling edge.

The message bits (1 to 20), which are the 13th to 32nd bits of the detected address data, comprises 18 address information bits and 2 function bits.

When the 32-bit transmission ends, ATTN goes HIGH to indicate that all necessary information has been transmitted.

When an address is detected, the next 32-bit data code word is received. The BCH(31,21) format error check bits are checked and if a 1-bit or two consecutive bit errors occur, they are corrected. Two random bit errors, or three or more bit errors are not corrected.

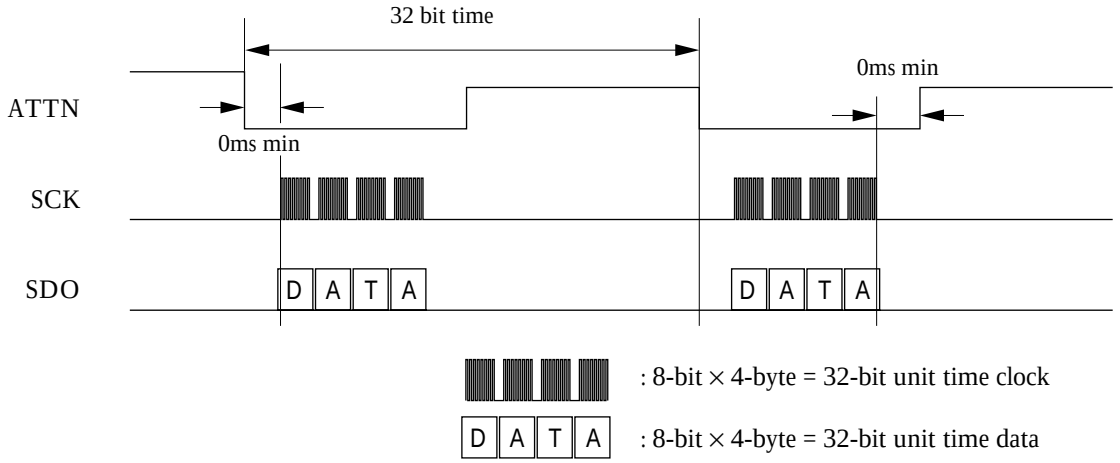
If the corrected data MSB is 1, the data is recognized as a message, data reception continues and the corrected message data and error check flags are sent to the CPU as 32-bit data, shown in table 7, with the same data handling as an address. In this case also, ATTN goes LOW after processing to inform the CPU that transmit ready data is available. The time from when ATTN goes LOW until the CPU sends the SCK should be the same as shown in figure 9. Also, when the message continues, the normal SCK clock speed becomes faster than the receive signal bit rate and as a result there is a limit to the transmitted information capacity. As ATTN is used as the transmit ready data available signal output, it can be used as the CPU interrupt signal to receive data with the timing shown in figure 9.

Conversely, when the decoder takes ATTN LOW to indicate transmit ready data is available, the microcontroller operates under normal starting conditions (high-speed clock operation), and 32-bit clock is input on SCK. After data is read in and until ATTN goes LOW for the next transmit ready data signal, the series processing should be such that it takes less than {32x(bit rate)} time.

When the MSB is 0 and data is recognized as an idle signal or idle code, data reception and data transfer to the CPU stops after the end-of-message is output for addresses not matching the self address.

However, when CPU BREAK input interrupt end-of-message method is selected (see “Flag Setting” section), data is treated as a message and reception continues even if the MSB is 0.

When sending data from the decoder to the microcontroller, the SCK clock frequency should not be less than 512, (1200), [2400] Hz. If this occurs, the SCK counter is reinitialized. This function, however, does make restoring operation easy even if this or another clock is accidentally input.



Refer to the AC Characteristics section for detailed timing specifications.

Figure 9. Received data transmit timing

6. Decoder Set Command Transfer (CPU to SM8212B)

In the SM8212B, the Break, Back-up, Write, BS-test, Start and End auxiliary modes are controlled control signals from the CPU. These modes are set by data written on SDI in sync with the SCK clock (see “Data/Flags” section).

When sending data from the decoder to the microcontroller, the SCK clock frequency should not be less than 1200 Hz. If this occurs, the SCK counter is reinitialized. This function, however, does make restoring operation easy even if this or another clock is accidentally input.

Note that read mode function is described in the “Decoder Internal Status Transfer” section.

(1) Break

This is the interrupt command to stop reception and data transfer. When the Break command is detected, the received code word ends and reception stops, then the device waits for self frame address detection or sync code detection timing. Reception may continue for up to 32-bit unit time after the Break command is received (or 34-bit time after the Break command is sent).

Even though message reception may continue for a short time when the Break command is sent, sync code detection does not take place and accordingly the received data may be deemed to have many errors.

Also, when CPU BREAK input interrupt end-of-message method only is selected, message reception continues even if an address code or an idle code is present, as long as the Break command is not issued.

The time required from when the Break command is issued until received data is output can be approximately 2 to 3 code words at internal sync speed. During this interval, 32 clock cycles are sent to the decoder while ATTN is LOW, and processing should be performed just as for normal operation. If no processing is performed, subsequent operation may become unstable.

(2) Back-up (Power save control)

This is the decoder OFF mode command. This command stops all internal operation except the oscillator, and thus is used to control current consumption. CLKO output is stopped. Note that in back-up mode, the input/output pins do not become high impedance.

Back-up mode is released and operation restarts when the decoder set start command is issued. All parameter and address information is retained during back-up, so operation starts directly from preamble mode.

Note that only the decoder set start command is accepted during back-up mode.

Note that issuing the BACK-UP command is prohibited in the WRITE mode.

(3) Write

This is the parameter and address write command. This operation mode can also be used to modify parameters and addresses. Write mode can be activated from BS-test mode, and also approximately 50 ms after reset, but for safety, wait minimum 900ms when Power-ON reset.

Parameters and addresses can be changed by first issuing a decoder set command to enter write mode and then writing new parameters and addresses.

Note that in write mode, all internal operation takes place with the same timing as for 1200 bps speed mode. BS1, BS2 andBS3 are keep LOW.

Each of the addresses can be turned ON/OFF, according to flag settings in the data written. Using this feature for a specific address in a pager allows the service provider, by prior agreement, to prohibit improper use of the pager delivery service (excluding delivery testing, stopping subsidiary services and similar functions).

In the SM8212B, data writes from the microcontroller have priority, even if a received information transmit ready signal (ATTN = LOW) is present (forced write).

When reception from the decoder RF stage has priority, operation switches to write mode after the end-of-message is confirmed by monitoring the internal operation using the read command. Then the parameter set commands and address set commands are written.

After writing, write mode is released using the decoder set start command, and operation starts from preamble mode.

(4) BS-test

This mode is used to test the RF stage operation, and is only available from write mode. BS1 and BS3 held HIGH for RF stage testing.

After testing, BS-test mode is released using the decoder set start command, and operation starts from preamble mode.

Note that issuing the BACK-UP command is prohibited in the BS-test mode.

(5) Start

This command is used to return to normal operation from back-up, write and BS-test modes. Operation always restarts from preamble mode.

Note the following points when setting commands:

Immediately after ATTN goes LOW

Commands send 8 SCK clock cycles to the decoder and the received data is sent using 32 clock cycles immediately after ATTN goes LOW. However, apart from the 8 clock cycles needed for the command, 32 clock cycles are needed to release ATTN.

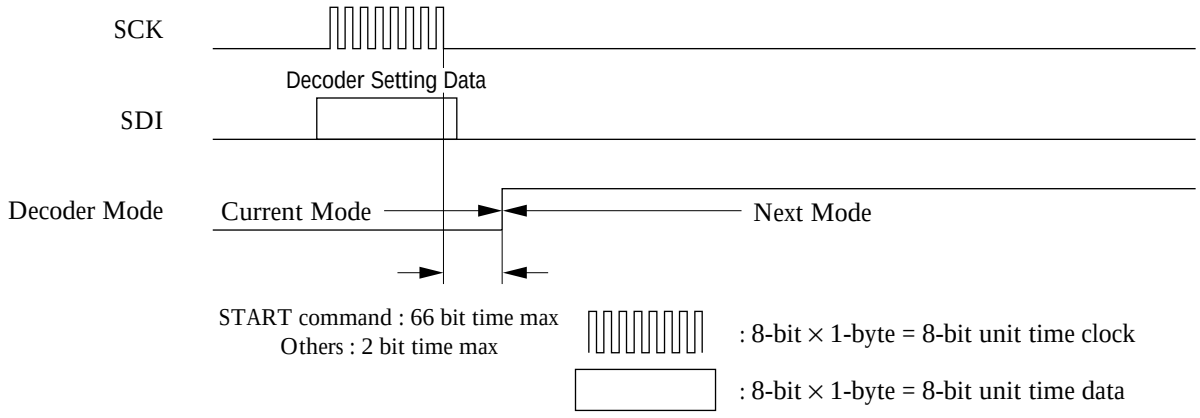
After being transferred the command, even if ATTN keeps LOW, transmitted reception data is unstable.

When ATTN is HIGH

These commands should use when ATTN HIGH timing only.

After command is transferred and until ATTN goes LOW for the next transmit ready data signal, the series processing should be such that it takes less than {32x(bit rate)} time.

When ATTN goes HIGH (excluding write mode), SCK is examined to determine if the signal is a break, back-up, write or read command. During message reception, ATTN is temporarily held HIGH if a command is issued to set ATTN LOW. This delay ensures that the data from the decoder is not misinterpreted. And in this case, even if ATTN keeps LOW, transmitted receiving data is unstable.



Refer to the AC Characteristics section for detailed timing specifications.

Figure 10. Auxiliary operating mode timing

7. Decoder Internal Status Transfer (SM8212B to CPU)

In the SM8212B, the internal decoder status and parameter/address end-of-processing confirmation, is transmitted to the CPU. The microcontroller uses this status information only when needed.

This is a 2-byte (16 bits) command where the first byte is a decoder set read command and the second byte is the decoder internal status that is sent to the microcontroller in sync with the SCK clock.

The microcontroller can use this function when not receiving data from the decoder (when ATTN is HIGH timing only).

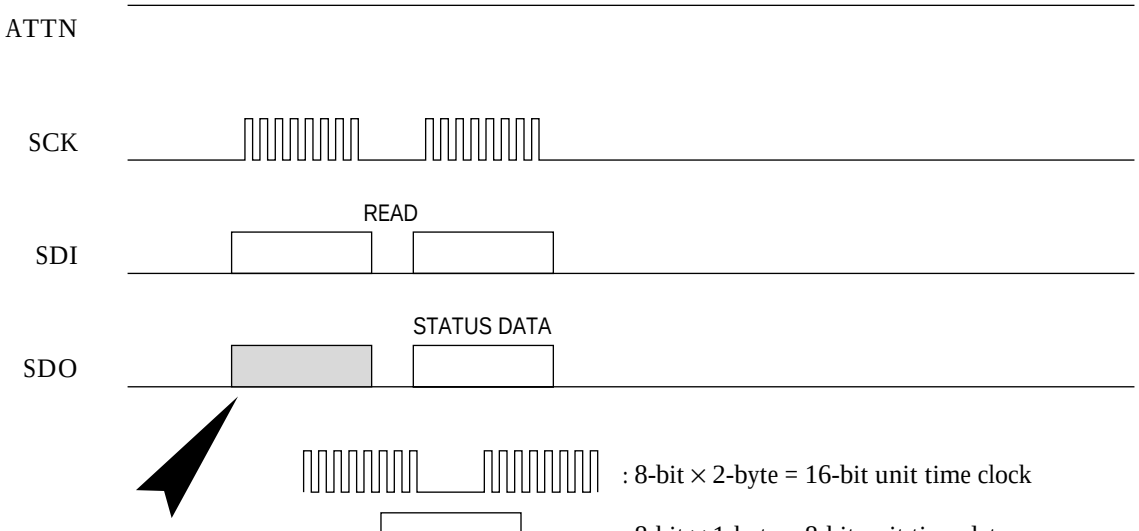
Note the following points when setting the read command:

When ATTN is HIGH

Read command should use when ATTN HIGH timing only.

After data is transferred and until ATTN goes LOW for the next transmit ready data signal, the series processing should be such that it takes less than {32x(bit rate)} time.

When ATTN goes HIGH (excluding write mode), SCK is examined to determine if the signal is a break, back-up, write or read command. During message reception, ATTN is temporarily held HIGH if a command is issued to set ATTN LOW. This delay ensures that the data from the decoder is not mis-interpreted. And in this case, even if ATTN keeps LOW, transmitted receiving data is unstable.



Refer to the AC Characteristics section for detailed timing specifications.

Figure 11. Internal status transfer timing

8. Miscellaneous Interface Pins

(1) SIGNAL

NRZ-format signal input pin, with built-in noise canceller filter.

Current pager systems operate at 3 baud rates (512, 1200 and 2400 bps). In conventional systems, the RF stage LPF time constants are changed in response to the baud rate in order to get the best possible reception. However, this requires changing the external components which results in increased product operating costs.

The SM8212B, however, performs digital processing on the input signal which allows the 3 baud rates to be covered without the need to substitute RF stage LPF components. The side effect of this digital filter processing is a small probability of rate errors occurring.

Digital processing can be turned ON/OFF using flags. When turned ON, there are 4 filter constant settings that can be selected to obtain the best possible reception conditions in a flexible manner (see “Parameter Flags” section).

(2) XT, XTN

Crystal oscillator element connection pins.

The SM8212B operates at 76.8 kHz system clock speed, and this clock can be provided simply by connecting a crystal element between XT and XTN. The oscillator amplifier, feedback resistance and oscillator capacitance are all built-in.

In this case, XTN should not be used as a clock to drive an external device. Also, a 1000 pF to 0.1 µF capacitor should be connected between XVSS and VDD.

(3) CLKO

Clock output pin. The clock output can be used as a CPU sleep clock or melody IC (SM1124 series) clock.

The output clock frequency, 76.8 or 38.4 kHz, is selected using the decoder parameter set command.

(4) RSTN

Decoder IC internal initialization reset pin. It also functions as an oscillator start-up booster (current source) immediately after power is applied to speed up oscillator stabilization.

(5) AREA

This pin goes HIGH for ≥ 1 second when a sync code is detected with 2 or less random bit errors in preamble, lock or idle mode sync code detection timing.

During intermittent-duty CPU operation, monitoring this pin is useful for out-of-range signal strength.

However, even if a sync code is detected, this pin is not held HIGH for ≥ 1 second if 2 consecutive sync codes could not be detected, or under the following situations in 1200 and 2400 bps modes.

- When the second of 2 consecutive sync codes could not be detected but a 6-bit preamble is detected and preamble continues.
- When operation transfers from lock mode to idle mode and then to preamble mode. Note that if operation stays in idle mode after transfer from lock mode, this pin goes HIGH for ≥ 1 second.

Data/Flags

1. Parameter set flags (1)

Table 5. Parameter set flags

	Parameter setting flag
1	0
2	1
3	0
4	0
5	0
6	0
7	0
8	BS2 OPTION (BS2 option)
9	END OF MESSAGE DETECTION
10	SELECT CLKO FREQUENCY
11	KILL CLKO
12	BIT RATE SET 1 (BRS1)
13	BIT RATE SET 0 (BRS0)
14	SIGNAL POLARITY
15	PL5
16	PL4
17	PL3
18	PL2
19	PL1
20	PL0
21	RF5
22	RF4
23	RF3
24	RF2
25	RF1
26	RF0
27	FILTER ENABLE/ DISABLE
28	FILTER 1
29	FILTER 0
30	ERROR 2 (ER 2)
31	ERROR 1 (ER 1)
32	ERROR 0 (ER 0)

Bits 1 to 7

These bits form the parameter set command.

Bit 8

This bit selects the output format of the RF DC-level adjustment signal output on BS2.

When the “BS2 option” flag is 0, pre-receive adjustment mode is selected, and BS2 goes HIGH for a period of 1.953xN ms (0.833xN ms) [0.417xN ms] immediately before receive timing during intermittent-duty operation in idle mode. BS2 is held LOW in preamble and lock mode. Note that values without parentheses are for 512 bps, in ( ) are for 1200 bps, and in [ ] are for 2400 bps. “N” represents the value set by RF5 (MSB) to RF0 (LSB).

When the “BS2 option” flag is 1, mid-receive adjustment mode is selected, with different timing depending on the mode.

In idle mode, BS2 is held HIGH only during intermittent-duty operation receive timing which is a period of 62.5 ms (26.7 ms) [13.4 ms].

In preamble mode, BS2 is held LOW.

In lock mode, BS2 is held HIGH during sync code receive timing. The sync code is a POCSAG-format conforming signal comprising 32 bits of 16 “0” and 16 “1” bits to maintain energy balance so that, even for long message reception and fast-changing reception conditions, it can still be detected.

Bit 9

End-of-message method select flag.

When 0, end of message occurs when either an idle code word or another address is received during message reception, or when a break command is issued from the CPU.

When 1, end of message occurs only when a break command is issued from the CPU. So even if another address is received, the data is sent continuously to the CPU with message data handling. Therefore, the signal is considered to be valid even if the service provider sends a message and not enough information is received due to signal noise.

Bit 10

CLKO output clock frequency select flag.

When 0, 76.8 kHz is selected.

When 1, 38.4 kHz is selected.

Bit 11

CLKO clock output enable flag.

When 0, output is enabled.

When 1, output is disabled.

If CLKO clock output is not used, it can be useful in preventing unwanted noise generation.

2. Parameter set flags (2)

Table 5. Parameter set flags

	Parameter setting flag
1	0
2	1
3	0
4	0
5	0
6	0
7	0
8	BS2 OPTION (BS2 option)
9	END OF MESSAGE DETECTION
10	SELECT CLKO FREQUENCY
11	KILL CLKO
12	BIT RATE SET 1 (BRS1)
13	BIT RATE SET 0 (BRS0)
14	SIGNAL POLARITY
15	PL5
16	PL4
17	PL3
18	PL2
19	PL1
20	PL0
21	RF5
22	RF4
23	RF3
24	RF2
25	RF1
26	RF0
27	FILTER ENABLE/ DISABLE
28	FILTER 1
29	FILTER 0
30	ERROR 2 (ER 2)
31	ERROR 1 (ER 1)
32	ERROR 0 (ER 0)

Bits 12 to 13

Receive bit rate set flags.

BRS1	BRS0	Reception bit rate
0	0	512 bps
0	1	1200 bps
1	0	2400 bps
1	1	Can't accept

Bit 14

NRZ input signal polarity select flag.

When 0, normal logic is selected.

When 1, inverse logic is selected.

Bits 15 to 20

BS3 (PLL setup signal) setup time set flags.

"M" represents the value of PL5 (MSB) to PL0 (LSB) and is used to control the receive timing setup time before BS3 rising edge. The setup time is 1.953xM ms (0.833xM ms) [0.417xM ms]. The valid values are from 2 to 62 (61 steps). Note that 3F HEX is an invalid setting.

Bits 21 to 26

BS1 (RF control main output signal) setup time set flags.

"N" represents the value of RF5 (MSB) to RF0 (LSB) and is used to control the receive timing setup time before BS3 rising edge. The setup time is 1.953xN ms (0.833xN ms) [0.417xN ms]. The valid values are from 2 to 62 (61 steps). Note that 3E and 3F HEX are invalid settings.

Note also that the setup times should be set such that (BS3 rising-edge setup time) > (BS1 rising-edge setup time).

Bit 27

NRZ signal input noise canceller filter ON/OFF flag.

When 0, filter is OFF.

When 1, filter is ON.

Bits 28 to 29

These bits set the noise canceller filter on-state (strength) when the filter is turned ON using bit 27.

FILTER 1	FILTER 0	Filter strength
0	0	Filter strength 1
0	1	Filter strength 2
1	0	Filter strength 3
1	1	Filter strength 4

Filter ON-state strength:
1 < 2 < 3 < 4

Bits 30 to 32

Preamble mode rate error detection condition set flags.

In preamble mode, under worst-case reception conditions, a single standard is used when distinguishing between noise and preamble to detect rate errors. These flags determine the rate error detection standard. The error counter value (number of permissible rate errors) can be selected from the range 1 to 8.

ER 2	ER 1	ER 0	Threshold	ER 2	ER 1	ER 0	Threshold
0	0	0	Count = 1	1	0	0	Count = 5
0	0	1	Count = 2	1	0	1	Count = 6
0	1	0	Count = 3	1	1	0	Count = 7
0	1	1	Count = 4	1	1	1	Count = 8

3. Address set flags

In the SM8212B, each of the 8 independent addresses can be assigned a frame.

Address settings are made in 8 batches in write mode immediately after power is applied and immediately after reset (9 batches total, including the parameter batch). All batches should be set. If not all batches are set, subsequent operation may become unstable.

Also, an address setting can be modified during normal operation, 1 address at a time, with no adverse effects.

Note : Please refrain from turning "ON" the same number of address for two or more at the same time when setting addresses.

Table 6. Address set flags

	Address setting flag
1	0
2	1
3	1
4	0
5	0
6	0
7	0
8	ADDRESS ENABLE
9	ADDRESS 2 (ADDR 2)
10	ADDRESS 1 (ADDR 1)
11	ADDRESS 0 (ADDR 0)
12	FRAME 2 (FR 2)
13	FRAME 1 (FR 1)
14	FRAME 0 (FR 0)
15	A1
16	A2
17	A3
18	A4
19	A5
20	A6
21	A7
22	A8
23	A9
24	A9
25	A11
26	A12
27	A13
28	A14
29	A15
30	A16
31	A17
32	A18

Bits 1 to 7

These bits form the address set command.

Bit 8

These bits are the address (bits 9 to 32) enable flags.

When 1, the address set by bits 9 to 32 are valid.

When 0, the address set by bits 9 to 32 are invalid.

Bits 9 to 11

These bits are the address (bits 15 to 32) call sign set flags.

Using 8-address control, the call signs are A, B, C, D, E, F, G and H.

When an address code word is received, it is compared with the self addresses.

ADDR 2	ADDR 1	ADDR 0	Name	ADDR 2	ADDR 1	ADDR 0	Name
0	0	0	A	1	0	0	E
0	0	1	B	1	0	1	F
0	1	0	C	1	1	0	G
0	1	1	D	1	1	1	H

Bits 12 to 14

These bits are the address (bits 15 to 32) frame assign flags.

Any frame can be assigned individually to any of the 8 controllable addresses. Up to 8 frames can be assigned.

FR 2	FR 1	FR 0	Frame	FR 2	FR 1	FR 0	Frame
0	0	0	Frame 0	1	0	0	Frame 4
0	0	1	Frame 1	1	0	1	Frame 5
0	1	0	Frame 2	1	1	0	Frame 6
0	1	1	Frame 3	1	1	1	Frame 7

Bits 15 to 32

Address bits.

The 18-bit address should be written with MSB first.

4. Receive Data (1)

Table 7. Receive data format

	Reception data
1	1
2	MESSAGE/ ADDRESS
3	SELF ADDRESS
4	ADDRESS 2 (ADDR 2)
5	ADDRESS 1 (ADDR 1)
6	ADDRESS 0 (ADDR 0)
7	FUNCTION 1 (FUNC 1)
8	FUNCTION 0 (FUNC 0)
9	SYN - VAL
10	ERROR 1 (ERR 1)
11	ERROR 0 (ERR 0)
12	PARITY ERROR
13	MESSAGE 1/ADDRESS 1
14	MESSAGE 2/ADDRESS 2
15	MESSAGE 3/ADDRESS 3
16	MESSAGE 4/ADDRESS 4
17	MESSAGE 5/ADDRESS 5
18	MESSAGE 6/ADDRESS 6
19	MESSAGE 7/ADDRESS 7
20	MESSAGE 8/ADDRESS 8
21	MESSAGE 9/ADDRESS 9
22	MESSAGE 10/ADDRESS 10
23	MESSAGE 11/ADDRESS 11
24	MESSAGE 12/ADDRESS 12
25	MESSAGE 13/ADDRESS 13
26	MESSAGE 14/ADDRESS 14
27	MESSAGE 15/ADDRESS 15
28	MESSAGE 16/ADDRESS 16
29	MESSAGE 17/ADDRESS 17
30	MESSAGE 18/ADDRESS 18
31	MESSAGE 19/FUNCTION 1
32	MESSAGE 20/FUNCTION 0

Bit 1

The receive data leading bit is always 1.

Bit 2

Message/address indicator flag.

When 0, the data is an address.

When 1, the data is a message.

Bit 3

Self address indicator flag.

When 1, the data is treated as a self address (device address).

When 0, the data is a message.

When this bit is set to 1, the self address corresponds to one of the addresses indicated by bits 4 to 6.

Bits 4 to 6

Address call sign flags.

When bit 3 of data is 1, indicating a self address, these bits indicate the call sign.

When the data is a message, all 3 bits are set to 0.

ADDR 2	ADDR 1	ADDR 0	Name	ADDR 2	ADDR 1	ADDR 0	Name
0	0	0	A	1	0	0	E
0	0	1	B	1	0	1	F
0	1	0	C	1	1	0	G
0	1	1	D	1	1	1	H

Bits 7 to 8

Function bit flags.

When bit 3 of data is 1, indicating a self address, these bits set the call function for the address indicated by bits 4 to 6.

When the data is a message, both bits are set to 0.

FUNC 1	FUNC 0	Function
0	0	A Call
0	1	B Call
1	0	C Call
1	1	D Call

5. Receive data (2)

Table 7. Receive data format

	Reception data
1	1
2	MESSAGE/ ADDRESS
3	SELF ADDRESS
4	ADDRESS 2 (ADDR 2)
5	ADDRESS 1 (ADDR 1)
6	ADDRESS 0 (ADDR 0)
7	FUNCTION 1 (FUNC 1)
8	FUNCTION 0 (FUNC 0)
9	SYN - VAL
10	ERROR 1 (ERR 1)
11	ERROR 0 (ERR 0)
12	PARITY ERROR
13	MESSAGE 1/ADDRESS 1
14	MESSAGE 2/ADDRESS 2
15	MESSAGE 3/ADDRESS 3
16	MESSAGE 4/ADDRESS 4
17	MESSAGE 5/ADDRESS 5
18	MESSAGE 6/ADDRESS 6
19	MESSAGE 7/ADDRESS 7
20	MESSAGE 8/ADDRESS 8
21	MESSAGE 9/ADDRESS 9
22	MESSAGE 10/ADDRESS 10
23	MESSAGE 11/ADDRESS 11
24	MESSAGE 12/ADDRESS 12
25	MESSAGE 13/ADDRESS 13
26	MESSAGE 14/ADDRESS 14
27	MESSAGE 15/ADDRESS 15
28	MESSAGE 16/ADDRESS 16
29	MESSAGE 17/ADDRESS 17
30	MESSAGE 18/ADDRESS 18
31	MESSAGE 19/FUNCTION 1
32	MESSAGE 20/FUNCTION 0

Bit 9

Sync code preceding data reception receive status flag.

When 1, indicates that there are 2 or less random bit errors.

This flag is useful in determining data reliability.

Bits 10 to 11

Received message (or address) error correction indicator flags.

Note that 2-bit random errors and 3-bit (or more) errors are not corrected.

When data is an address, [ERR 1, 0] = (1, 1) is 2-bit random errors.

ERR 1	ERR 0	Condition
0	0	No errors
0	1	1-bit error
1	0	2-bit continuous (burst) error
1	1	2-bit random or 3-bit (or more) error

Bit 12

Parity error indicator flag.

When 1, indicates a parity error.

When 0, indicates no parity error.

Bits 13 to 32

Message (or address) bits.

These bits represent the message (or address) content, output with MSB first.

End-of-message data

These bits represent data at the end of a message (including when using the break command).

The end-of-message data is as follows:

Bits 1 to 3

All 3 bits are set to 1.

Bits 4 to 8

All 5 bits are set to 0.

Bit 9

Sync code preceding data reception receive status flag.

When 1, indicates that there are 2 or less random bit errors.

This flag is useful in determining data reliability.

Bits 10 to 12

These bits are unknown data to be ignored.

Bits 13 to 32

All bits are set to 0.

6. Receive data (3)

The following table show the address, message and end-of-message data formats, respectively.

Table 7-1 Address data format

	Reception data
1	1
2	0
3	1
4	ADDRESS 2 (ADDR 2)
5	ADDRESS 1 (ADDR 1)
6	ADDRESS 0 (ADDR 0)
7	FUNCTION 1 (FUNC 1)
8	FUNCTION 0 (FUNC 0)
9	SYN - VAL
10	ERROR 1 (ERR1)
11	ERROR 0 (ERR))
12	PARITY ERROR
13	ADDRESS 1
14	ADDRESS 2
15	ADDRESS 3
16	ADDRESS 4
17	ADDRESS 5
18	ADDRESS 6
19	ADDRESS 7
20	ADDRESS 8
21	ADDRESS 9
22	ADDRESS 10
23	ADDRESS 11
24	ADDRESS 12
25	ADDRESS 13
26	ADDRESS 14
27	ADDRESS 15
28	ADDRESS 16
29	ADDRESS 17
30	ADDRESS 18
31	FUNCTION 1
32	FUNCTION 0

Table 7-2 Message data format

	Reception data
1	1
2	1
3	0
4	0
5	0
6	0
7	0
8	0
9	SYN - VAL
10	ERROR 1 (ERR 1)
11	ERROR 0 (ERR 0)
12	PARITY ERROR
13	MESSAGE 1
14	MESSAGE 2
15	MESSAGE 3
16	MESSAGE 4
17	MESSAGE 5
18	MESSAGE 6
19	MESSAGE 7
20	MESSAGE 8
21	MESSAGE 9
22	MESSAGE 10
23	MESSAGE 11
24	MESSAGE 12
25	MESSAGE 13
26	MESSAGE 14
27	MESSAGE 15
28	MESSAGE 16
29	MESSAGE 17
30	MESSAGE 18
31	MESSAGE 19
32	MESSAGE 20

Table 7-3 End-of-message data format

	Reception data
1	1
2	1
3	1
4	0
5	0
6	0
7	0
8	0
9	SYN - VAL
10	UNKNOWN
11	UNKNOWN
12	UNKNOWN
13	0
14	0
15	0
16	0
17	0
18	0
19	0
20	0
21	0
22	0
23	0
24	0
25	0
26	0
27	0
28	0
29	0
30	0
31	0
32	0

6. Decoder set flags

These flags set the auxiliary operating modes. See "Decoder Set Command Transfer" for a description of each auxiliary operating mode.

Note that the start command is accepted when in back-up, write, or BS-test mode. The start command is not accepted in modes other than these three.

Also note that the write command is invalid in write mode.

Table 8. Decoder set flags

	Decoder setting flag
1	1
2	0
3	BREAK
4	BACK - UP
5	WRITE
6	BS - TEST
7	START
8	0

Bits 1 to 2 and bit 8

These bits form the decoder set command.

Only one of bits 3 to 7 can be logic 1 at any given time to select the corresponding auxiliary operating mode.

If more than one bit is 1 at any time, operation may become unstable.

Bit 3

Break mode (command) flag.

When 1, break mode operation is invoked.

Bit 4

Back-up mode (command) flag.

When 1, back-up mode operation is invoked.

Bit 5

Write mode (command) flag.

When 1, write mode operation is invoked.

Bit 6

BS-test mode (command) flag.

When 1, BS-test mode operation is invoked.

Bit 7

Start mode (command) flag.

When 1, start mode operation is invoked.

7. Read command set flags/data

Table 9. Read command format/internal status data

	READ command		Internal status
1	1	1	0
2	0	2	AREA
3	0	3	IDLE MODE
4	0	4	PREAMBLE MODE
5	0	5	LOCK MODE
6	0	6	WRITE MODE
7	0	7	ADET+MDET (Receiving)
8	1	8	BUSY/ READY
9	0	9	0
10	0	10	AREA
11	0	11	IDLE MODE
12	0	12	PREAMBLE MODE
13	0	13	LOCK MODE
14	0	14	WRITE MODE
15	0	15	ADET+MDET (Receiving)
16	0	16	BUSY/ READY

= Indeterminate data = Determinate data

Read command bits 1 to 16

These bits form the decoder read command.

Bits 1 to 8 form the actual command, and bits 9 to 16 are dummy data. While command bits 1 to 8 are being set, data may be output on SDO and can be treated as indeterminate data and ignored. While bits 9 to 16 are being set, however, data output on SDO is valid data.

Internal status bit 1 (read command bit 9)

Internal status output data leading bit.

This bit is always 0.

Internal status bit 2 (read command bit 10)

AREA pin condition flag (when reading internal status data).

When 0, AREA is LOW.

When 1, AREA is HIGH.

Internal status bit 3 (read command bit 11)

Decoder status flag.

When 1, decoder is operating in idle mode.

Internal status bit 4 (read command bit 12)

Decoder status flag.

When 1, decoder is operating in preamble mode.

Internal status bit 5 (read command bit 13)

Decoder status flag.

When 1, decoder is operating in lock mode.

Internal status bit 6 (read command bit 14)

Decoder status flag.

When 1, decoder is operating in write mode.

Internal status bit 7 (read command bit 15)

Decoder status flag.

When 1, decoder is receiving self address or message.

Internal status bit 8 (read command bit 16)

Decoder status flag.

When 1, indicates data write operation to the decoder internal RAM (BUSY in write mode).

Do not write data when this flag is set to 1.

After each 32-bit data is written, READY confirmation is not required before writing subsequent data if a space of 28.4 ms minimum is provided.

Lock Mode Timing Examples

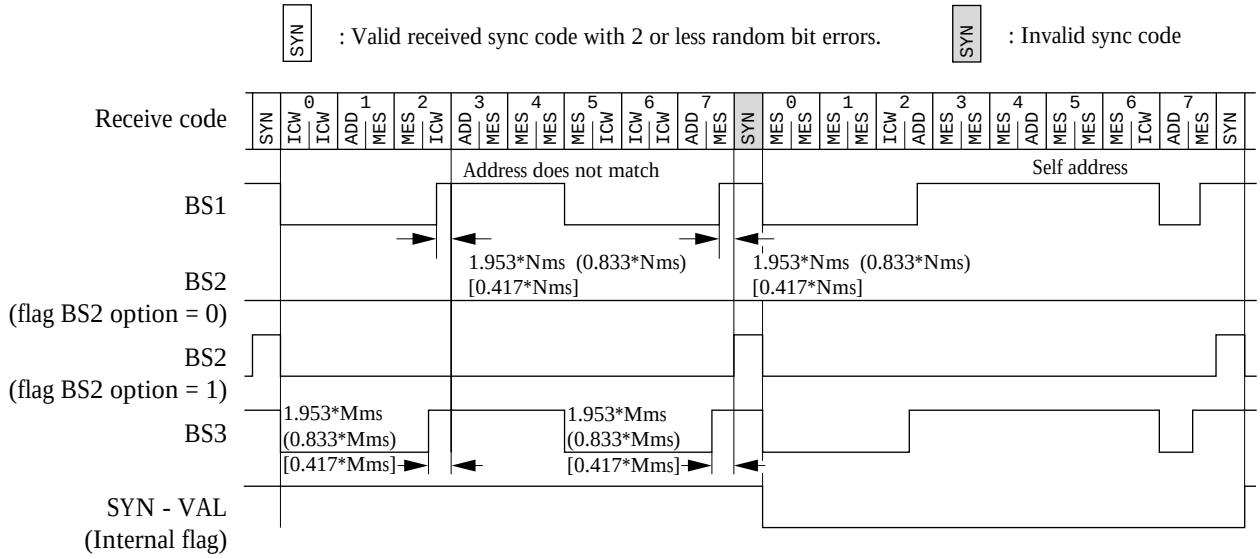


Figure 12. Self frame 3 and 4

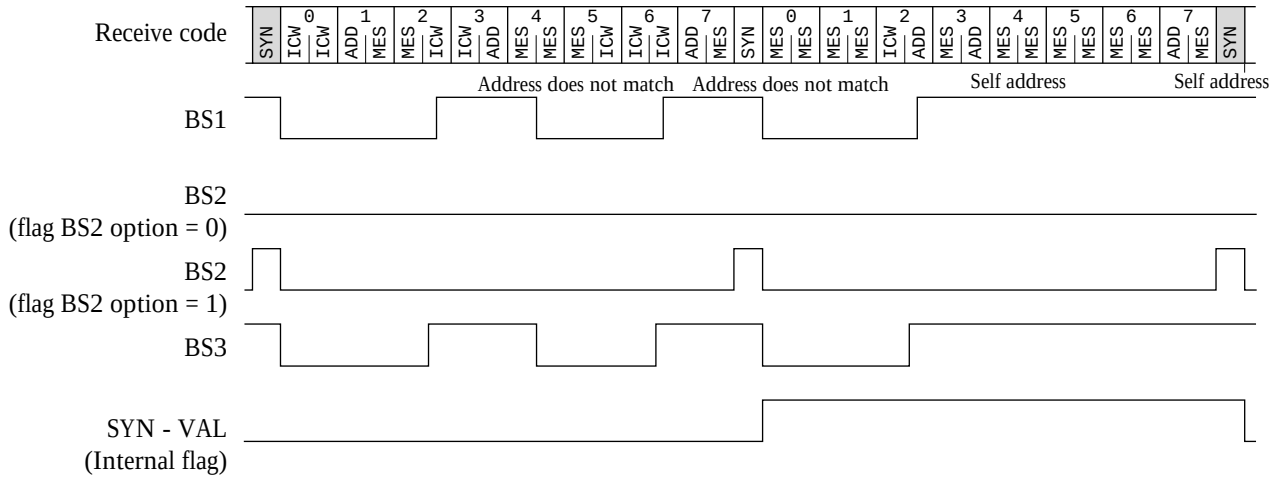


Figure 13. Self frame 3 and 7 (1)

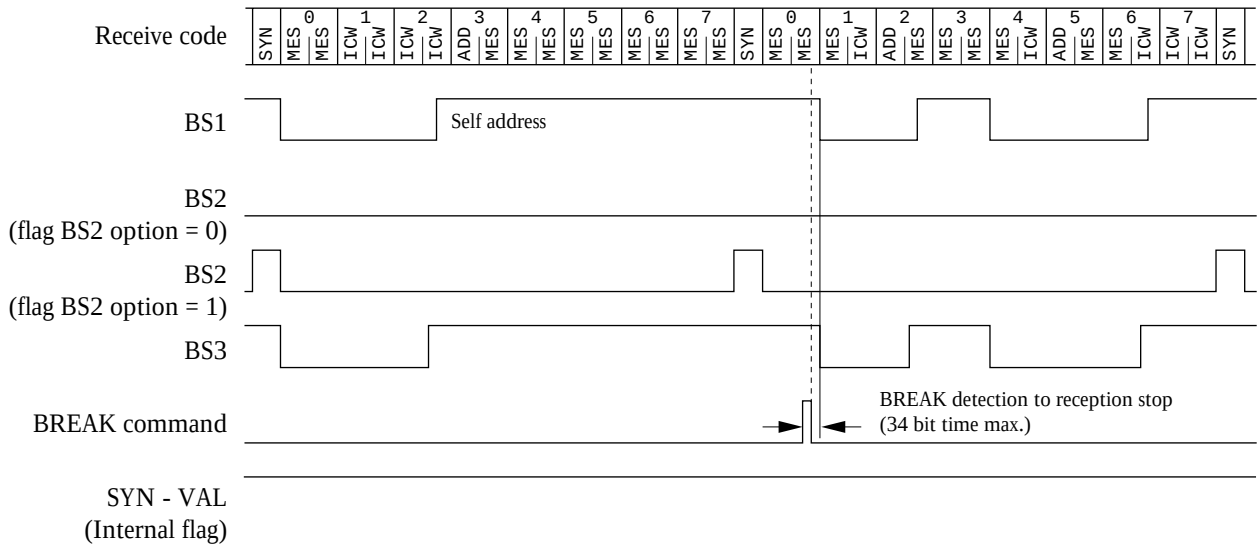
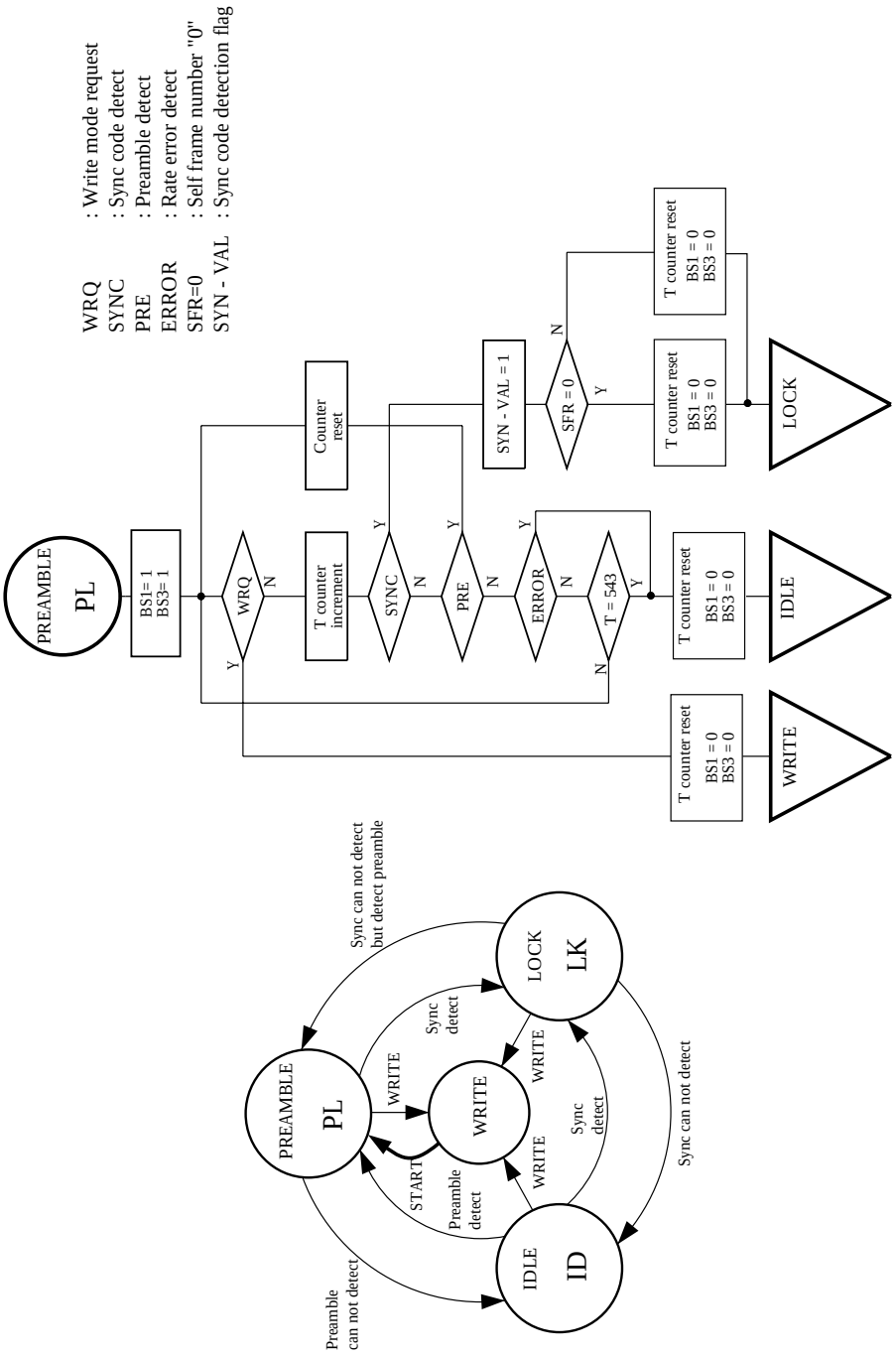
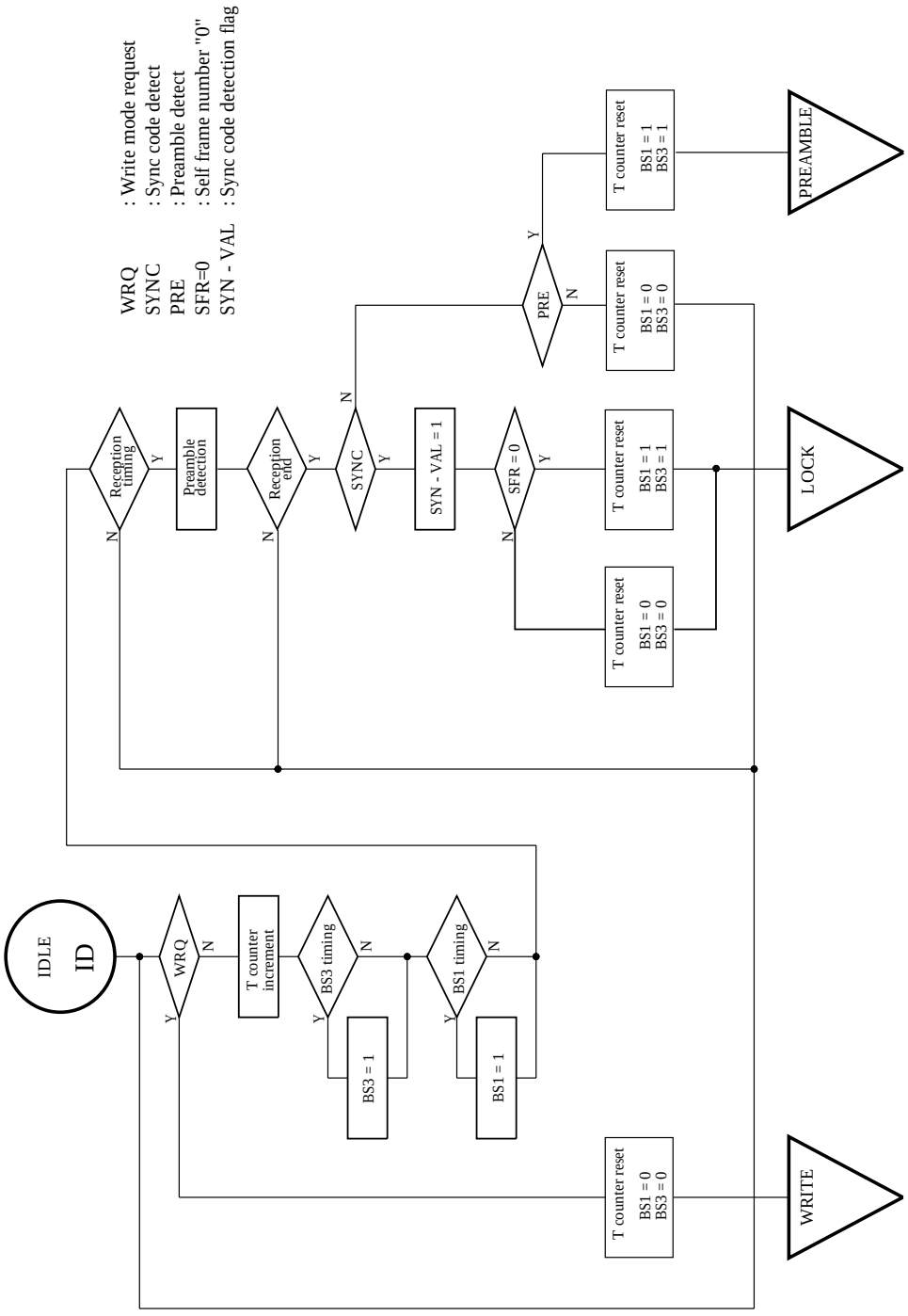
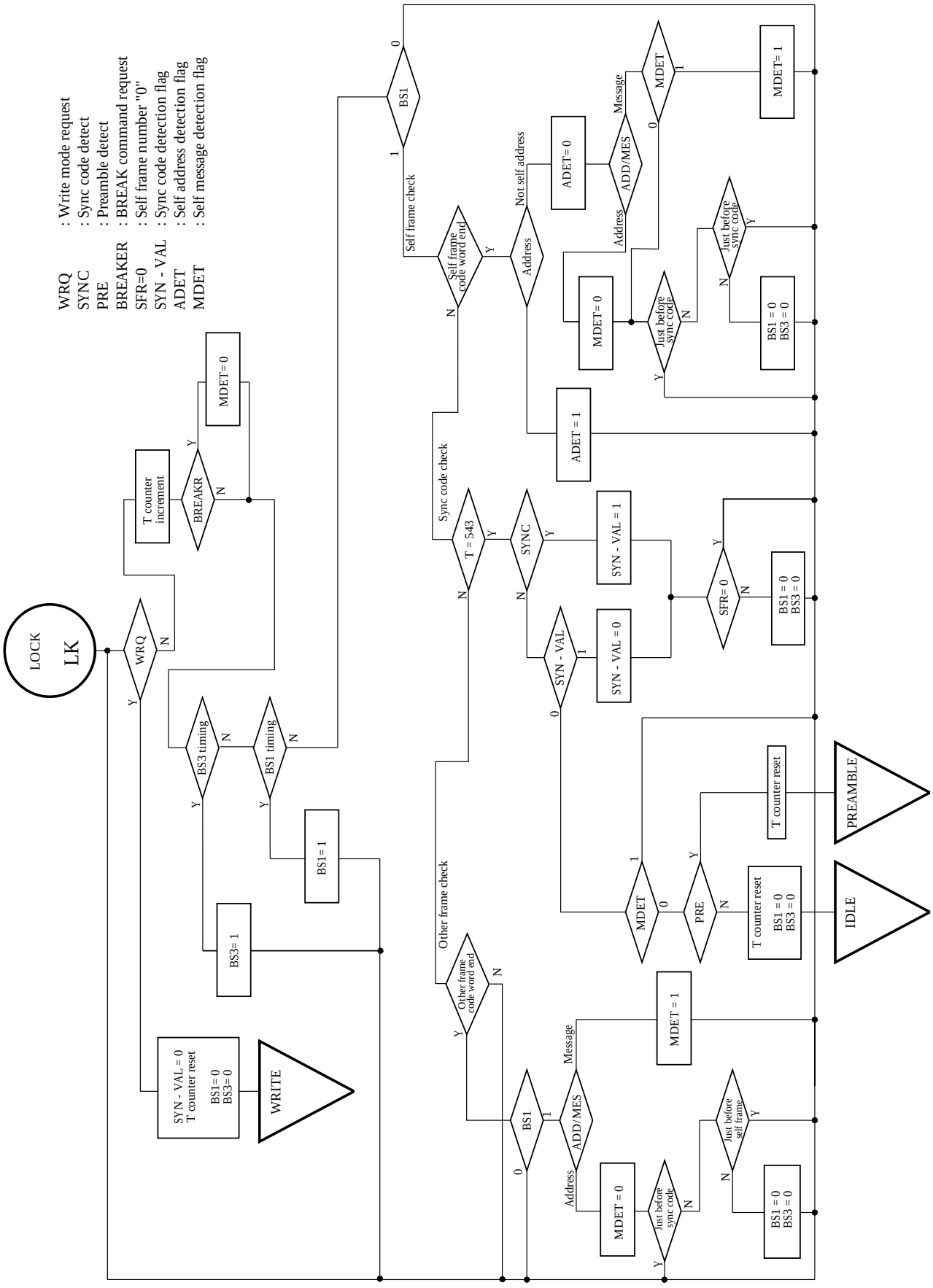


Figure 14. Self frame 3 and 7 (2)

Preamble, Idle, and Lock Mode Signal Flow




WRQ : Write mode request
SYNC : Sync code detect
PRE : Preamble detect
SFR=0 : Self frame number "0"
SYN - VAL : Sync code detection flag
IDLE
ID
WRQ
T counter increment
BS3 timing
BS3 = 1
BS1 timing
BS1 = 1
T counter reset
BS1 = 0
BS3 = 0
WRITE
Reception timing
Preamble detection
Reception end
SYNC
SYN - VAL = 1
SFR = 0
T counter reset
BS1 = 1
BS3 = 1
LOCK
PRE
T counter reset
BS1 = 0
BS3 = 0
T counter reset
BS1 = 1
BS3 = 1
PREAMBLE
Y
N


WRQ : Write mode request
SYNC : Sync code detect
PRE : Preamble detect
BREAKER : BREAK command request
SFR=0 : Self frame number "0"
SYN - VAL : Sync code detection flag
ADET : Self address detection flag
MDET : Self message detection flag
LOCK
LK
WRQ
T counter increment
BREAKR
MDET= 0
BS3 timing
BS1 timing
BS3= 1
BS1= 1
SYN - VAL = 0
T counter reset
BS1= 0
BS3= 0
WRITE
BS1
Self frame check
Self frame code word end
Address
Not self address
ADET= 0
ADD/MES
Message
MDET
MDET= 1
MDET= 0
Just before sync code
BS1 = 0
BS3 = 0
ADET = 1
Sync code check
T = 543
SYNC
SYN - VAL = 1
SYN - VAL = 0
SFR= 0
BS1 = 0
BS3 = 0
Other frame check
Other frame code word end
MDET = 1
MDET = 0
Just before self frame
PRE
T counter reset
BS1 = 0
BS3 = 0
PREAMBLE
IDLE

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