512Kx32 Static RAM CMOS, High Speed Module

FEATURES

- 512Kx32 bit CMOS Static
- Random Access Memory
  - Access Times: 15, 20, and 25ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Package
  - 72 Pin ZIP, No. 173
  - 72 lead SIMM, No. 174 (Gold Option)
  - Common Data Inputs and Outputs
- Single +5V (±10%) Supply Operation

Note: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The EDI8F32512C is a high speed 16 megabit Static RAM module organized as 512K words by 32 bits. This module is constructed from four 512Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables (EØ-E3) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

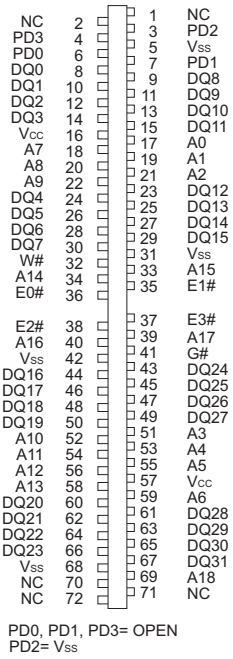
The EDI8F32512C is offered in 72 pin ZIP and 72 lead SIMM packages, which enable 16 megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Pins PD1- PD4, are used to identify module memory density in applications where alternate modules can be interchanged.

FIG. 1

Pin Configurations and Block Diagram

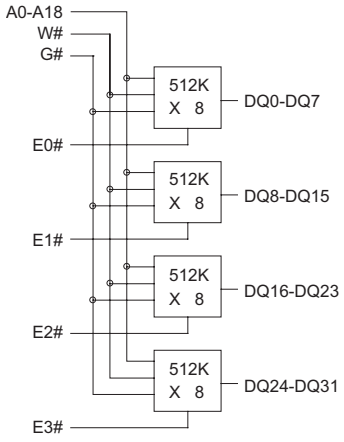


PD0, PD1, PD3= OPEN
PD2= VSS

8G32512C Pin Config.

Pin Names

A0-A18	Address Inputs
E0#-E3#	Chip Enables
W#	Write Enable
G#	Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connectiona



8G32512C Blk Dia.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	5.0 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	--	6.0	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(Note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	$I_{CC}1$	W#, E# = V_{IL}, II/O = 0mA, Min Cycle			800	mA
Standby (TTL) Power Supply Current	$I_{CC}2$	E $\geq$ V_{IH}, $V_{IN} \geq V_{IL}$ or $V_{IN} \geq V_{IH}$			300	mA
Full Standby Power Supply Current CMOS	$I_{CC}3$	E $\geq$ V_{CC}-0.2V $V_{IN} \geq V_{CC}$=0.2V or $V_{IN} \geq$ 0.2V			80	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	--	--	±20	µA
Output Leakage Current	I_{LO}	V I/O = 0V TO V_{CC}	--	--	±20	µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	--	--	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

TRUTH TABLE

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	HIGH Z	$I_{CC}2/I_{CC}3$
L	H	L	Read	D_{OUT}	$I_{CC}1$
L	L	X	Write	D_{IN}	$I_{CC}1$
L	H	H	Output Deselect	HIGH Z	$I_{CC}1$

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	45	pF

These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	TRA	15		20		25		ns
Address Access Time	t_{AVQV}	TAA		15		20		25	ns
Chip Enable Access	t_{ELQV}	TACS		15		20		25	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	TCHZ		6		10		12	ns
Output Hold from Address Change	t_{AVQX}	TOH	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	TOE		6		8		10	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	TOLZ	0		0		0		ns
Output Disable to Output in High (1)	t_{GHQZ}	TOHZ		620		8		10	ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 2
READ CYCLE 1 - W# HIGH, G#, E# LOW

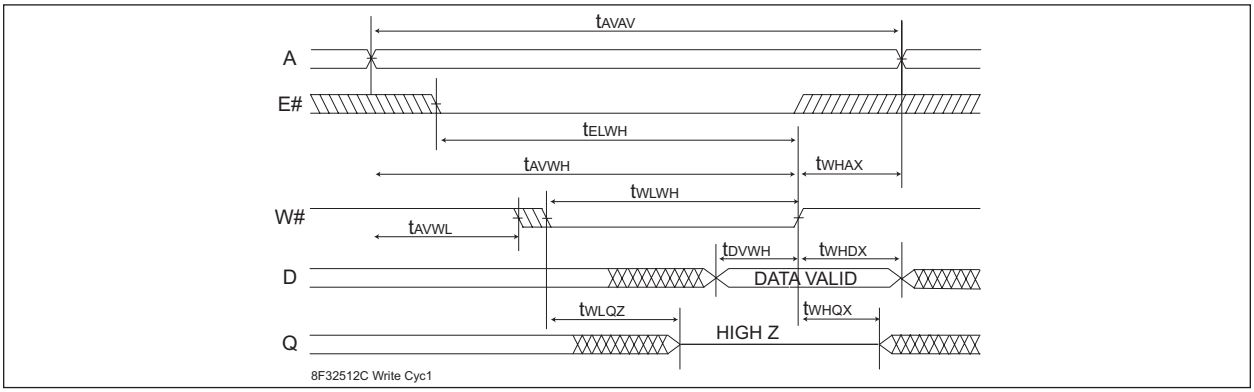
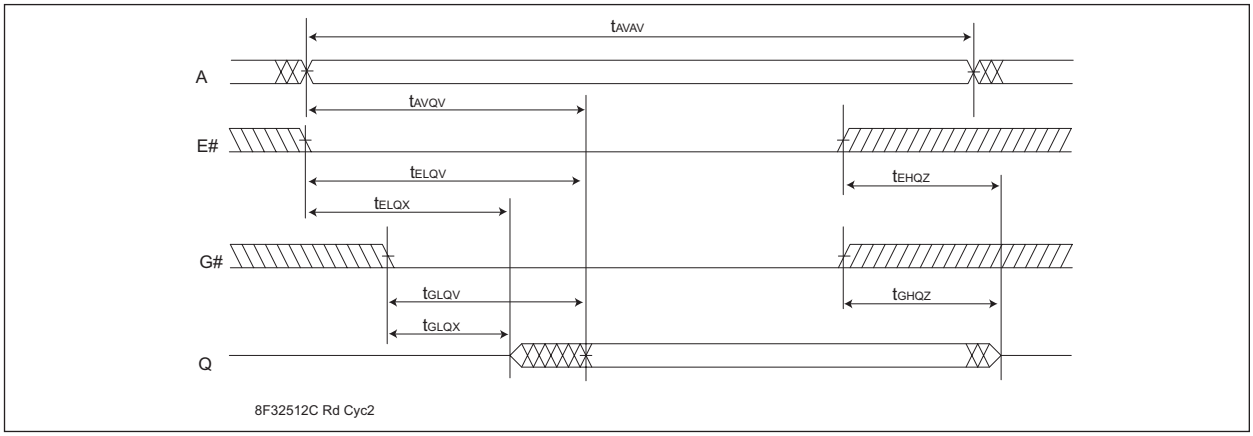


FIG. 3
READ CYCLE 2 - W# HIGH



AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	TWC	15		20		25		ns
Chip Enable to End of Write	t_{ELWH}	TCW	8		15		20		ns
	t_{WLEH}	TCW	8		15		20		ns
Address Setup Time	t_{AVWL}	TAS	0		0		0		ns
	t_{AVEL}	TAS	0		0		0		ns
Address Valid to End of Write	t_{AVWH}	TAW	8		15		15		ns
	t_{AHEH}	TAW	8		15		15		ns
Write Pulse Width	t_{WLWH}	TWP	10		15		15		ns
	t_{ELEH}	TWP	10		15		15		ns
Write Recovery Time	t_{WHAX}	TWR	0		0		0		ns
	t_{EHAX}	TWR	0		0		0		ns
Data Hold Time	t_{WHDX}	TDH	0		0		0		ns
	t_{EHDX}	TDH	0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	TWHZ	0	6	0	8	0	12	ns
Data to Write Time	t_{DVWH}	TDW	7		9		10		ns
	t_{DVEH}	TDW	7		9		10		ns
Output Active from End of Write (1)	t_{WHQX}	TWLZ	3		3		3		ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 4

WRITE CYCLE 1 - W# CONTROLLED

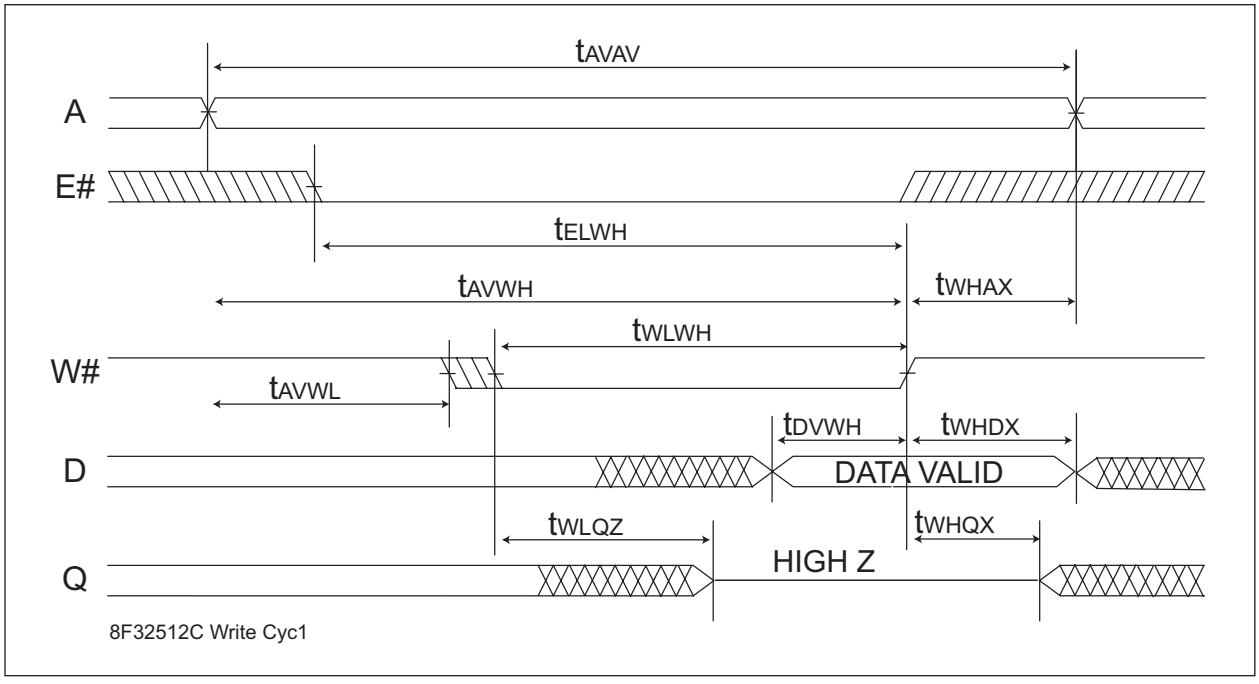
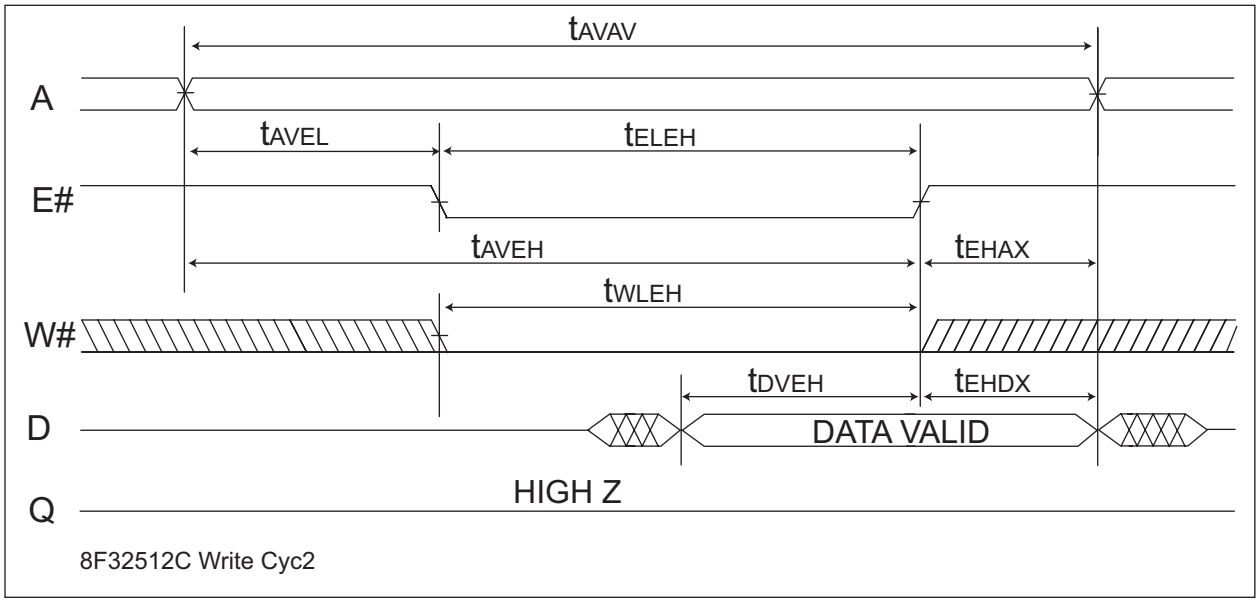


FIG. 5

WRITE CYCLE 2 - E# CONTROLLED



ORDERING INFORMATION

Part Number	Speed (ns)	Package No.
EDI8F32512C15MMC	15	174
EDI8F32512C20MMC	20	174
EDI8F32512C25MMC	25	174

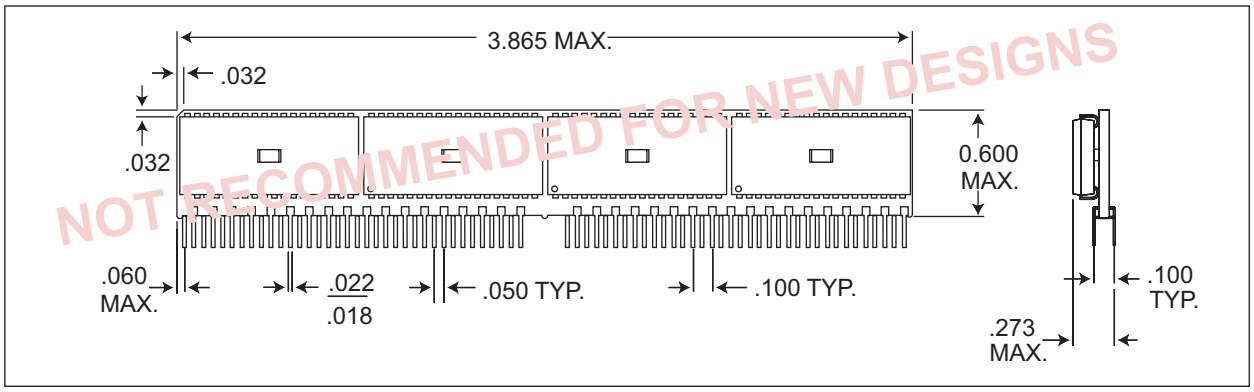
Part Number	Speed (ns)	Package No.
EDI8F32512C15MZC	15	173
EDI8F32512C20MZC	20	173
EDI8F32512C25MZC	25	173

NOTES:

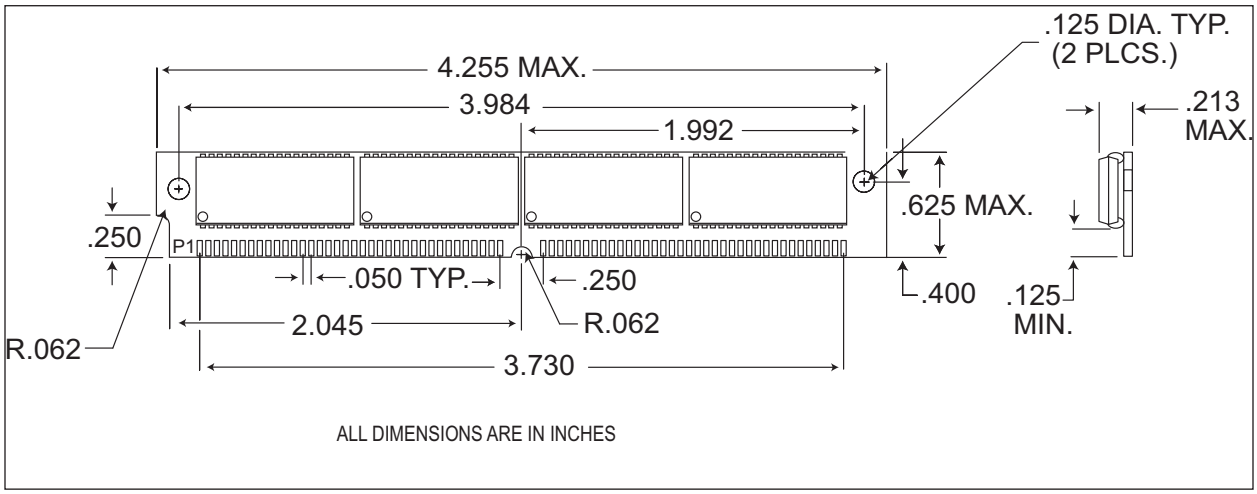
- Consult Factory for availability of RoHS compliant products. (indicated with "G" at the end of the part number)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option
- To order gold SIMM option, change from "EDI8F" to "EDI8G".

PACKAGE DESCRPTION

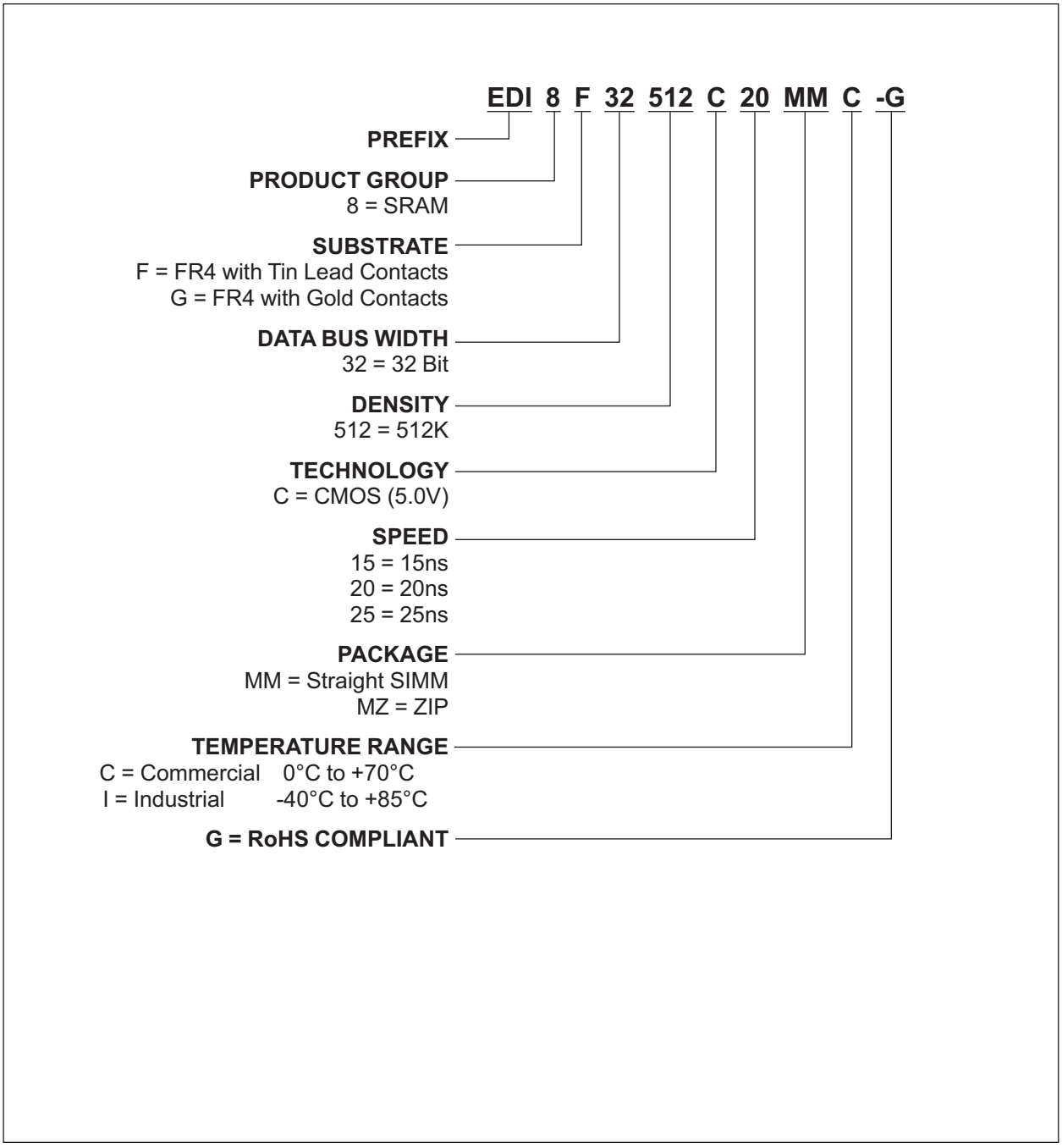
PACKAGE NO. 173: 72 PIN ZIP



PACKAGE NO. 174: 72 LEAD SIMM



PART NUMBERING GUIDE



Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 9	9.1 Added RoHS compliance option	March 2006	Final
	9.2 Offer vendor source control		
	9.3 Provide industrial temperature option		
	9.4 Added part number guide		
	9.5 Added document title page		