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The WL600C is a 2.4-2.5GHz RF transmitter and receiver chip for use in digital radio, and operates from a supply voltage of 2.7 - 3.6V. It is designed to work with the Zarlink Semiconductor WL800 frequency synthesiser and the WL102 WLAN controller chip which together make up the DE6038 frequency hopping Wireless Local Area Network (WLAN) transceiver.

The receiver circuit contains a low noise amplifier, image rejecting mixer, IF limiting strip with RSSI and a quadrature demodulator. There is also a power amplifier driver stage and ramp control facility for use in transmit.

Features

- Part of DE6038 chipset (WL800, WL102)
- High level of integration
- Low noise figure
- Low power consumption
- High data rates with comparator for 2 level FSK
- Minimal external components
- 48 lead LQFP package

Absolute Maximum Ratings

Supply voltage Vcc	4V
Transmit/Receive and standby input	-0.5 to Vcc +0.5V
Current consumption	TBD
Junction temperature Tj	150°
ESD protection	2KV

Related Documents

Datasheets WL800/102 DE6038

DS4581

ISSUE 2.1

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Ordering Information

WL600C/KG/GP1R

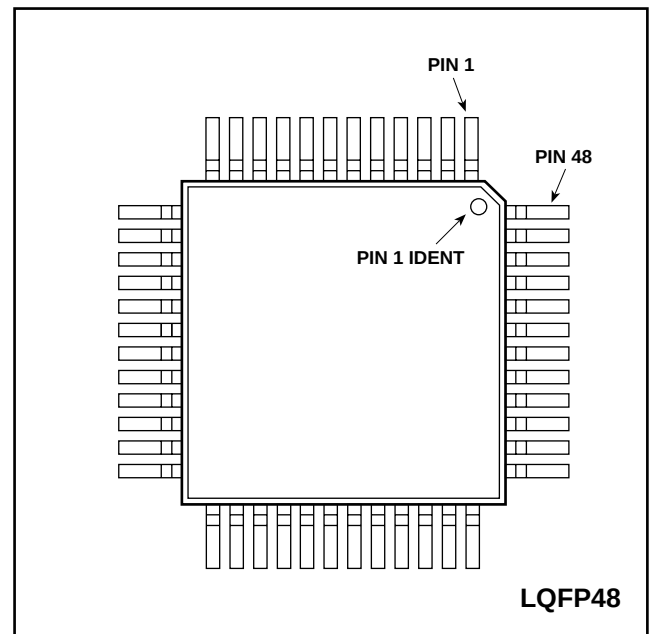


Figure 1 - Pin connections - top view

Pin	Description	Pin	Description
1	QUAD+	25	VCC_RF
2	QUAD-	26	GND_RF
3	GND_IF	27	VCC_LNA
4	DEMOD_OUT+	28	GND_RF
5	DEMOD_OUT-	29	RF_IN
6	RSSI	30	LNA_DEGEN
7	CLAMP_SET	31	LNA_DEGEN
8	CCA_THRESHOLD	32	DRIVE
9	VCC_IFSTRIP	33	VCC_PA
10	DECOUPLE_LOG-	34	GND_RF
11	DECOUPLE_LOG+	35	RAMP_CAP
12	IF_IN+	36	PA_ON
13	IF_IN-	37	STDBYB
14	CCAB	38	TX/RXB
15	GND_IF	39	GND_LO
16	BUFFER_IN+	40	LO_IN
17	BUFFER_IN-	41	VCC_LO
18	VCC_DATA	42	DATA_IN+
19	RXD	43	DATA_IN-
20	RXDB	44	BUFFER_OUT-
21	GND_RF	45	BUFFER_OUT+
22	IF_OUT-	46	CLAMP-
23	IF_OUT+	47	CLAMP+
24	GND_PADDLE	48	GND_PADDLE

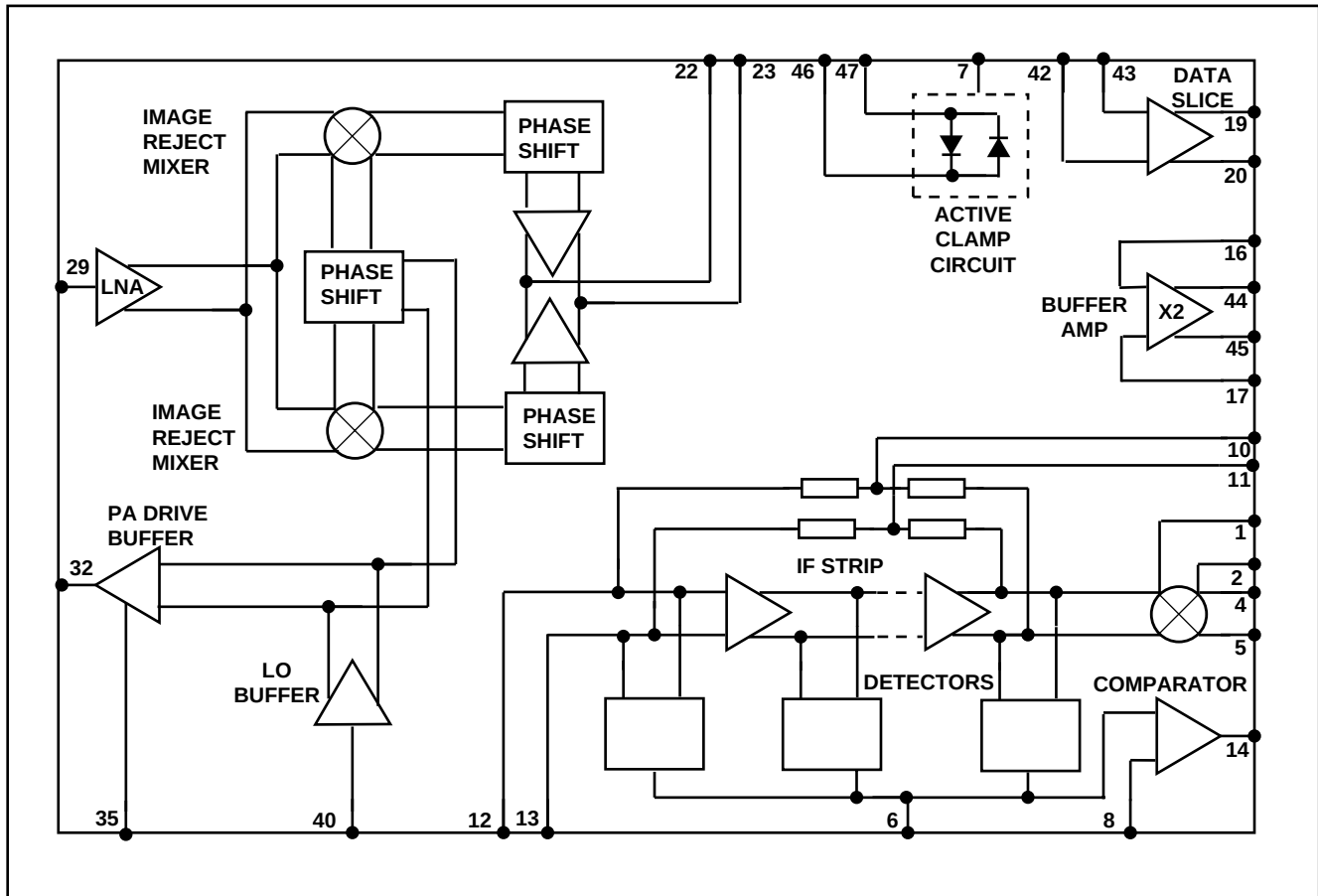


Figure 2 - WL600C block diagram

DEVICE PIN OUT

Pin	Ref	Type	Description
1	QUAD+	I/O	Quadrature demodulator tank circuit connection
2	QUAD -	I/O	Quadrature demodulator tank circuit connection
3	GND_IF	GND	Ground for IF strip circuitry
4	DEMOD_OUT +	OUT	Demodulator output
5	DEMOD_OUT -	OUT	Demodulator output
6	RSSI	OUT	RSSI detector analogue output
7	CLAMP_SET	IN	Sets clamp knee voltage
8	CCA_THRESHOLD	IN	Sets level at which CCA comparator will switch
9	VCC_IFSTRIP	VCC	Power supply for log amp, demod, and internal references
10	DECOUPLE_LOG -	I/O	Decoupling for log amp feedback network, AC couple
11	DECOUPLE_LOG +	I/O	Decoupling for log amp feedback network, AC couple
12	IF_IN +	IN	Log amp input, AC couple
13	IF_IN -	IN	Log amp input, AC couple
14	CCAB	OUT	CCA comparator output: signal = logic high, clear = logic low
15	GND_IF	GND	Ground for IF strip circuitry
16	BUFFER_IN +	IN	x 2 buffer input
17	BUFFER_IN -	IN	x 2 buffer input
18	VCC_DATA	VCC	Power supply for clamp, data comparator and buffer amp
19	RXD	OUT	Data comparator output

Pin	Ref	Type	Description
20	RXDB	OUT	Data comparator output
21	GND_RF	GND	Ground for LNA, mixer, IF summation, and PA driver circuits
22	IF_OUT-	OUT	Downconverter output, requires external load and RFC
23	IF_OUT+	OUT	Downconverter output, requires external load and RFC
24	GND_PADDLE	GND	Ground for substrate and package paddle
25	VCC_RF	VCC	Power supply for mixer, summation, and PA ramp circuits
26	GND_RF	GND	Ground for LNA, mixer, IF summation, and PA driver circuits
27	VCC_LNA	VCC	Power supply for LNA
28	GND_RF	GND	Ground for LNA, mixer, IF summation, and PA driver circuits
29	RF_IN	IN	LNA input, AC couple
30	LNA_DEGEN	I/O	LNA degeneration, connect to ground
31	LNA_DEGEN	I/O	LNA degeneration, connect to ground
32	DRIVE	OUT	Power amplifier driver output, requires external load and RFC
33	VCC_PA	VCC	Power supply for power amplifier driver
34	GND_RF	GND	Ground for LNA, mixer, IF summation, and PA driver circuits
35	RAMP_CAP	I/O	PA ramp circuit timing capacitor connection
36	PA_ON	IN	PA ramp circuit control input: PA on = logic high, PA off = logic low
37	STDBYB	IN	Power down control input: active= logic high, standby = logic low
38	TX/RXB	IN	Transmit/Receive control input: transmit = logic high, receive = logic low
39	GND_LO	GND	Ground for LO buffer, phaseshifter, and standby circuitry
40	LO_IN	IN	Local oscillator input, AC couple
41	VCC_LO	VCC	Power supply for LO buffer, phaseshifter, and standby circuitry
42	DATA_IN+	IN	Data comparator input
43	DATA_IN-	IN	Data comparator input
44	BUFFER_OUT-	OUT	x2 buffer output
45	BUFFER_OUT+	OUT	x2 buffer output
46	CLAMP -	I/O	Data clamp, knee voltage set by pin 7, AC couple
47	CLAMP +	I/O	Data clamp, knee voltage set by pin 7, AC couple
48	GND_PADDLE	GND	Ground for substrate and package paddle

Electrical Characteristics

These characteristics are guaranteed over the following conditions (unless otherwise stated):

$$T_{AMB} = -20^{\circ}\text{C to } +85^{\circ}\text{C } V_{CC} = 2.7\text{V to } 3.6\text{V,}$$

Characteristic		Value		Unit	Condition
	Min	Typ	Max		
Supply current (transmit)		50		mA	
Supply current (Receive)		60		mA	
Supply current in standby		0.3		mA	
PA DRIVER & RAMP CIRCUIT					
Logic low voltage	0		0.8	V	Ramp down
Logic high voltage	Vcc-0.7		Vcc	V	Ramp up
Logic Input current			10	μA	
Ramp capacitor charge Current		250		μA	
Ramp capacitor voltage swing		1		V	
Output power	-2		2	dBm	
Output band	2.4		2.5	GHz	
Max to Min power out ratio	20			dB	
RECEIVER LOW NOISE AMPLIFIER & MIXERS					
Conversion gain	19	22		dB	Differential into 600Ohms
3rd order intercept point	-10			dBm	
1dB input gain compression	-22			dBm	
Noise figure		7	10	dB	Matched to 50Ohms
Input impedance 2.4GHz		13+j20		Ohms	
2.45GHz		15+j30			
2.5GHz		20+j50			
Image frequency rejection	25			dB	
Local oscillator input level		-16		dBm	
Local oscillator input impedance		15-j40		Ohms	
IF output impedance		600		Ohms	With external 900Ω resistor
TRANSMIT/RECEIVE INPUT					
Logic low voltage	0		0.8	V	Receive mode
Logic high voltage	Vcc-0.7		Vcc	V	Transmit mode
Input current			10	μA	

Electrical Characteristics (cont)

These characteristics are guaranteed over the following conditions (unless otherwise stated):

$$T_{AMB} = -20^{\circ}\text{C to } +85^{\circ}\text{C } V_{CC} = 2.7\text{V to } 3.6\text{V},$$

Characteristic	Value			Unit	Condition
	Min	Typ	Max		
LIMITING STRIP					
Maximum input frequency			50	MHz	Set by external 1k8 resistor
Noise figure		3.5	6	dB	
Input resistance		1200		Ohms	
Capacitance			0.5	pF	
Limiting strip gain		70		dB	
Limiting point		-78	-75	dBm	
RSSI					
Rise time	100			ns	Input = 0dBm
Non linearity			±3	dB	
Maximum output voltage		1.9		V	
Output voltage @ -70dBm input		1.3		V	
Output impedance		6		kOhms	
CLEAR CHANNEL ASSESSMENT COMPARATOR					
Logic high voltage	2.2			V	
Logic low voltage			0.5	V	
Threshold input limits	1		2	V	
Input current			1	µA	
DEMODULATOR					
Detect output voltage		0.4		Vp-p	Differential. 150kHz deviation Quad circuit (2.2µH/40kΩ) Dependent on Quad circuit
Detected signal bandwidth		3		MHz	
Output pull down current		350		µA	
Output DC common mode		Vcc-1.5		V	
CLAMP CIRCUIT					
Knee voltage range	0.1		0.350	V	Inversely proportional to knee voltage
Clamp set range	1		2	V	
DC bias at inputs		Vcc-1		V	
Slope resistance		100		Ohms	
OUTPUT COMPARATOR					
Input offset voltage			5	mV	For load capacitance 0-10pF pk-pk differential
Input current			1	µA	
Output rise/fall time	11	15	20	ns	
Output voltage swing		400		mV	
Input common mode range	1		Vcc-0.7	V	
Output common mode		Vcc-0.85		V	

Electrical Characteristics (cont)

These characteristics are guaranteed over the following conditions (unless otherwise stated):

$$T_{AMB} = -20^{\circ}\text{C to } +85^{\circ}\text{C } V_{CC} = 2.7\text{V to } 3.6\text{V,}$$

Characteristic	Value			Unit	Condition
	Min	Typ	Max		
BUFFER AMP					
Buffer amplifier gain		2			
Input common mode range	1.2		V _{CC} -0.5	V	
Output common mode		V _{CC} -1.5		V	
Max difference between inputs			450	mV	
Output pull down current		350		μA	Amp will limit outside this range
STANDBY INPUT					
Logic low voltage	0		0.8	V	Chip must be in receive mode
Logic high voltage	V _{CC} -0.7		V _{CC}	V	when switching to/from standby
Input current		100		μA	Circuit powered down
Standby to receive time				μs	Circuit powered up

Functional Description

Receive

The RF input stage of the WL600C receiver is a 2.5GHz low noise amplifier (LNA). The output of the single ended LNA is split and fed into the inputs of two mixers which form an image rejecting down converter. An external oscillator (2.357 → 2.457GHz) is fed through an RC phase shift network to provide the required quadrature local oscillator signal.

The mixer outputs are fed through further phase shift networks and are combined to form a differential 43MHz IF signal which is used to drive the 43MHz SAW filter.

The output of the SAW filter is fed into a differential limiting strip which provides the IF gain. The strip has a series of detectors whose output provides an analog voltage indicating receive signal strength (RSSI). Alternatively, for basic applications a comparator connected to the RSSI detectors can be used. When the RSSI signal is greater than a value set by the CCA_THRESHOLD input the clear channel assessment (CCAB) output goes high.

A conventional quadrature demodulator (with external tuned circuit to supply the quadrature drive) provides the analogue data stream which is then AC coupled to a data slice comparator. A clamp circuit is connected between the comparator inputs to provide DC restoration of the AC coupled signal. The comparator output then goes to the data and clock recovery circuits on a CMOS integrated circuit (such as the WL102).

Transmit

The local oscillator signal is also used in transmit at a higher frequency (2.4 → 2.5GHz) and is buffered and amplified on the WL600C. This provides the drive to the transmit power amplifier (also off chip).

A ramp circuit is included to control the drive level to the power amplifier in a controlled manner. This is done at the start and end of a transmit sequence and should be used to prevent the generation of spectral "splash". A single external capacitor controls the rate of increase and decrease of the power drive level.

Control Waveforms

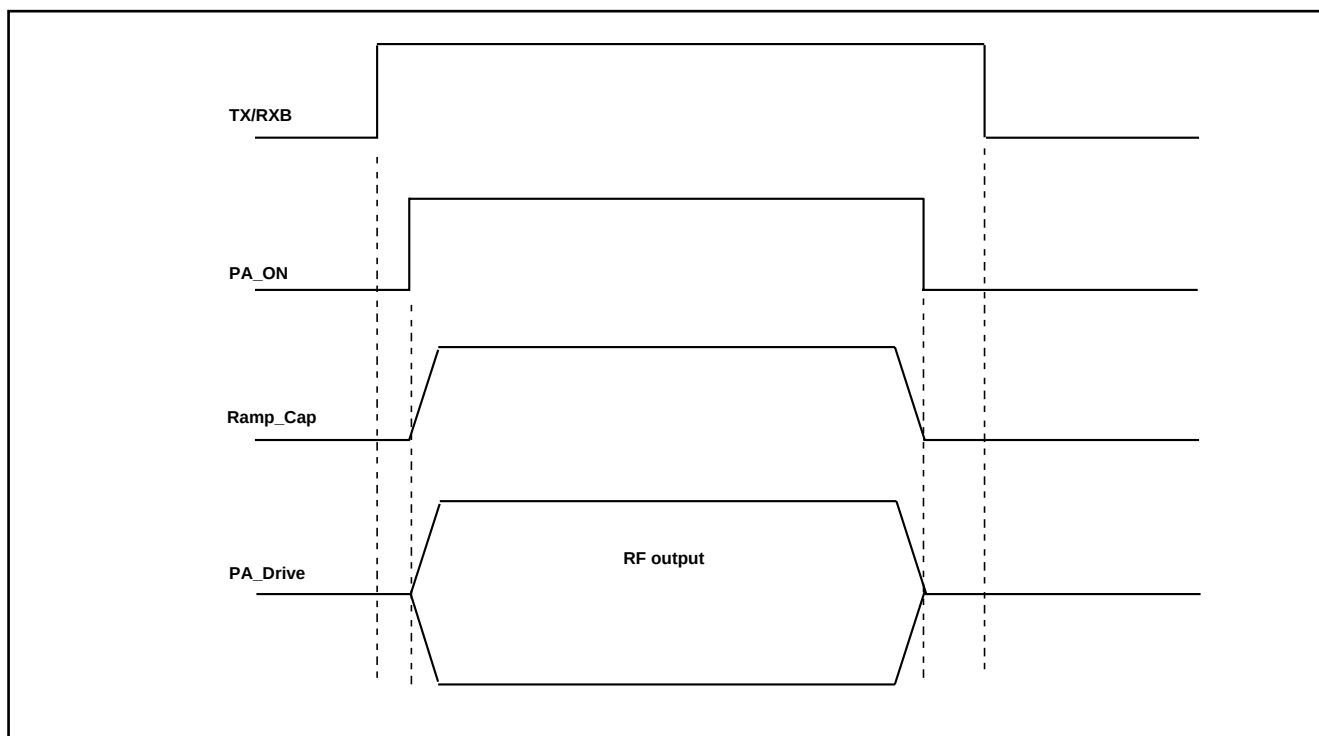
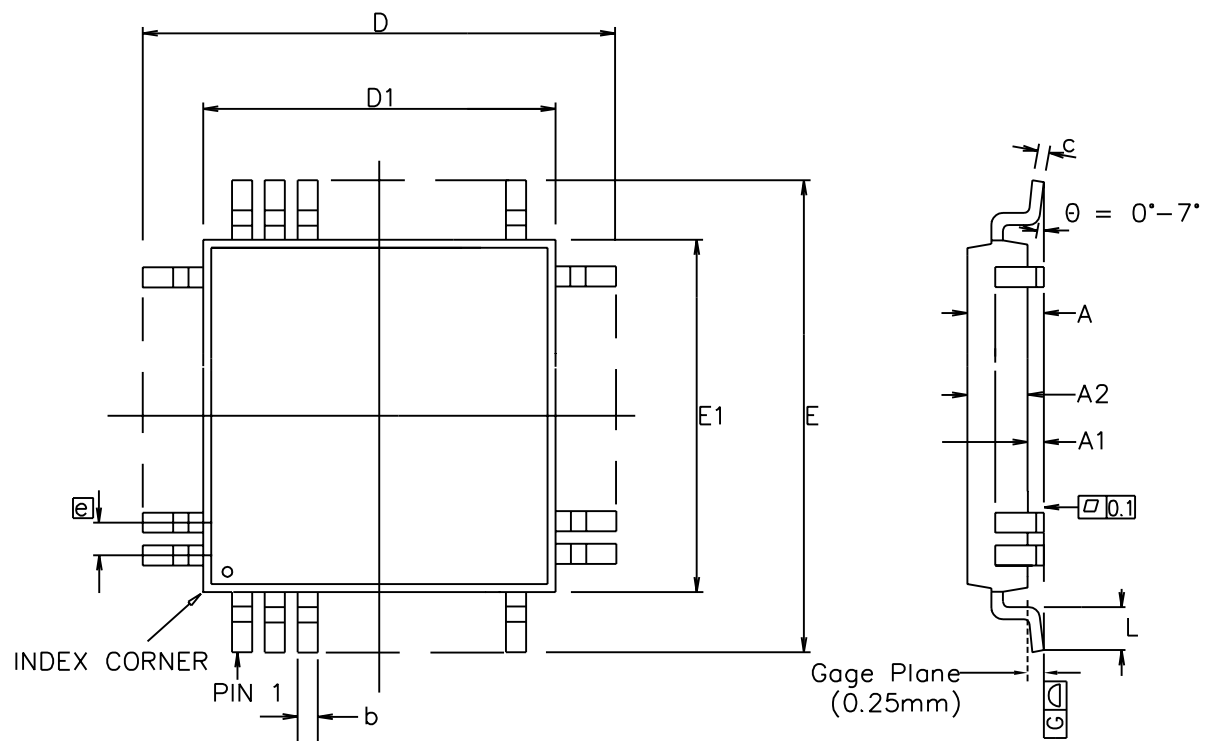


Figure 3 - Transmit control waveforms

Control Logic

Control Line	Logic '0'	Logic '1'
TX/RXB	Receive	Transmit
PA_ON	PA off	PA on
STDBYB	Standby	Active



Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

Symbol	Control Dimensions in millimetres		Altern. Dimensions in inches	
	MIN	MAX	MIN	MAX
A	---	1.60	---	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
D	9.00	BSC	0.354	BSC
D1	7.00	BSC	0.276	BSC
E	9.00	BSC	0.354	BSC
E1	7.00	BSC	0.276	BSC
L	0.45	0.75	0.018	0.030
e	0.50	BSC	0.020	BSC
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
Pin features				
N	48			
ND	12			
NE	12			
NOTE	SQUARE			

Conforms to JEDEC MS-026 BBC Iss. C

This drawing supersedes 418/ED/51210/017 (Swindon)

© Zarlink Semiconductor 2002 All rights reserved.					Package Code QC	
ISSUE	1	2	3	4	Previous package codes GP / B	Package Outline for 48 lead LQFP (7 x 7 x 1.4mm) 2.0mm Footprint
ACN	201364	203413	207116	212440		
DATE	28Oct96	4Nov97	9Jul99	25Mar02		GPD00248
APPRD.						





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