MAX7034

315MHz/434MHz ASK Superheterodyne Receiver

General Description

The MAX7034 fully integrated low-power CMOS superheterodyne receiver is ideal for receiving amplitude-shift-keyed (ASK) data in the 300MHz to 450MHz frequency range (including the popular 315MHz and 433.92MHz frequencies). The receiver has an RF sensitivity of -114dBm. With few external components and a low-current power-down mode, it is ideal for cost-sensitive and power-sensitive applications typical in the automotive and consumer markets. The MAX7034 consists of a low-noise amplifier (LNA), a fully differential image-rejection mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO), a 10.7MHz IF limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data-recovery circuitry.

The MAX7034 is available in a 28-pin (9.7mm x 4.4mm) TSSOP package and is specified over the automotive (-40°C to +125°C) temperature range.

Applications

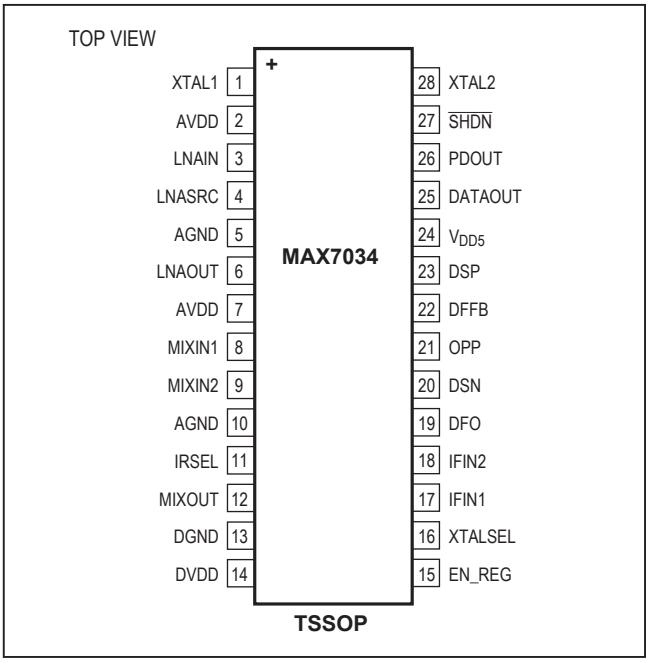
- Automotive Remote Keyless Entry
- Security Systems
- Garage Door Openers
- Home Automation
- Remote Controls
- Local Telemetry
- Wireless Sensors

Features

- Optimized for 315MHz or 433.92MHz Band
- Operates from Single +3.3V/+5.0V Supply
- Selectable Image-Rejection Center Frequency
- Selectable x64 or x32 f_{LO}/f_{XTAL} Ratio
- Low (< 6.7mA) Operating Supply Current
- < 3.0µA Low-Current Power-Down Mode for Efficient Power Cycling
- 250µs Startup Time
- Built-In 44dB RF Image Rejection
- Excellent Receive Sensitivity Over Temperature
- -40°C to +125°C Operation
- -40°C to +105°C Operation (3.0V to 3.6V Supply)

***Ordering Information* and *Typical Application Circuit* appear at end of data sheet.**

Pin Configuration



19-3109; Rev 4; 11/16

Absolute Maximum Ratings

V_{DD5} to AGND .....-0.3V to +6.0V
AVDD to AGND .....-0.3V to +4.0V
DVDD to DGND.....-0.3V to +4.0V
AGND to DGND .....-0.1V to +0.1V
IRSEL, DATAOUT, XTALSEL, $\overline{SHDN}$, EN_REG to AGND ..... -0.3V to (V_{DD5} + 0.3V)
All Other Pins to AGND.....-0.3V to (V_{DVDD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 12.8mW/°C above +70°C) ..1025.6mW
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(*Typical Application Circuit*, V_{DD5} = +4.5V to +5.5V, no RF signal applied. T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD5} = +5.0V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD5}	+5.0V nominal supply voltage		4.5	5.0	5.5	V
Supply Current	I_{DD}	$V_{\overline{SHDN}}$ = V_{DD5}	f_{RF} = 315MHz		6.7	8.2	mA
			f_{RF} = 433MHz		7.2	8.7	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V			3	8	µA
Input-Voltage Low	V_{IL}					0.4	V
Input-Voltage High	V_{IH}	EN_REG, SHDN		V_{DD5} - 0.4			V
		XTALSEL		V_{DVDD} - 0.4			
Input Logic Current High	I_{IH}				15		µA
Image-Reject Select Voltage (Note 2)		f_{RF} = 433MHz, V_{IRSEL} = V_{DVDD}		V_{DVDD} - 0.4			V
		f_{RF} = 375MHz, V_{IRSEL} = V_{DVDD}/2		1.1		V_{DVDD} - 1.5	
		f_{RF} = 315MHz, V_{IRSEL} = 0V				0.4	
DATAOUT Voltage-Output Low	V_{OL}	I_{SINK} = 10µA			0.125		V
DATAOUT Voltage-Output High	V_{OH}	I_{SOURCE} = 10µA		V_{DD5} - 0.125			V

AC Electrical Characteristics

(*Typical Application Circuit*, V_{DD5} = +4.5V to +5.5V, all RF inputs are referenced to 50Ω, f_{RF} = 433.92MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD5} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Startup Time	t_{ON}	Time for valid signal detection after $V_{\overline{SHDN}}$ = V_{DD5}. Does not include baseband filter settling.		250		µs
Receiver Input Frequency Range	f_{RF}		300		450	MHz
Maximum Receiver Input Level				0		dBm
Sensitivity at T_A = +25°C (Note 3)		315MHz		-114		dBm
		434MHz		-113		
Sensitivity at T_A = +125°C (Note 3)		315MHz		-113		dBm
		434MHz		-110		
Maximum Data Rate		Manchester coded		33		kbps
		NRZ coded		66		
LNA/MIXER						
LNA/Mixer Voltage Gain (Note 4)		330Ω IF filter load		45		dB
LNA/Mixer Input-Referred 1dB Compression Point				-50		dBm
Mixer Output Impedance	Z_{OUT_MIX}			330		Ω
Mixer Image Rejection		f_{RF} = 434MHz, V_{IRSEL} = V_{DVDD}		42		dB
		f_{RF} = 375MHz, V_{IRSEL} = V_{DVDD}/2		44		
		f_{RF} = 315MHz, V_{IRSEL} = 0V		44		
INTERMEDIATE FREQUENCY (IF)						
Input Impedance	Z_{IN_IF}			330		Ω
Operating Frequency	f_{IF}	Bandpass response		10.7		MHz
3dB Bandwidth				10		MHz
RSSI Linearity				±0.5		dB
RSSI Dynamic Range				80		dB
RSSI Level		P_{RFIN} < -120dBm		1.15		V
		P_{RFIN} > -40dBm		2.2		

AC Electrical Characteristics (continued)

(*Typical Application Circuit*, V_{DD5} = +4.5V to +5.5V, all RF inputs are referenced to 50Ω, f_{RF} = 433.92MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD5} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DATA FILTER							
Maximum Bandwidth					50		kHz
DATA SLICER							
Comparator Bandwidth					100		kHz
Output High Voltage					V_{DD5}		V
Output Low Voltage					0		V
CRYSTAL OSCILLATOR							
Crystal Frequency (Note 5)	f_{XTAL}	f_{RF} = 433.92MHz	$V_{XTALSEL}$ = 0V		6.6128		MHz
			$V_{XTALSEL}$ = V_{DVDD}		13.2256		
		f_{RF} = 315MHz	$V_{XTALSEL}$ = 0V		4.7547		
			$V_{XTALSEL}$ = V_{DVDD}		9.5094		
Crystal Tolerance					50		ppm
Input Capacitance		From each pin to ground			6.2		pF
Maximum Load Capacitance	C_{LOAD}				10		pF

Note 1: 100% tested at T_A = +125°C. Guaranteed by design and characterization over entire temperature range.

Note 2: IRSEL is internally set to 375MHz IR mode. It can be left open when the 375MHz image-rejection setting is desired. Bypass to AGND with a 1nF capacitor in a noisy environment.

Note 3: Peak power level. BER = 2 x 10-3, Manchester encoded, data rate = 4kbps, IF bandwidth = 280kHz.

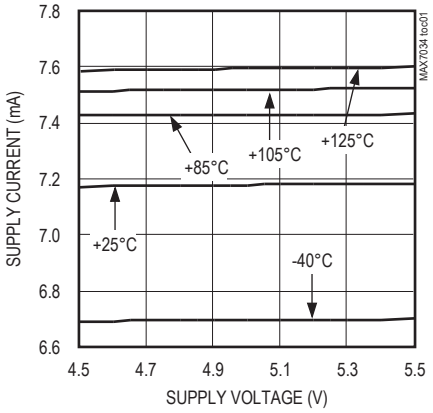
Note 4: The voltage conversion gain is measured with the LNA input matching inductor and the LNA/Mixer resonator in place, and does not include the IF filter insertion loss.

Note 5: Crystal oscillator frequency for other RF carrier frequency within the 300MHz to 450MHz range is (f_{RF} - 10.7MHz)/64 for XTALSEL = 0V, and (f_{RF} - 10.7MHz)/32 for XTALSEL = V_{DVDD}.

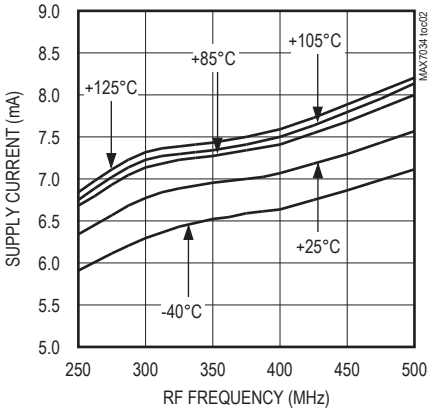
Typical Operating Characteristics

(*Typical Application Circuit*, V_{DD5} = +5.0V, f_{RF} = 433.92MHz, T_A = +25°C, unless otherwise noted.)

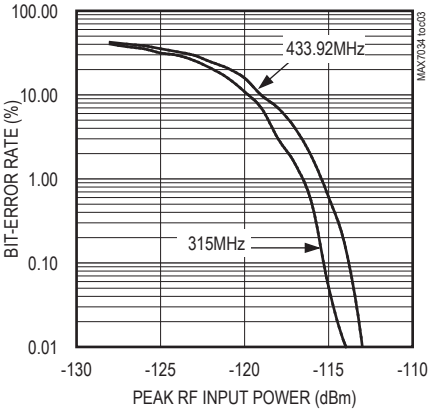
SUPPLY CURRENT vs. SUPPLY VOLTAGE



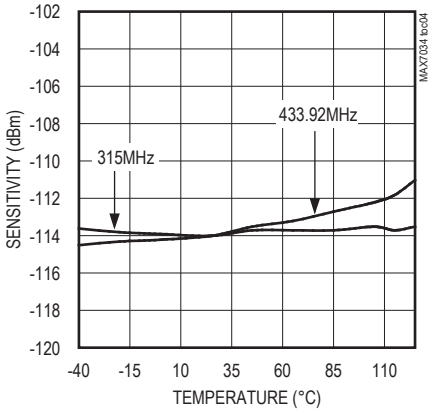
SUPPLY CURRENT vs. RF FREQUENCY



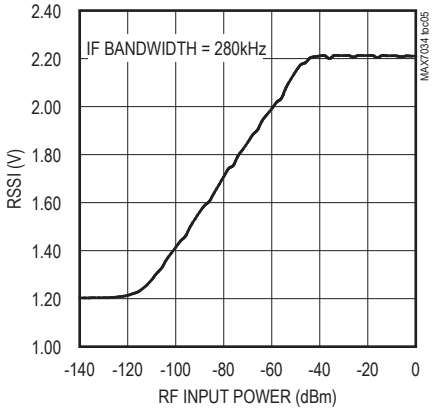
BIT-ERROR RATE vs. PEAK RF INPUT POWER



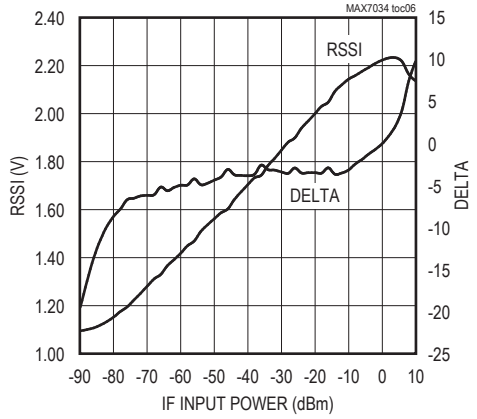
SENSITIVITY vs. TEMPERATURE



RSSI vs. RF INPUT POWER



RSSI AND DELTA vs. IF INPUT POWER



LNA/MIXER VOLTAGE GAIN vs. IF FREQUENCY

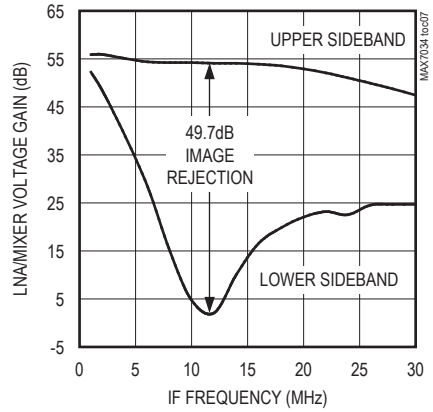


IMAGE REJECTION vs. RF FREQUENCY

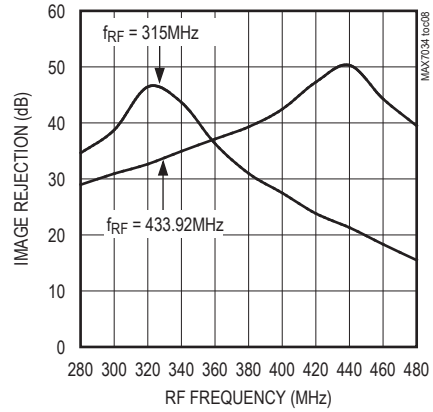
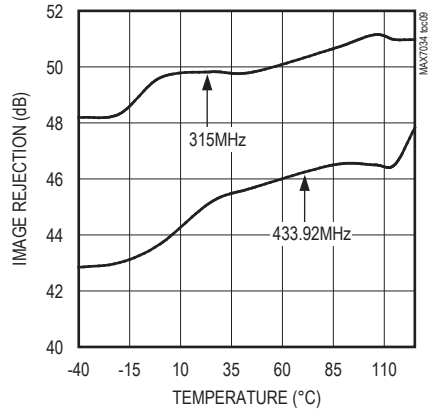


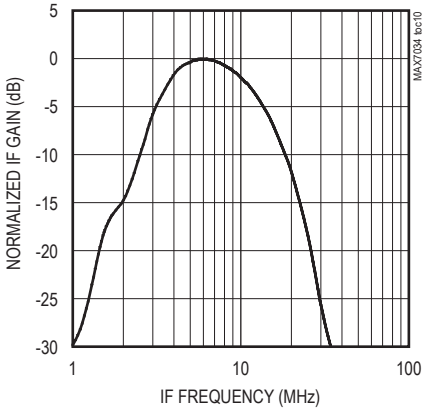
IMAGE REJECTION vs. TEMPERATURE



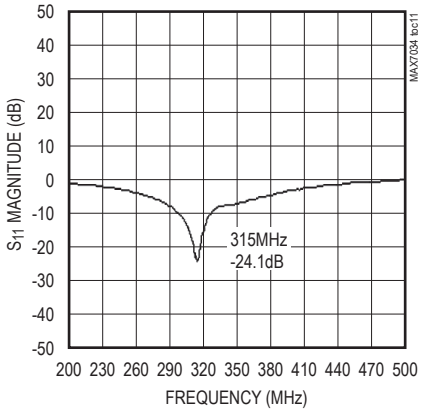
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{DD5} = +5.0V, f_{RF} = 433.92MHz, T_A = +25°C, unless otherwise noted.)

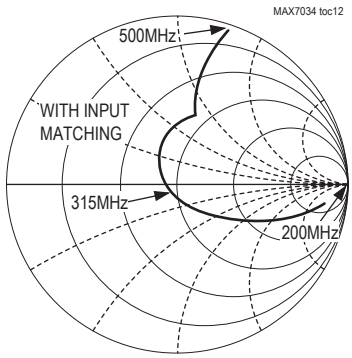
NORMALIZED IF GAIN vs. IF FREQUENCY



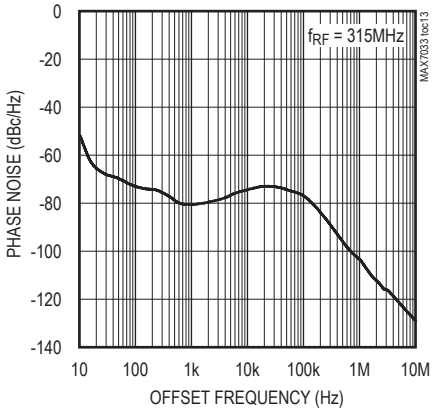
S_{11} MAGNITUDE PLOT OF RFIN vs. FREQUENCY



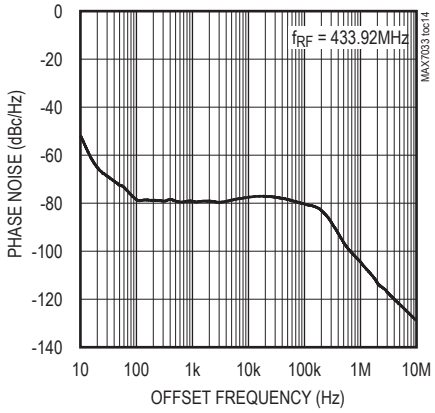
S_{11} SMITH CHART PLOT OF RFIN



PHASE NOISE vs. OFFSET FREQUENCY



PHASE NOISE vs. OFFSET FREQUENCY



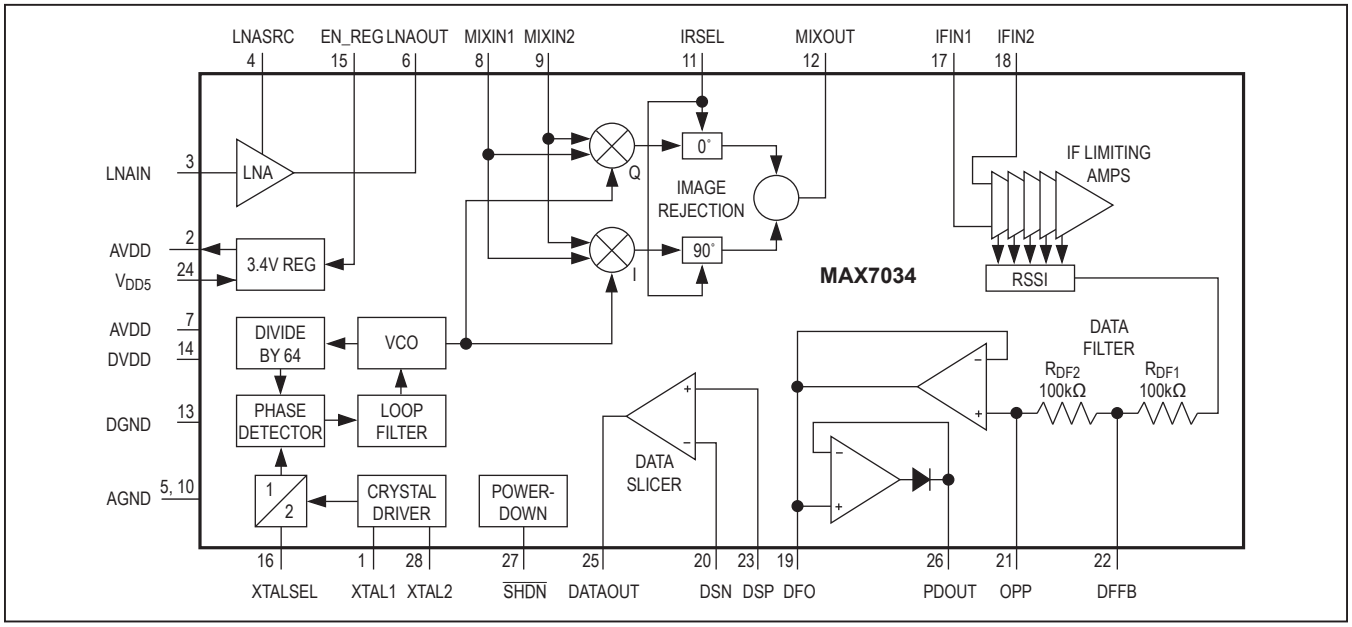
Pin Description

PIN	NAME	FUNCTION
1	XTAL1	Crystal Input 1
2, 7	AVDD	Positive Analog Supply Voltage. For +5V operation, pin 2 is the output of an on-chip +3.4V low-dropout regulator, and should be bypassed to AGND with a 0.1µF capacitor as close as possible to the pin. Pin 7 must be externally connected to the supply from pin 2, and bypassed to AGND with a 0.01µF capacitor as close as possible to the pin (see the *Voltage Regulator* section and the *Typical Application Circuit*).
3	LNAIN	Low-Noise Amplifier Input. See the *Low-Noise Amplifier* section.

Pin Description (continued)

PIN	NAME	FUNCTION
4	LNASRC	Low-Noise Amplifier Source for external Inductive Degeneration. Connect inductor to ground to set LNA input impedance. See the *Low-Noise Amplifier* section.
5, 10	AGND	Analog Ground
6	LNAOUT	Low-Noise Amplifier Output. Connect to mixer input through an LC tank filter. See the *Low-Noise Amplifier* section.
8	MIXIN1	1st Differential Mixer Input. Connect to LC tank filter from LNAOUT through a 100pF capacitor. See the *Typical Application Circuit*.
9	MIXIN2	2nd Differential Mixer Input. Connect to V_{DD3} side of the LC tank filter through a 100pF capacitor. See the *Typical Application Circuit*.
11	IRSEL	Image-Rejection Select. Set V_{IRSEL} = 0V to center image rejection at 315MHz. Leave IRSEL unconnected to center image rejection at 375MHz. Set V_{IRSEL} = DVDD to center image rejection at 434MHz. See the *Mixer* section.
12	MIXOUT	330Ω Mixer Output. Connect to the input of the 10.7MHz bandpass filter.
13	DGND	Digital Ground
14	DVDD	Positive Digital Supply Voltage. Connect to both of the AVDD pins. Bypass to DGND with a 0.01µF capacitor as close as possible to the pin (see the *Typical Application Circuit*).
15	EN_REG	Regulator Enable. Connect to V_{DD5} to enable internal regulator. Pull this pin low to allow device operation between +3.0V and +3.6V. See the *Voltage Regulator* section.
16	XTALSEL	Crystal Divider Ratio Select. Drive XTALSEL low to select f_{LO}/f_{XTAL} ratio of 64, or drive XTALSEL high to select f_{LO}/f_{XTAL} ratio of 32.
17	IFIN1	1st Differential Intermediate-Frequency Limiter Amplifier Input. Connect to the output of a 10.7MHz bandpass filter.
18	IFIN2	2nd Differential Intermediate-Frequency Limiter Amplifier Input. Bypass to AGND with a 1500pF capacitor as close as possible to the pin.
19	DFO	Data Filter Output
20	DSN	Negative Data Slicer Input
21	OPP	Noninverting Op-Amp Input for the Sallen-Key Data Filter
22	DFFB	Data Filter Feedback Node. Input for the feedback of the Sallen-Key data filter.
23	DSP	Positive Data Slicer Input
24	V_{DD5}	+5V Supply Voltage. Bypass to AGND with a 0.01µF capacitor as close as possible to the pin. For +5V operation, V_{DD5} is the input to an on-chip voltage regulator whose +3.4V output appears at AVDD pin 2. (see the *Voltage Regulator* section and the *Typical Application Circuit*).
25	DATAOUT	Digital Baseband Data Output
26	PDOUT	Peak-Detector Output
27	SHDN	Power-Down Select Input. Drive high to power up the IC. Internally pulled down to AGND with a 100kΩ resistor.
28	XTAL2	Crystal Input 2. Can also be driven with an external reference oscillator. See the *Crystal Oscillator* section.

Functional Diagram



Detailed Description

The MAX7034 CMOS superheterodyne receiver and a few external components provide the complete receive chain from the antenna to the digital output data. Depending on signal power and component selection, data rates can be as high as 33kbps Manchester (66kbps NRZ).

The MAX7034 is designed to receive binary ASK data modulated in the 300MHz to 450MHz frequency range. ASK modulation uses a difference in amplitude of the carrier to represent logic 0 and logic 1 data.

Voltage Regulator

For operation with a single +4.5V to +5.5V supply voltage, connect V_{DD5} and the EN_REG pin to the supply voltage. An on-chip voltage regulator drives one of the AVDD pins (pin 2) to approximately +3.4V. For proper operation, DVDD and both AVDD pins must be connected together. For operation with a single +3.0V to +3.6V supply voltage, connect both the AVDD pins, DVDD, and V_{DD5} to the supply voltage and connect the EN_REG pin to ground (which disables the internal voltage regulator). If the MAX7034 is powered from +3.0V to +3.6V, the performance is limited to the -40°C to +105°C range.

In either supply voltage mode, bypass V_{DD5}, DVDD, and the pin 7 AVDD pin to AGND with 0.01µF capacitors, and the pin 2 AVDD to AGND with a 0.1µF capacitor, all placed as close as possible to the pins.

Low-Noise Amplifier

The LNA is an nMOS cascode amplifier with off-chip inductive degeneration. The gain and noise figures are dependent on both the antenna matching network at the LNA input and the LC tank network between the LNA output and the mixer inputs.

The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedance at LNAIN, allowing for a more flexible input impedance match, such as a typical printed-circuit board (PCB) trace antenna. A nominal value for this inductor with a 50Ω input impedance is 15nH, but is affected by the PCB trace.

The LC tank filter connected to LNAOUT comprises L1 and C9 (see the *Typical Application Circuit*). Select L1 and C9 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f_{RF} = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where:

$L_{TOTAL} = L1 + L_{PARASITICS}$.

$C_{TOTAL} = C9 + C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PCB traces, package pins, mixer input impedance, etc. These parasitics at high frequencies cannot be ignored, and can have a dramatic effect on the tank filter center frequency. The total parasitic capacitance is generally between 4pF and 6pF.

Mixer

A unique feature of the MAX7034 is the integrated image rejection of the mixer. This device eliminates the need for a costly front-end SAW filter for most applications. Advantages of not using a SAW filter are increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double balanced mixers that perform an IQ downconversion of the RF input to the 10.7MHz IF from a low-side injected LO (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image-rejection circuit then combines these signals to achieve 44dB of image rejection. Low-side injection is required due to the on-chip image-rejection architecture. The IF output is driven by a source follower biased to create a driving-point impedance of 330Ω; this provides a good match to the off-chip 330Ω ceramic IF filter.

The IRSEL pin is a logic input that selects one of the three possible image-rejection frequencies. When V_{IRSEL} = 0V, the image rejection is tuned to 315MHz. $V_{IRSEL} = V_{DVDD}/2$ tunes the image rejection to 375MHz, and $V_{IRSEL} = V_{DVDD}$ tunes the image rejection to 434MHz. The IRSEL pin is internally set to $V_{DVDD}/2$ (image rejection at 375MHz) when it is left unconnected, thereby eliminating the need for an external $V_{DVDD}/2$ voltage.

Phase-Locked Loop

The PLL block contains a phase detector, charge pump, integrated loop filter, VCO, asynchronous 64x clock divider, and crystal oscillator driver. Besides the crystal, this PLL does not require any external components. The VCO generates a low-side LO. The relationship between the RF, IF, and crystal frequencies is given by:

$$f_{XTAL} = \frac{f_{RF} - f_{IF}}{32 \times M}$$

where:

M = 1 ($V_{XTALSEL} = V_{DVDD}$) or 2 ($V_{XTALSEL}$ = 0V)

To allow the smallest possible IF bandwidth (for best sensitivity), minimize the tolerance of the reference crystal.

Intermediate Frequency and RSSI

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. The six internal AC-coupled limiting amplifiers produce an overall gain of approximately 65dB, with a bandpass-filter-type response centered near the 10.7MHz IF frequency with a 3dB bandwidth of approximately 10MHz. The RSSI circuit demodulates the IF by producing a DC output proportional to the log of the IF signal level, with a slope of approximately 14.2mV/dB.

Applications Information

Crystal Oscillator

The crystal oscillator in the MAX7034 is designed to present a capacitance of approximately 3pF between the XTAL1 and XTAL2. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its intended operating frequency, introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher. For example, a 4.7547MHz crystal designed to operate with a 10pF load capacitance oscillates at 4.7563MHz with the MAX7034, causing the receiver to be tuned to 315.1MHz rather than 315.0MHz, an error of about 100kHz, or 320ppm. **It is very important to use a crystal with a load capacitance that is equal to the capacitance of the MAX7034 crystal oscillator plus PCB parasitics.**

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance. Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE} + C_{LOAD}} - \frac{1}{C_{CASE} + C_{SPEC}}\right) \times 10^6$$

where:

f_P is the amount the crystal frequency pulled in ppm.

C_M is the motional capacitance of the crystal.

C_{CASE} is the case capacitance.

C_{SPEC} is the specified load capacitance.

C_{LOAD} is the actual load capacitance.

When the crystal is loaded as specified (i.e., $C_{LOAD} = C_{SPEC}$), the frequency pulling equals zero.

It is possible to use an external reference oscillator in place of a crystal to drive the VCO. AC-couple the external oscillator to XTAL2 with a 1000pF capacitor. Drive XTAL2 with a signal level of approximately $500mV_{P-P}$. AC-couple XTAL1 to ground with a 1000pF capacitor.

Data Filter

The data filter is implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency should be set to approximately 1.5 times the fastest expected data rate from the transmitter. Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 1 can create a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of C7 and C6, use the following equations, along with the coefficients in Table 1:

$$C7 = \frac{b}{a(100k)(\pi)(f_C)}$$

$$C6 = \frac{a}{4(100k)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency.

For example, to choose a Butterworth filter response with a corner frequency of 5kHz:

$$C7 = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C6 = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Choosing standard capacitor values changes C7 to 470pF and C6 to 220pF, as shown in the *Typical Application Circuit*.

Data Slicer

The data slicer takes the analog output of the data filter and converts it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. One input is supplied by the data filter output. Both comparator inputs are accessible off-chip to allow for different methods of generating the slicing threshold, which is applied to the second comparator input.

The suggested data slicer configuration uses a resistor (R1) connected between DSN and DSP with a capacitor (C8) from DSN to DGND (Figure 2). This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The values of R1 and C8 affect how fast the threshold tracks to the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower than the lowest expected data rate.

Note that a long string of zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester coding, which has an equal number of zeros and ones, is used.

To prevent continuous toggling of DATAOUT in the absence of an RF signal due to noise, add hysteresis to the data slicer as shown in Figure 3.

Table 1. Coefficents to Calculate C7 and C6

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618

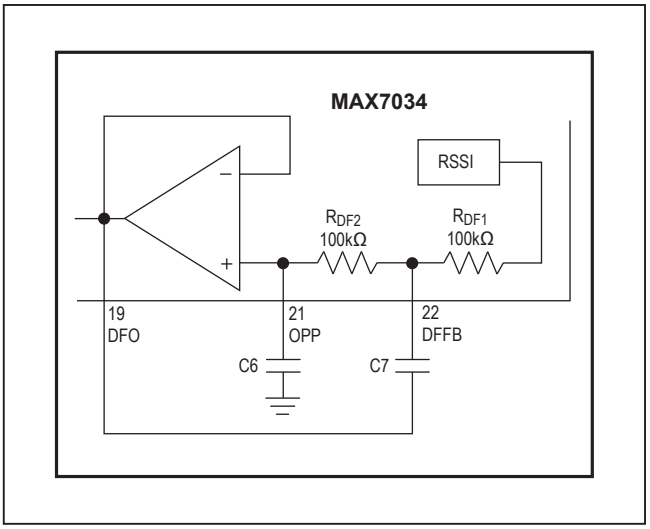


Figure 1. Sallen-Key Lowpass Data Filter

Peak Detector

The peak-detector output (PDOUT), in conjunction with an external RC filter, creates a DC output voltage equal to the peak value of the data signal. The resistor provides a path for the capacitor to discharge, allowing the peak detector to dynamically follow peak changes of the data-filter output voltage. For faster data slicer response, use the circuit shown in Figure 4. For more details on hysteresis and peak-detector applications, refer to Maxim Application Note 3671, *Data Slicing Techniques for UHF ASK Receivers*.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ/10 or longer act as antennas.

Keeping the traces short also reduces parasitic inductance. Generally, 1 inch of a PCB trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5 inch trace connecting a 100nH inductor adds an extra 10nH of inductance or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all power-supply pins.

Control Interface Considerations

When operating the MAX7034 with a +4.5V to +5.5V supply voltage, the $\overline{SHDN}$ pin can be driven by a microcontroller with either +3.0V or +5V interface logic levels. When operating the MAX7034 with a +3.0V to +3.6V supply, only +3.0V logic from the microcontroller is allowed.

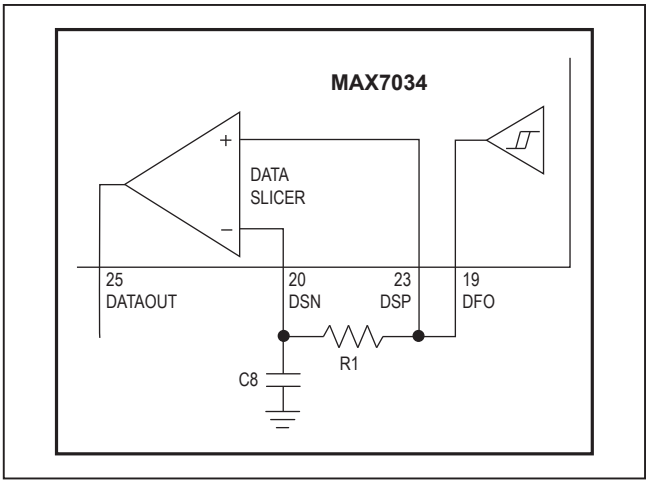


Figure 2. Generating Data Slicer Threshold

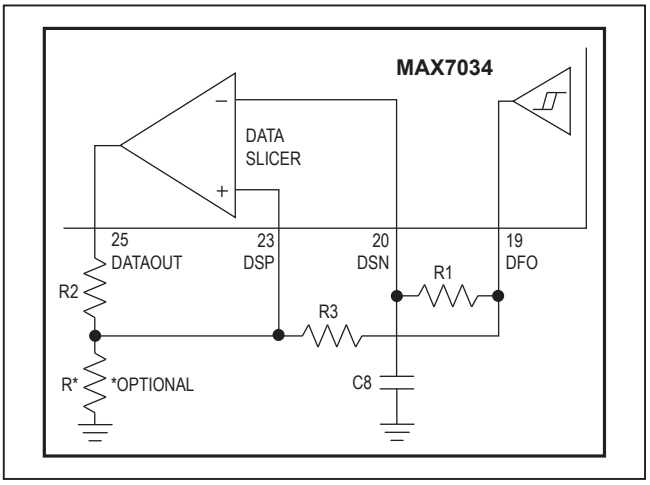


Figure 3. Generating Data Slicer Hysteresis

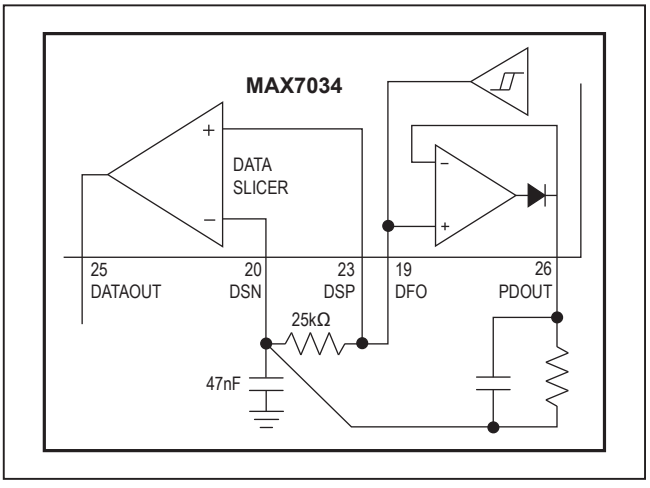
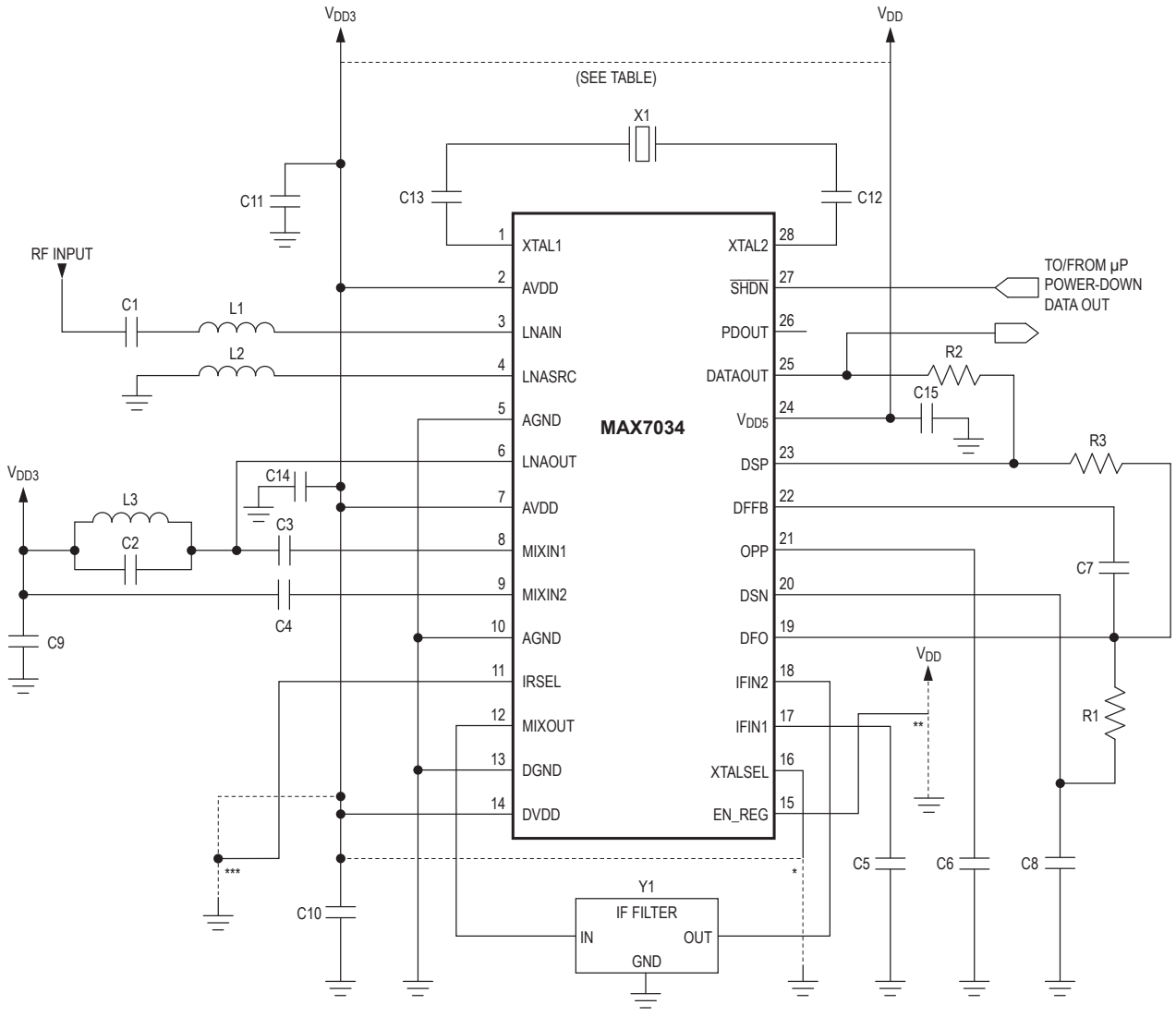


Figure 4. Using PDOUT for Faster Startup

Typical Application Circuit

IF V_{DD} IS	THEN V_{DD3} IS	AND EN_REG IS
3.0V TO 3.6V	CONNECTED TO V_{DD}	GROUNDED
4.5V TO 5.5V	CREATED BY LDO, AVAILABLE AT AVDD (PIN 2)	CONNECTED TO V_{DD}



COMPONENT VALUES IN TABLE 2

***SEE THE *MIXER* SECTION.

*SEE THE *PHASE-LOCKED LOOP* SECTION.

**SEE THE *VOLTAGE REGULATOR* SECTION.

Table 2. Component Values for Typical Application Circuit

COMPONENT	VALUE FOR f_{RF} = 433MHz	VALUE FOR f_{RF} = 315MHz	DESCRIPTION
C1	100pF	100pF	5%
C2	Open	Open	±0.1pF
C3	100pF	100pF	5%
C4	100pF	100pF	5%
C5	1500pF	1500pF	10%
C6	220pF	220pF	5%
C7	470pF	470pF	5%
C8	0.47µF	0.47µF	20%
C9	220pF	220pF	10%
C10	0.01µF	0.01µF	20%
C11	0.1µF	0.1µF	20%
C12	100pF	100pF	5%
C13	100pF	100pF	5%
C14	0.01µF	0.01µF	20%
C15	0.01µF	0.01µF	20%
L1	56nH	120nH	5% or better**
L2	15nH	15nH	5% or better**
L3	27nH	51nH	5% or better**
R1	5.1kΩ	5.1kΩ	5%
R2	Open	Open	—
R3	0Ω	0Ω	—
X1 (÷64)	6.6128MHz*	4.7547MHz*	NDK or Suntsu
X1 (÷32)	13.2256MHz*	9.5094MHz*	NDK or Suntsu
Y1	10.7MHz ceramic filter	10.7MHz ceramic filter	Murata

**Crystal frequencies shown are for ÷64 ($V_{XTALSEL}$ = 0V) and ÷32 ($V_{XTALSEL}$ = V_{DD}).*

***Wire wound recommended.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TSSOP	U28+1	21-0066	90-0171

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7034AUI/V+T	-40°C to +125°C	28 TSSOP

/V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/08	Initial release	—
1	3/09	Added /V designation to part number.	1
2	5/11	Updated *Pin Description*, *Functional Diagram*, *Voltage Regulator* section, *Typical Application Circuit*, and *Package Information*; added *Control Interface Considerations* section	7, 8, 11, 12, 13
3	6/12	Updated capacitors in *Data Filter* section; updated Table 1 to reflect correct capacitor; updated Figures 1, 2, 3; updated Table 2 component values and wire wound recommendation	10, 11, 13
4	11/16	Updated Electrical Characteristics table	1, 3, 4

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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