ARM® Cortex®-M0
32-bit Microcontroller

NuMicro® Family
NUC029 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® NUC029 series 32-bit microcontroller is embedded with ARM® Cortex®-M0 core for industrial control and applications which need rich communication interfaces or require high performance, high integration, and low cost. The Cortex®-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller. The NuMicro® NUC029 series includes four part numbers: NUC029LAN, NUC029NAN, NUC029ZAN, NUC029TAN and NUC029FAE.

The NUC029LAN/NUC029NAN/NUC029ZAN/NUC029TAN can run up to 50 MHz and operate at 2.5V ~ 5.5V, -40℃ ~ 85℃, and the NUC029FAE can run up to 24 MHz and operate at 2.5V ~ 5.5V, -40℃ ~ 105℃. Therefore, the NUC029 series can afford to support a variety of industrial control and applications which need high CPU performance.

The NUC029LAN/NUC029NAN/NUC029ZAN/NUC029TAN offers 64K/64K/32K bytes flash, 4 Kbytes Data Flash, 4 Kbytes flash for the ISP, and 4 Kbytes SRAM. The NUC029FAE offers 16 Kbytes flash, size configurable Data Flash (shared with program flash), 2 Kbytes flash for the ISP, and 2K-bytes SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I^2C, PWM, ADC, WDT (Watchdog Timer), WWDT (Window Watchdog Timer), Analog Comparator and Brown-out Detector, have been incorporated into the NUC029 series in order to reduce component count, board space and system cost. These useful functions make the NUC029 series powerful for a wide range of applications.

Additionally, the NuMicro® NUC029 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, and IAP (In-Application Programming), which allow the user to update the program memory without removing the chip from the actual end product.

Item	NUC029LAN/NUC029NAN/ NUC029ZAN/NUC029TAN	NUC029FAE
Core	Up to 50 MHz	Up to 24 MHz
Operating Temp.	-40℃ ~ +85℃	-40℃ ~ +105℃
Hardware Divider	√	-
Clock Control	Supports PLL as clock source	-
	-	Supports external 32.768 kHz crystal oscillator as clock source
Window WDT	√	-
PWM	PWM Generator and Capture Timer	Enhanced PWM Generator
ADC	12-bit SAR ADC with 760 kSPS (Supports Single, Burst, Single-Cycle, and Continuous Scan mode)	10-bit SAR ADC with 300 kSPS (Only supports Single mode)
EBI	√	-
Built-in Temp.Sensor	√	-

Table 1-1 NuMicro® NUC029 Series Difference List

2 FEATURES

- ARM® Cortex®-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
  - Provides hardware divider and supports signed 32-bit dividend, 16-bit divisor operation(NUC029xAN only)
- Operating voltage ranges from 2.5 V to 5.5 V
- Memory
  - 16/32/64 KB Flash for program memory (APROM)
  - Up to 4 KB Flash for loader (LDROM)
  - Up to 4 KB SRAM for internal scratch-pad RAM (SRAM)
  - 4 KB Flash for data memory (Data Flash) (NUC029xAN only)
  - Configurable Data Flash (NUC029FAE only)
- Clock Control
  - Programmable system clock source
  - 22.1184 MHz internal oscillator
    - Dynamically calibrating the HIRC OSC to 22.1184 MHz ±3% from -40℃ to 105℃ by external 32.768 kHz crystal oscillator (LXT) (NUC029FAE only)
  - 4~24 MHz external crystal input
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in Sleep mode
  - PLL allows CPU operation up to the maximum 50 MHz (NUC029xAN only)
  - 32.768 kHz external crystal input (LXT) for Power-down wake-up and system operation clock (NUC029FAE only)
- GPIO
  - Up to 40 general-purpose I/O (GPIO) pins for LQFP/QFN 48-pin package
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - Configurable I/O mode after POR
- Timer
  - Up to four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides up to four timer counting modes: one-shot, periodic, toggle and continuous counting
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Supports event counting function to count the input event from external counter pin
  - 24-bit capture value is readable through TCAP (Timer Capture Data Register)
  - Supports external capture pin for interval measurement
    - Supports external capture pin to reset 24-bit up counter
    - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
  - Supports internal capture triggered while internal ACMP output signal transition

(NUC029xAN only)
  - Supports Inter-Timer trigger mode (NUC029xAN only)
  - Supports internal signal (CPO0, CPO1) for interval measurement (NUC029FAE only)
- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Power-down or Sleep mode
  - Interrupt or reset selectable on watchdog time-out
  - Time-out reset delay period can be selected to 3/18/130/1026 * WDT_CLK (NUC029xAN only)
- WWDT (Window Watchdog Timer) (NUC029xAN only)
  - 6-bit down counter with 11-bit pre-scale for wide range window selected
- PWM Generator and Capture Timer (NUC029xAN only)
  - Up to four built-in 16-bit PWM generators, providing eight PWM outputs or four complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers with rising/falling capture inputs
  - Supports capture interrupt
  - Internal 10 kHz to PWM clock source
  - Polar inverse function
  - Center-aligned type function
  - Timer duty interrupt enable function
  - Two kinds of PWM interrupt period type selection
  - Two kinds of PWM interrupt duty type selection
  - Period/duty trigger ADC function
  - PWM Timer synchronous start function
- Enhanced PWM Generator (NUC029FAE only)
  - Independent 16-bit PWM duty control units with maximum three outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART
  - Up to two sets of UART devices
  - Programmable baud-rate generator
  - Buffered receiver and transmitter, each with 16 bytes FIFO
  - Optional flow control function (CTS and RTS)
  - Supports IrDA(SIR) function
  - Supports RS-485 function
  - Supports LIN function (NUC029xAN only)
- SPI
  - Up to two sets of SPI devices
  - Supports Master/Slave mode

- Full-duplex synchronous serial data transfer
- Provides 3 wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer
- PLL clock source (NUC029xAN only)

- I^2C
  - Up to two sets of I^2C modules
  - Supports Master/Slave mode
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Supports Power-down wake-up function
  - Supports FIFO function (NUC029FAE only)
- ADC
  - 12-bit SAR ADC with 760 kSPS for NUC029xAN, and 10-bit SAR ADC with 300 kSPS for NUC029FAE
  - Up to eight single-end analog input channels
    - Or four differential analog input channels (NUC029xAN only)
  - Four operation modes (NUC029FAE only support Single mode)
    - Single mode: A/D conversion is performed one time on a specified channel
    - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO
    - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
    - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion
  - An A/D conversion can be started by:
    - Software Write 1 to ADST bit
    - External pin (STADC)
    - PWM trigger with optional start delay period
  - Each conversion result is held in data register with valid and overrun indicators
  - Each channel has individual data register (NUC029xAN only)
  - Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
  - Internal temperature sensor output (NUC029xAN only)
- Analog Comparator
  - Up to four sets of Comparator analog modules
  - External input or internal band-gap voltage selectable at negative node
  - Interrupt when compared results change
  - Power-down wake-up

- EBI (External Bus Interface) for external memory-mapped device access (NUC029LAN/ NUC029NAN only)
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-bit or 16-bit data width
  - Supports byte-write in 16-bit data width
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- One built-in temperature sensor with 1℃ resolution (NUC029xAN only)
- BOD (Brown-out Detector)
  - With 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID (UID)
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature:
  - NUC029LAN/NUC029NAN/NUC029ZAN/NUC029TAN: -40℃~85℃
  - NUC029FAE:-40℃~105℃
- Reliability: EFT > ± 4 KV, ESD HBM pass 4 KV
- Packages:
  - All Green package (RoHS)
  - 48-pin LQFP, 48-pin QFN, 33-pin QFN, 20-pin TSSOP

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
EBI	External Bus Interface
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NUC029 Series Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			PWM (16-bit)	ADC (12-bit)	ADC (10-bit)	Comparator	WDT	WWDT	EBI	PLL	32.768 kHz Crystal Oscillator	ISP/ICP/IAP	Package	Operating Temperature Range(℃)
							UART	SPI	I^2C												
NUC029LAN	64	4	4	4	40	4	2	2	2	8	8	-	4	√	√	√	√	-	√	LQFP48	-40 to +85
NUC029NAN	64	4	4	4	40	4	2	2	2	8	8	-	4	√	√	√	√	-	√	QFN48	-40 to +85
NUC029ZAN	64	4	4	4	24	4	2	1	2	5	5	-	3*	√	√	-	√	-	√	QFN33 (5x5)	-40 to +85
NUC029TAN	32	4	4	4	24	4	2	1	2	5	5	-	3*	√	√	-	√	-	√	QFN33 (4x4)	-40 to +85
NUC029FAE	16	2	Config.	2	17	2	1	1	1	3	-	4	2**	√	-	-	-	√	√	TSSOP20	-40 to +105

Table 4-1 NuMicro® NUC029 Series Selection Guide

Note:

*: ACMP3 only has positive and negative input.

**: ACMP0 only has positive and negative input, and ACMP1 only has positive input.

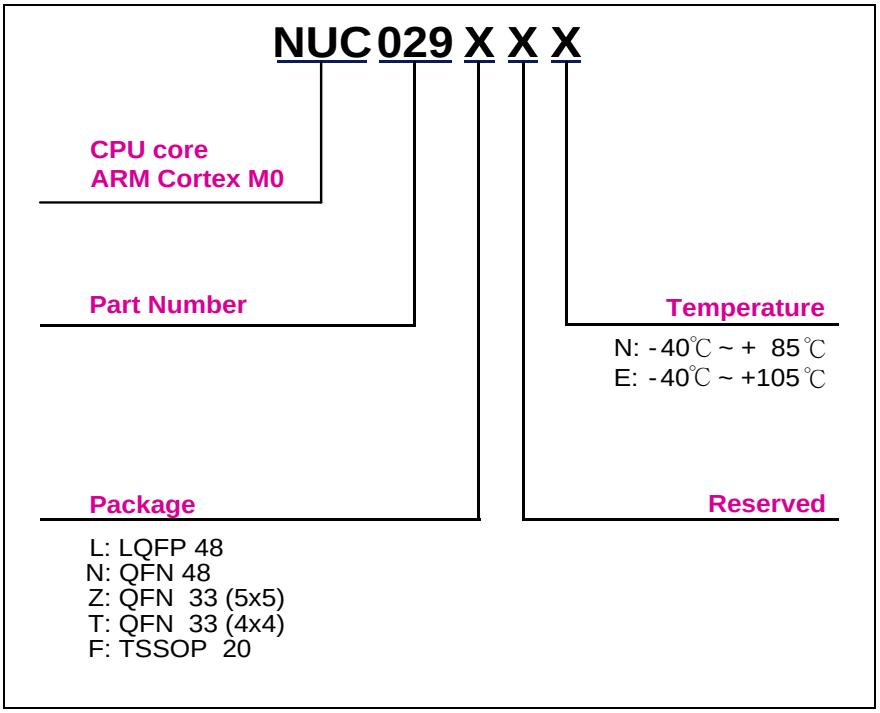


Figure 4-1 NuMicro® NUC029 Series Selection Code

4.2 Pin Configuration

4.2.1 NuMicro® NUC029 Pin Diagram

4.2.1.1 NuMicro® NUC029LAN LQFP 48 pin

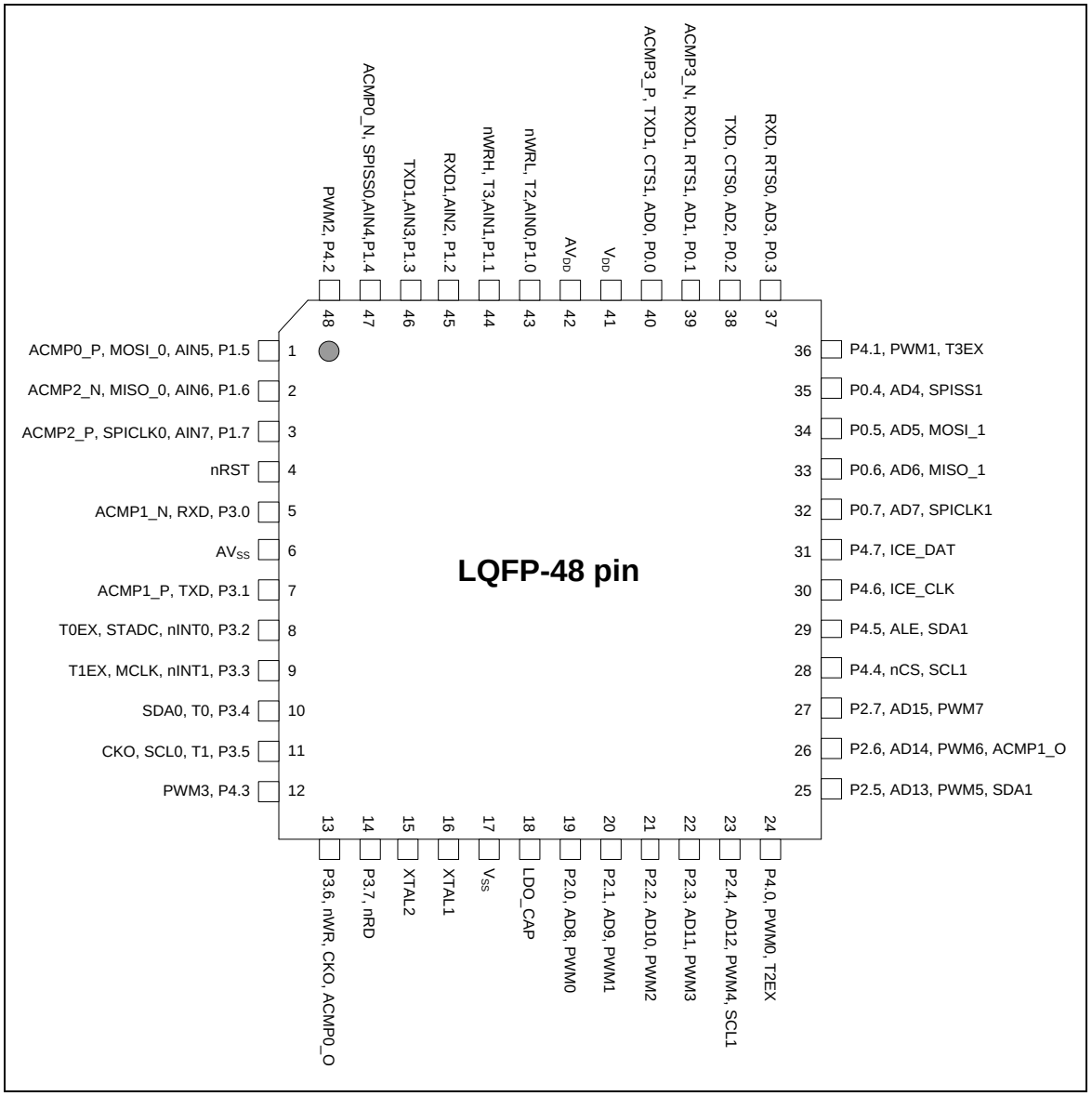


Figure 4-2 NuMicro® NUC029LAN LQFP 48-pin Diagram

4.2.1.2 NuMicro® NUC029NAN QFN 48 pin

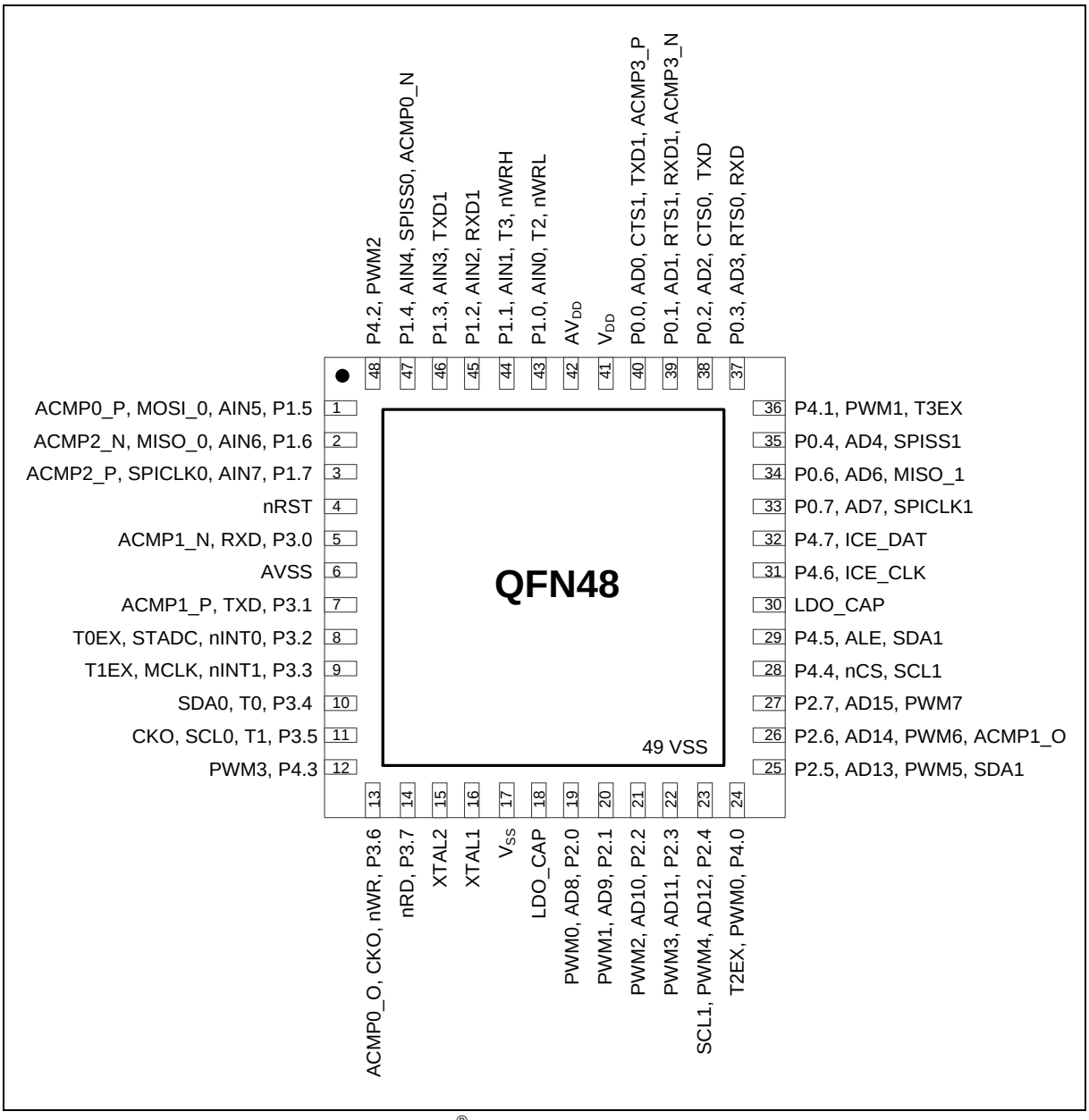


Figure 4-3 NuMicro® NUC029NAN QFN 48-pin Diagram

4.2.1.3 NuMicro® NUC029ZAN/NUC029TAN QFN 33 pin

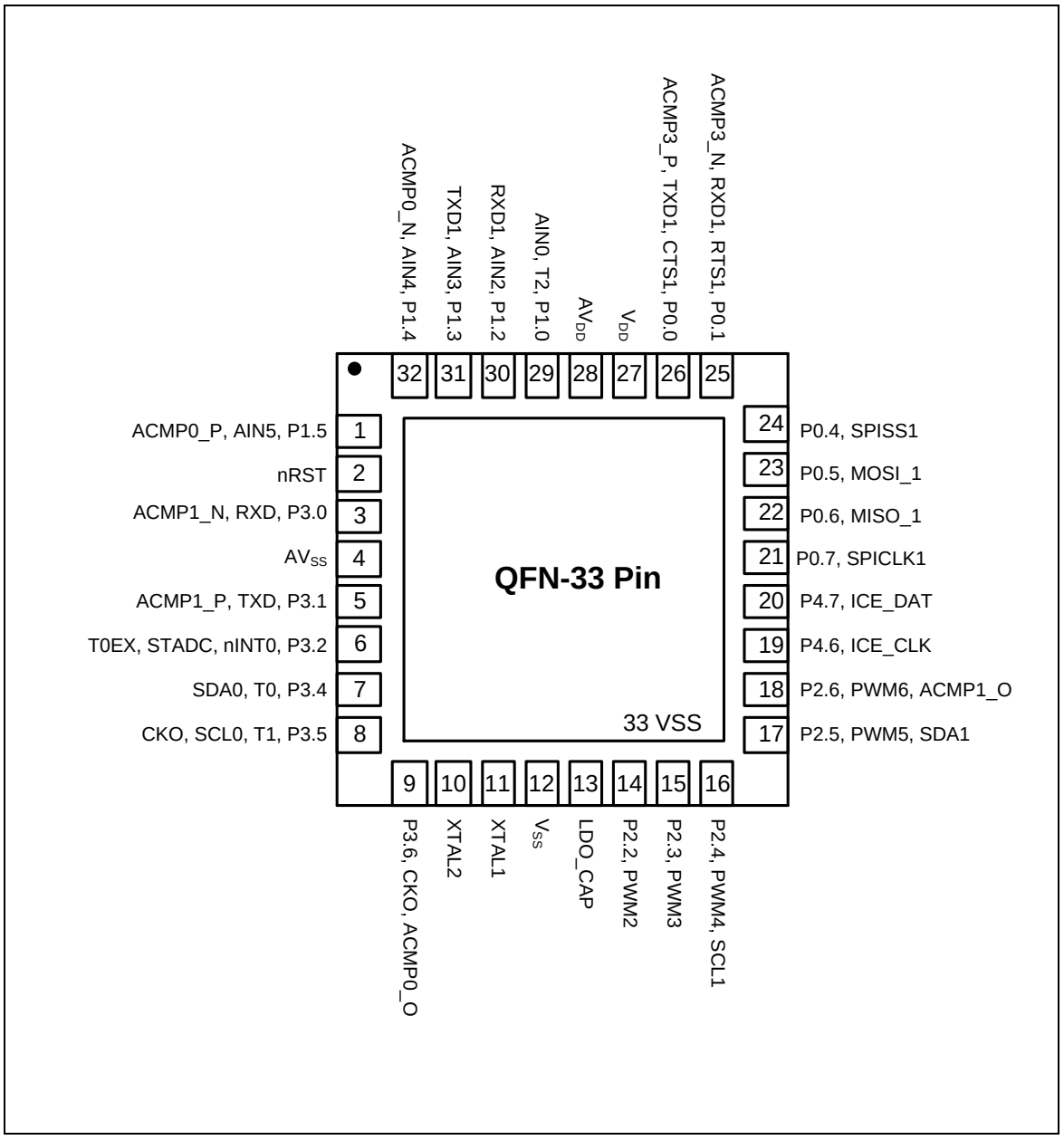


Figure 4-4 NuMicro® NUC029ZAN/NUC029TAN QFN 33-pin Diagram

4.2.1.4 NuMicro® NUC029FAE TSSOP 20 pin

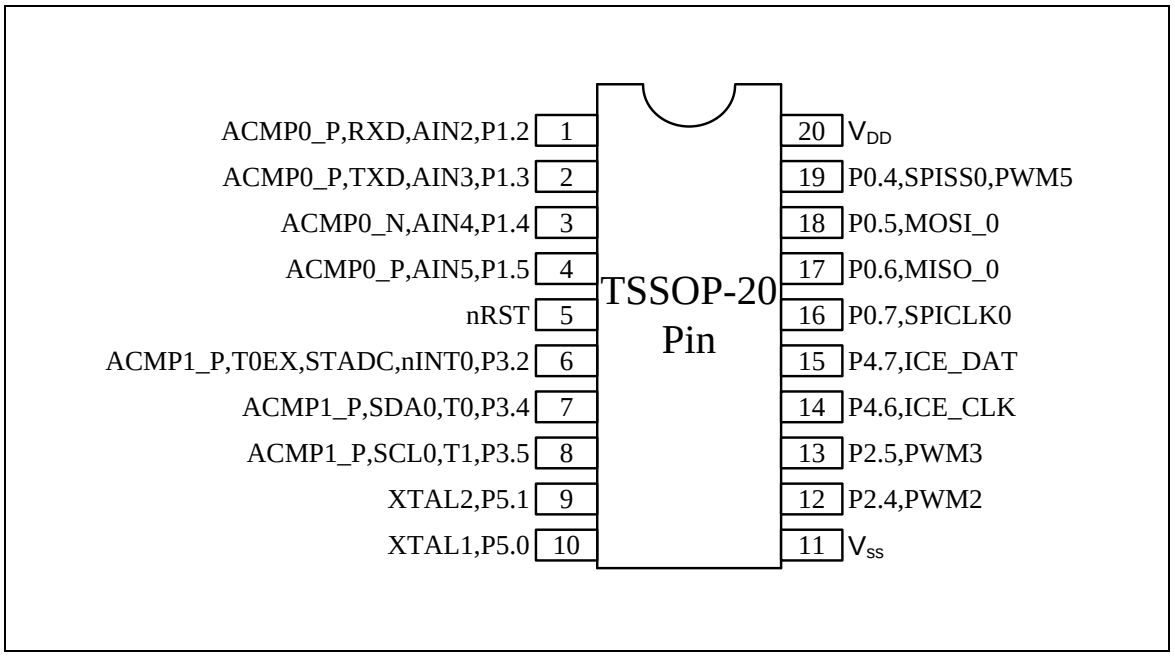


Figure 4-5 NuMicro® NUC029FAE TSSOP 20-pin Diagram

4.3 Pin Description

4.3.1 NuMicro® NUC029 Pin Description

Pin No.		Pin Name	Pin Type	Description
LQFP/QFN 48-pin	QFN 33-pin			
1	1	P1.5	I/O	General purpose digital I/O pin.
		AIN5	AI	ADC5 analog input.
		ACMP0_P	AI	Comparator0 positive input pin.
	–	MOSI_0	I/O	SPI0 MISO (Master Out, Slave In) pin.
2	–	P1.6	I/O	General purpose digital I/O pin.
		AIN6	AI	ADC6 analog input.
		MISO_0	I/O	SPI0 MISO (Master In, Slave Out) pin.
		ACMP2_N	AI	Comparator2 negative input pin.
3	–	P1.7	I/O	General purpose digital I/O pin.
		AIN7	AI	ADC7 analog input.
		SPICLK0	I/O	SPI0 serial clock pin.
		ACMP2_P	AI	Comparator2 positive input pin.
4	2	nRST	I (ST)	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
5	3	P3.0	I/O	General purpose digital I/O pin.
		RXD[2]	I	Data receiver input pin for UART0.
		ACMP1_N	AI	Comparator1 negative input pin.
6	4	AV_{SS}	AP	Ground pin for analog circuit.
7	5	P3.1	I/O	General purpose digital I/O pin.
		TXD[2]	O	Data transmitter output pin for UART0.
		ACMP1_P	AI	Comparator1 positive input pin
8	6	P3.2	I/O	General purpose digital I/O pin.
		nINT0	I	External interrupt0 input pin.
		STADC	I	ADC external trigger input.
		T0EX	I	Timer0 external capture/reset trigger input pin.
9	–	P3.3	I/O	General purpose digital I/O pin.
		nINT1	I	External interrupt1 input pin.
		MCLK	O	EBI external clock output pin.
		TIEX	I	Timer1 external capture/reset trigger input pin.
10	7	P3.4	I/O	General purpose digital I/O pin.

Pin No.		Pin Name	Pin Type	Description
LQFP/QFN 48-pin	QFN 33-pin			
		T0	I/O	Timer0 external event counter input pin
		SDA0	i/O	I2C0 data input/output pin.
11	8	P3.5	I/O	General purpose digital I/O pin.
		T1	I/O	Timer1 external event counter input pin.
		SCL0	I/O	I^2C0 clock I/O pin.
		CKO[2]	O	Frequency divider output pin.
12	–	P4.3	I/O	General purpose digital I/O pin.
		PWM3[2]	I/O	PWM3 output/Capture input.
13	9	P3.6	I/O	General purpose digital I/O pin.
		CKO[2]	O	Frequency divider output pin.
	–	ACMP0_O	O	Analog comparator0 output pin.
		nWR	O	EBI write enable output pin.
14	–	P3.7	I/O	General purpose digital I/O pin.
		nRD	O	EBI read enable output pin.
15	10	XTAL2	O	External 4~24 MHz (high speed) crystal output pin.
16	11	XTAL1	I (ST)	External 4~24 MHz (high speed) crystal input pin.
17	12	V_{SS}	P	Ground pin for digital circuit.
	33			
18	13	LDO_CAP	P	LDO output pin.
19	–	P2.0	I/O	General purpose digital I/O pin.
		AD8	I/O	EBI Address/Data bus bit8
		PWM0[2]	I/O	PWM0 output/Capture input.
20	–	P2.1	I/O	General purpose digital I/O pin.
		AD9	I/O	EBI Address/Data bus bit9
		PWM1[2]	I/O	PWM1 output/Capture input.
21	14	P2.2	I/O	General purpose digital I/O pin.
		PWM2[2]	I/O	PWM2 output/Capture input.
	–	AD10	I/O	EBI Address/Data bus bit10.
22	15	P2.3	I/O	General purpose digital I/O pin.
		PWM3[2]	I/O	PWM3 output/Capture input.
	–	AD11	I/O	EBI Address/Data bus bit11.
23	16	P2.4	I/O	General purpose digital I/O pin.

Pin No.		Pin Name	Pin Type	Description
LQFP/QFN 48-pin	QFN 33-pin			
		PWM4	I/O	PWM4 output/Capture input.
		SCL1[2]	I/O	I²C1 clock I/O pin.
	–	AD12	I/O	EBI Address/Data bus bit12.
24		P4.0	I/O	General purpose digital I/O pin.
	–	PWM0[2]	I/O	PWM0 output/Capture input.
		T2EX	I	Timer2 external capture/reset trigger input pin.
25		P2.5	I/O	General purpose digital I/O pin.
	17	PWM5	I/O	PWM5 output/Capture input.
		SDA1[2]	i/O	I2C1 data input/output pin.
	–	AD13	I/O	EBI Address/Data bus bit13.
26		P2.6	I/O	General purpose digital I/O pin.
	18	PWM6	I/O	PWM6 output/Capture input.
		ACMP1_O	O	Analog comparator1 output pin.
	–	AD14	I/O	EBI Address/Data bus bit14.
27		P2.7	I/O	General purpose digital I/O pin.
	–	AD15	I/O	EBI Address/Data bus bit15.
		PWM7	I/O	PWM7 output/Capture input.
28		P4.4	I/O	General purpose digital I/O pin.
	–	nCS	O	EBI chip select enable output pin.
		SCL1[2]	I/O	I²C1 clock I/O pin.
29		P4.5	I/O	General purpose digital I/O pin.
	–	ALE	O	EBI address latch enable output pin.
		SDA1[2]	i/O	I2C1 data input/output pin.
30	19	P4.6	I/O	General purpose digital I/O pin.
		ICE_CLK	I	Serial Wired Debugger Clock pin.
31	20	P4.7	I/O	General purpose digital I/O pin.
		ICE_DAT	I/O	Serial Wired Debugger Data pin.
32	21	P0.7	I/O	General purpose digital I/O pin.
		SPICLK1	I/O	SPI1 serial clock pin.
	–	AD7	I/O	EBI Address/Data bus bit7.
33	22	P0.6	I/O	General purpose digital I/O pin.
		MISO_1	I/O	SPI1 MISO (Master In, Slave Out) pin.

Pin No.		Pin Name	Pin Type	Description
LQFP/QFN 48-pin	QFN 33-pin			
	–	AD6	I/O	EBI Address/Data bus bit6.
34	23	P0.5	I/O	General purpose digital I/O pin.
		MOSI_1	I/O	SPI1 MISO (Master Out, Slave In) pin.
	–	AD5	I/O	EBI Address/Data bus bit5.
35	24	P0.4	I/O	General purpose digital I/O pin.
		SPISS1	I/O	SPI1 slave select pin.
	–	AD4	I/O	EBI Address/Data bus bit4.
36	–	P4.1	I/O	General purpose digital I/O pin.
		PWM1[2]	I/O	PWM1 output/Capture input.
		T3EX	I	Timer3 external capture/reset trigger input pin.
37	–	P0.3	I/O	General purpose digital I/O pin.
		AD3	I/O	EBI Address/Data bus bit3.
		RTS0	O	Request to Send output pin for UART0.
		RXD[2]	I	Data receiver input pin for UART0.
38	–	P0.2	I/O	General purpose digital I/O pin.
		AD2	I/O	EBI Address/Data bus bit2.
		CTS0	I	Clear to Send input pin for UART0.
		TXD[2]	O	Data transmitter output pin for UART0.
39	25	P0.1	I/O	General purpose digital I/O pin.
		RTS1	O	Request to Send output pin for UART1.
		RXD1[2]	I	Data receiver input pin for UART1.
		ACMP3_N	AI	Comparator3 negative input pin.
	–	AD1	I/O	EBI Address/Data bus bit1.
40	26	P0.0	I/O	General purpose digital I/O pin.
		CTS1	I	Clear to Send input pin for UART1.
		TXD1[2]	O	Data transmitter output pin for UART1.
		ACMP3_P	AI	Comparator3 positive input pin.
	–	AD0	I/O	EBI Address/Data bus bit0.
41	27	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
42	28	AV_{DD}	AP	Power supply for internal analog circuit.
43	29	P1.0	I/O	General purpose digital I/O pin.

Pin No.		Pin Name	Pin Type	Description
LQFP/QFN 48-pin	QFN 33-pin			
		AIN0	**AI**	ADC0 analog input.
		T2	**I/O**	Timer2 external event counter input pin.
	–	nWRL	**O**	EBI low byte write enable output pin.
44	–	P1.1	**I/O**	General purpose digital I/O pin.
		AIN1	**AI**	ADC1 analog input.
		T3	**I/O**	Timer3 external event counter input pin.
		nWRH	**O**	EBI high byte write enable output pin.
45	30	P1.2	**I/O**	General purpose digital I/O pin.
		AIN2	**AI**	ADC2 analog input.
		RXD1[2]	**I**	Data receiver input pin for UART1.
46	31	P1.3	**I/O**	General purpose digital I/O pin.
		AIN3	**AI**	ADC3 analog input.
		TXD1[2]	**O**	Data transmitter output pin for UART1.
47	32	P1.4	**I/O**	General purpose digital I/O pin.
		AIN4	**AI**	ADC4 analog input.
		ACMP0_N	**AI**	Comparator0 negative input pin.
	–	SPISS0	**I/O**	SPI0 slave select pin.
48	–	P4.2	**I/O**	General purpose digital I/O pin.
		PWM2[2]	**I/O**	PWM2 output/Capture input.

Note1: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power; ST = Schmitt trigger

Note2: The PWM0 ~ PWM3, RXD, TXD, RXD1, TXD1, SCL1, SDA1 and CKO can be assigned to different pins. However, a pin function can only be assigned to a pin at the same time, i.e. software cannot assign RXD to P0.3 and P3.0 at the same time.

Pin No. TSSOP 20-pin	Pin Name	Pin Type	Description
1	P1.2	**I/O**	General purpose digital I/O pin.
	AIN2	**AI**	ADC2 analog input.
	RXD	**I**	Data receiver input pin for UART0.
	ACMP0_P	**AI**	Comparator0 positive input pin.
2	P1.3	**I/O**	General purpose digital I/O pin.
	AIN3	**AI**	ADC3 analog input.
	TXD	**O**	Data transmitter output pin for UART0.
	ACMP0_P	**AI**	Comparator0 positive input pin.
3	P1.4	**I/O**	General purpose digital I/O pin.
	AIN4	**AI**	ADC4 analog input.
	ACMP0_N	**AI**	Comparator0 negative input pin.
4	P1.5	**I/O**	General purpose digital I/O pin.
	AIN5	**AI**	ADC5 analog input.
	ACMP0_P	**AI**	Comparator0 positive input pin.
	AV_{SS}	**AP**	Ground pin for analog circuit.
5	nRST	**I (ST)**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
6	P3.2	**I/O**	General purpose digital I/O pin.
	nINT0	**I**	External interrupt0 input pin.
	STADC	**I**	ADC external trigger input.
	T0EX	**I**	Timer0 external capture/reset trigger input pin.
	ACMP1_P	**AI**	Comparator1 positive input pin
7	P3.4	**I/O**	General purpose digital I/O pin.
	T0	**I/O**	Timer0 external event counter input pin
	SDA0	**i/O**	I2C0 data input/output pin.
	ACMP1_P	**AI**	Comparator1 positive input pin
8	P3.5	**I/O**	General purpose digital I/O pin.
	T1	**I/O**	Timer1 external event counter input pin.
	SCL0	**I/O**	I^2C0 clock I/O pin.
	ACMP1_P	**AI**	Comparator1 positive input pin
9	P5.1	**I/O**	General purpose digital I/O pin.
	XTAL2	**O**	External 4~24 MHz (high speed) crystal output pin.
10	P5.0	**I/O**	General purpose digital I/O pin.

Pin No. TSSOP 20-pin	Pin Name	Pin Type	Description
	XTAL1	**I (ST)**	External 4~24 MHz (high speed) crystal input pin.
11	V_{SS}	**P**	Ground pin for digital circuit.
12	P2.4	**I/O**	General purpose digital I/O pin.
	PWM2	**I/O**	PWM0 output.
13	P2.5	**I/O**	General purpose digital I/O pin.
	PWM3	**I/O**	PWM3 output.
14	P4.6	**I/O**	General purpose digital I/O pin.
	ICE_CLK	**I**	Serial Wired Debugger Clock pin.
15	P4.7	**I/O**	General purpose digital I/O pin.
	ICE_DAT	**I/O**	Serial Wired Debugger Data pin.
16	P0.7	**I/O**	General purpose digital I/O pin.
	SPICLK0	**I/O**	SPI0 serial clock pin.
17	P0.6	**I/O**	General purpose digital I/O pin.
	MISO_0	**I/O**	SPI0 MISO (Master In, Slave Out) pin.
18	P0.5	**I/O**	General purpose digital I/O pin.
	MOSI_0	**I/O**	SPI0 MISO (Master Out, Slave In) pin.
19	P0.4	**I/O**	General purpose digital I/O pin.
	SPISS0	**I/O**	SPI1 slave select pin.
	PWM5	**I/O**	PWM5 output.
20	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.

Note1: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power; ST = Schmitt trigger

5 FUNCTIONAL DESCRIPTION

5.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entere d on Reset, and can be entered as a result of an exception return. Figure 5-1 shows the functional controller of processor.

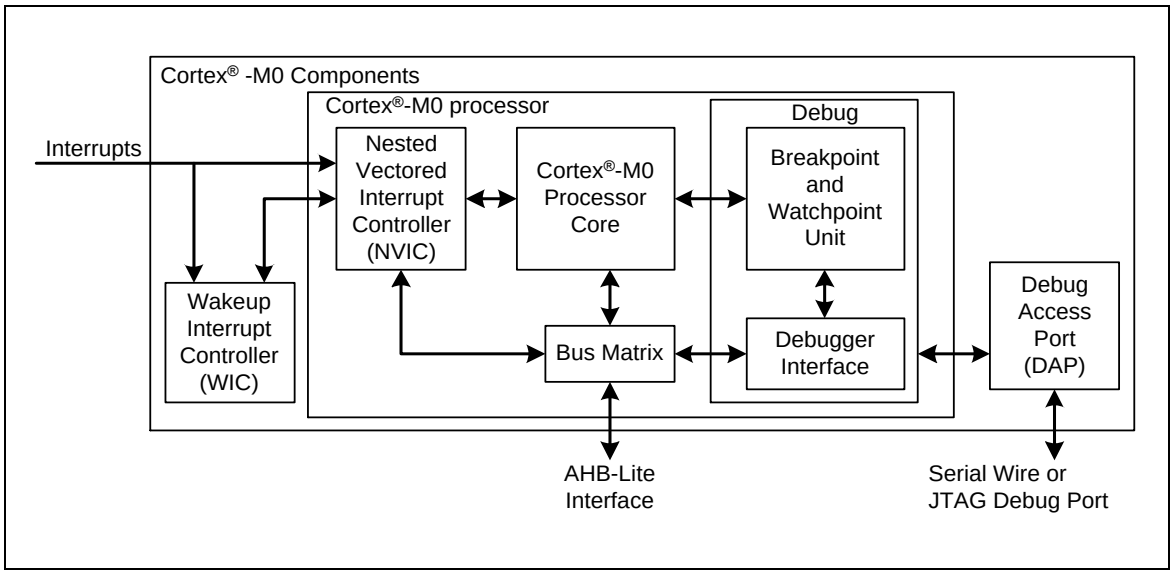


Figure 5-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

5.2 System Manager

5.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the RESET pin (nRST)
  - Watchdog Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - MCU Reset - SYSRESETREQ(AIRCR[2])
  - Cortex®-M0 Core One-shot Reset - CPU_RST(IPRSTC1[1])
  - Chip One-shot Reset - Chip_RST(IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCUReset and CPU Reset.

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8 V power for digital operation.
- Build-in a capacitor for internal voltage regulator. (NUC029FAE only)

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level with the digital power (V_{DD}). Figure 5-2 shows the NuMicro® NUC029xAN power distribution and Figure 5-3 shows the NuMicro® NUC029FAE power distribution.

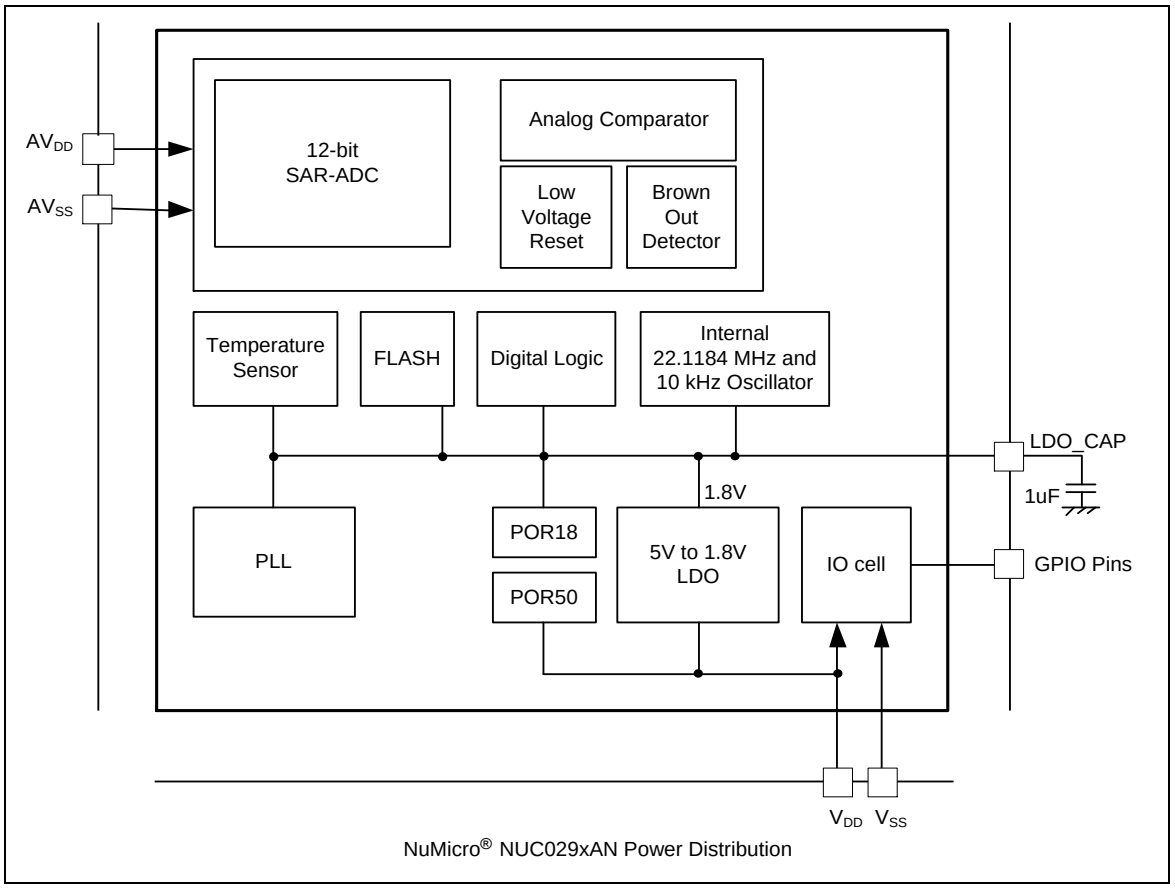


Figure 5-2 NuMicro® NUC029xAN Power Distribution Diagram

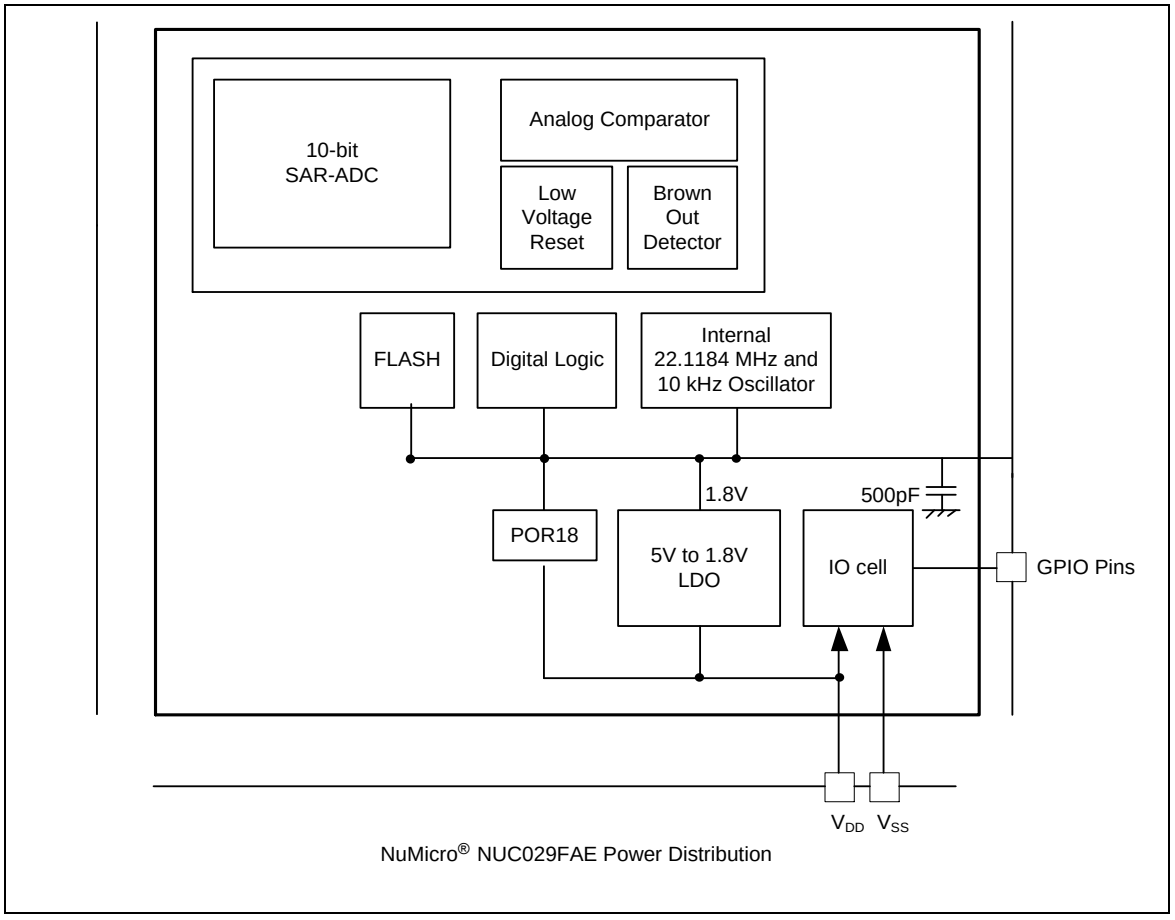


Figure 5-3 NuMicro® NUC029FAE Power Distribution Diagram

5.2.4 System Memory Map

The NuMicro® NUC029 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, addressing space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro® NUC029 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64 KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4 KB)
EBI Space (0x6000_0000 ~ 0x6001_FFFF) (NUC029LAN/NUC029NAN Only)		
0x6000_0000 – 0x6001_FFFF	EBI_BA	External Memory Space (128 KB)
AHB Controllers Space (0x5000_0000 ~ 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers

0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO (P0 ~ P4) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_CTL_BA	EBI Control Registers (NUC029LAN/NUC029NAN only)
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Register (NUC029xAN only)
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_40FF	WDT_BA	Watchdog Timer Control Registers
0x4000_4100 – 0x4000_7FFF	WWDT_BA	Window Watchdog Timer Control Registers (NUC029xAN only)
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP01_BA	Analog Comparator0/ Analog Comparator1 Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers (Nuc029xAN only)
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x401D_0000 – 0x401D_3FFF	ACMP23_BA	Analog Comparator2/ Analog Comparator3 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SYST_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Registers

Table 5-1 NuMicro® NUC029xAN Address Space Assignments for On-Chip Controllers

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	FLASH Memory Space (16 KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (2 KB)
AHB Controllers Space (0x5000_0000 ~ 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers

0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO (P0 ~ P5) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB Controllers Space (0x4000_0000 ~ 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Registers

Table 5-2 NuMicro® NUC029FAE Address Space Assignments for On-Chip Controllers

5.2.5 Whole System Memory Mapping

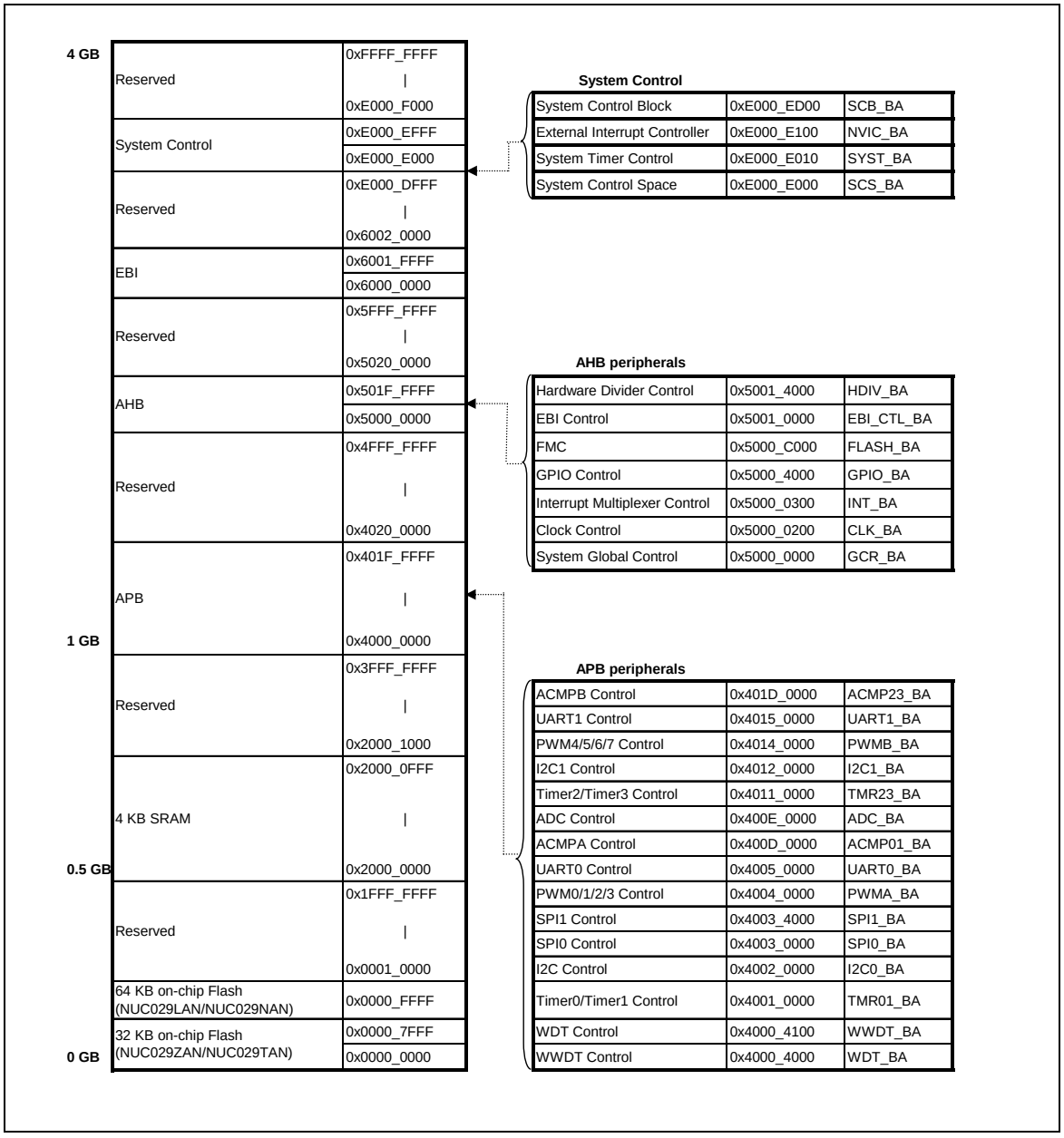


Figure 5-4 NuMicro® NUC029xAN Whole System Memory Mapping

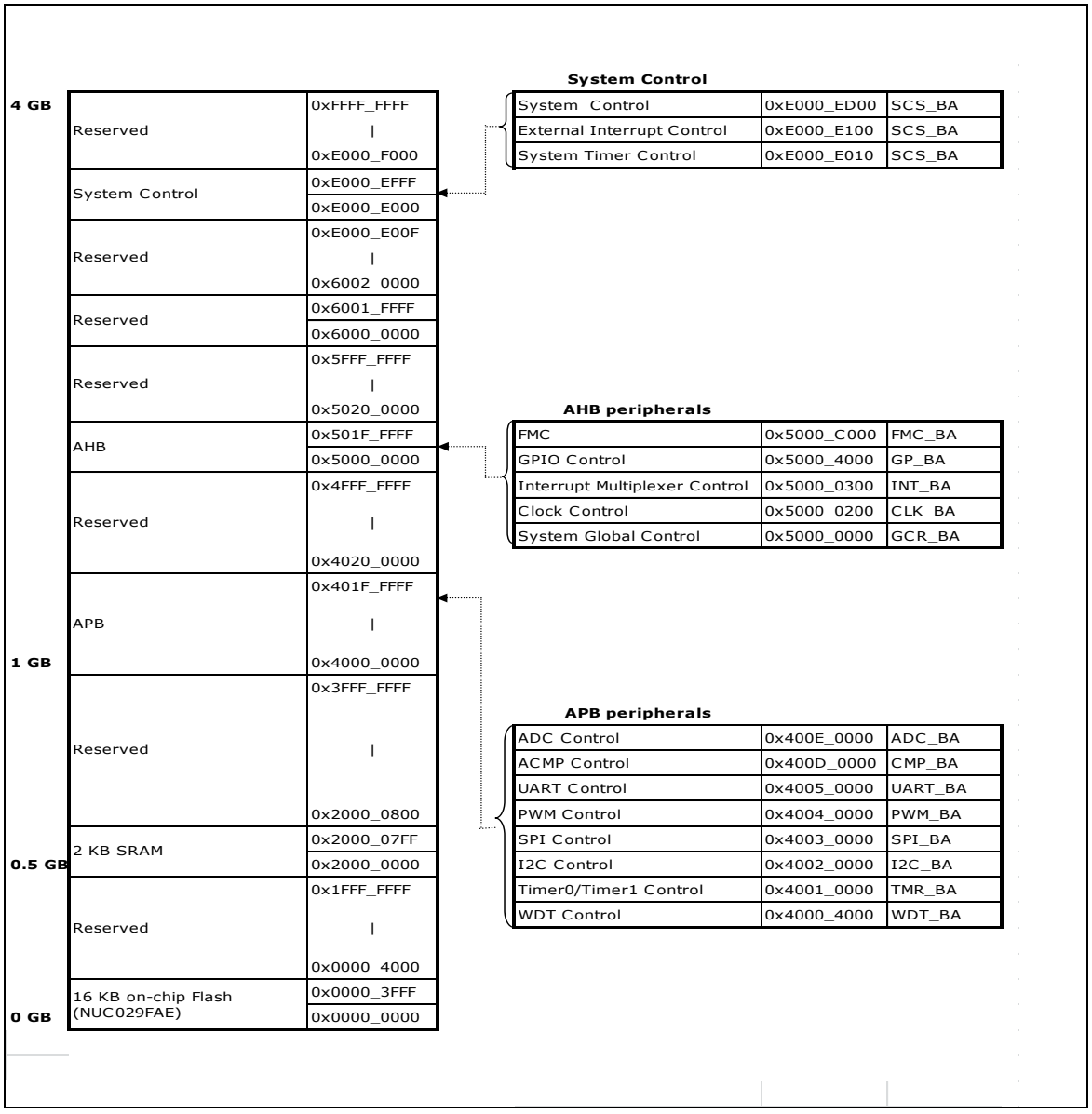


Figure 5-5 NuMicro® NUC029FAE Whole System Memory Mapping

5.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.7 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.7.1 *Exception Model and System Interrupt Map*

The following table lists the exception model supported by NuMicro® NUC029 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-3 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
1 ~ 15	-	-	-	System exceptions	-
16	0	**BOD_INT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P3.3 pin	Yes
20	4	**P0/1_INT**	GPIO	External signal interrupt from P0[7:0]/P1[7:0]	Yes
21	5	**P2/3/4_INT**	GPIO	External signal interrupt from P2[7:0]/P3[7:0]/P4[7:0], except P3.2 and P3.3	Yes
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt	No
23	7	**PWMB_INT**	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt	No
24	8	**TMR0_INT**	TMR0	Timer0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer1 interrupt	Yes
26	10	**TMR2_INT**	TMR2	Timer2interrupt	Yes
27	11	**TMR3_INT**	TMR3	Timer3 interrupt	Yes
28	12	**UART0_INT**	UART0	UART0 interrupt	Yes
29	13	**UART1_INT**	UART1	UART1 interrupt	Yes
30	14	**SPI0_INT**	SPI0	SPI0 interrupt	No
31	15	**SPI1_INT**	SPI1	SPI1 interrupt	No
32 ~ 33	16 ~ 17	-	-	Reserved	-
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt	Yes
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt	Yes
36 ~ 40	20 ~ 24	-	-	Reserved	-
41	25	**ACMP01_INT**	ACMP0/1	Analog Comparator0 or Comparator1 interrupt	Yes
42	26	**ACMP23_INT**	ACMP2/3	Analog Comparator2 or Comparator3 interrupt	Yes
43	27	-	-	Reserved	-
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	Reserved	-

Table 5-4 NuMicro® NUC029xAN System Interrupt Map

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
1 ~ 15	-	-	-	System exceptions	-
16	0	**BOD_INT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	-	-	Reserved	-
20	4	**P0/1_INT**	GPIO	External signal interrupt from P0[7:0]/P1[7:0]	Yes
21	5	**P2/3/4_INT**	GPIO	External signal interrupt from P2[7:0]/P3[7:0]/P4[7:0], except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM interrupt	No
24	8	**TMR0_INT**	TMR0	Timer0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer1 interrupt	Yes
26 ~ 27	10 ~ 11	-	-	Reserved	-
28	12	**UART_INT**	UART	UART interrupt	Yes
29	13	-	-	Reserved	-
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	-	-	Reserved	-
32	16	**GP5_INT**	GPIO	External signal interrupt from P5	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	NO
34	18	**I2C_INT**	I^2C	I^2C interrupt	Yes
35 ~ 40	19 ~ 24	-	-	Reserved	-
41	25	**ACMP_INT**	ACMP	Analog Comparator interrupt	Yes
42 ~ 43	26 ~ 27	-	-	Reserved	-
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	Reserved	-

Table 5-5 NuMicro® NUC029FAE System Interrupt Map

5.2.7.2 *Vector Table*

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 5-6 Vector Table Format

5.2.7.3 *Operation Description*

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

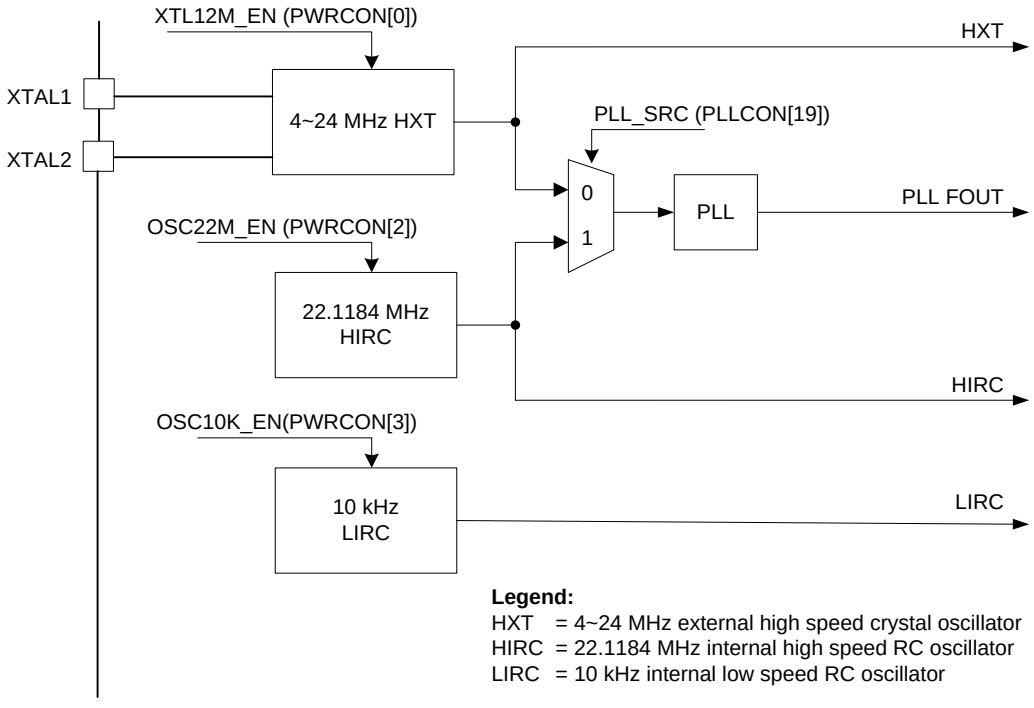
5.3 Clock Controller of NuMicro® NUC029xAN

5.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC)to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

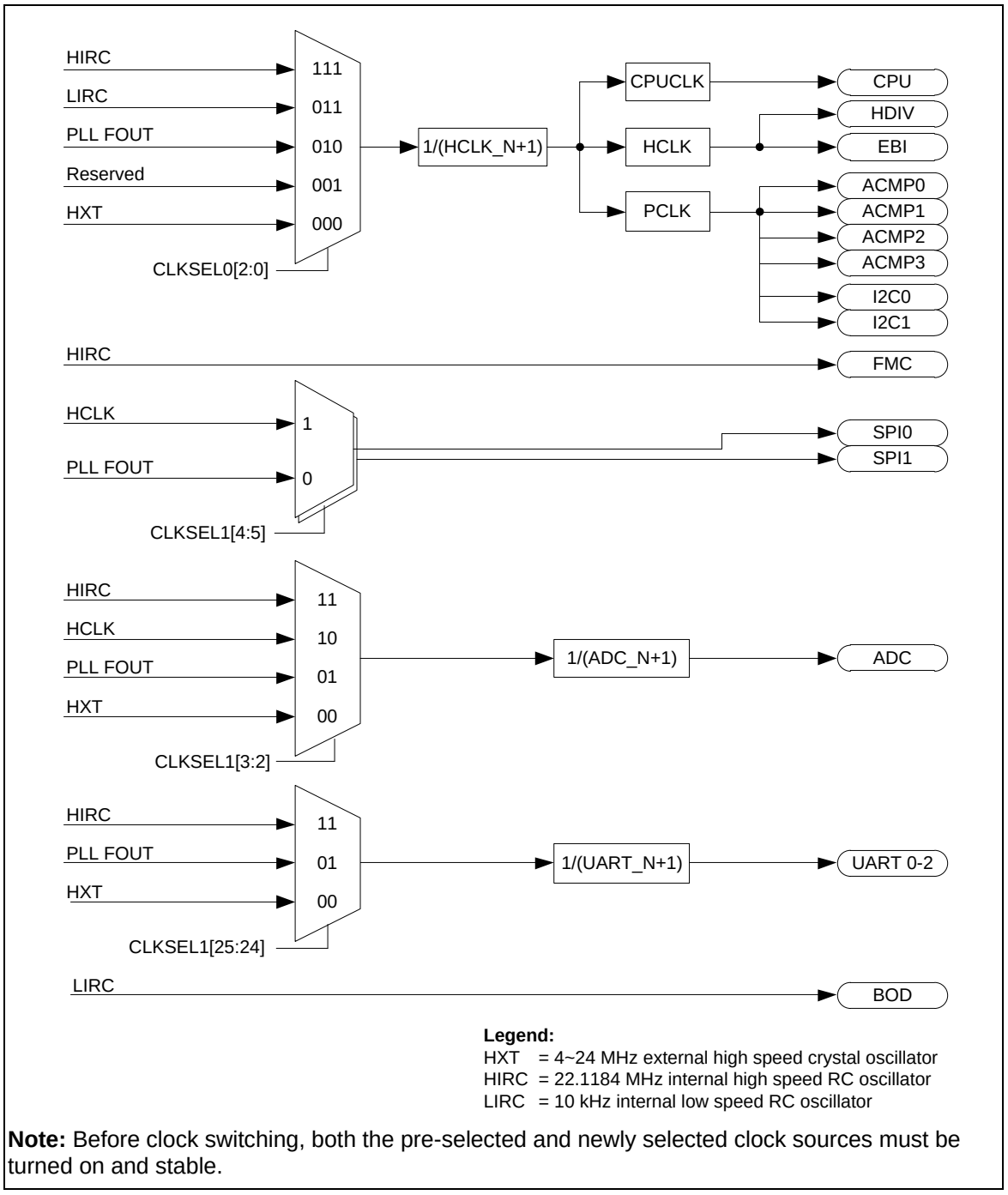
The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL source can be selected from external 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC)) (PLL FOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)



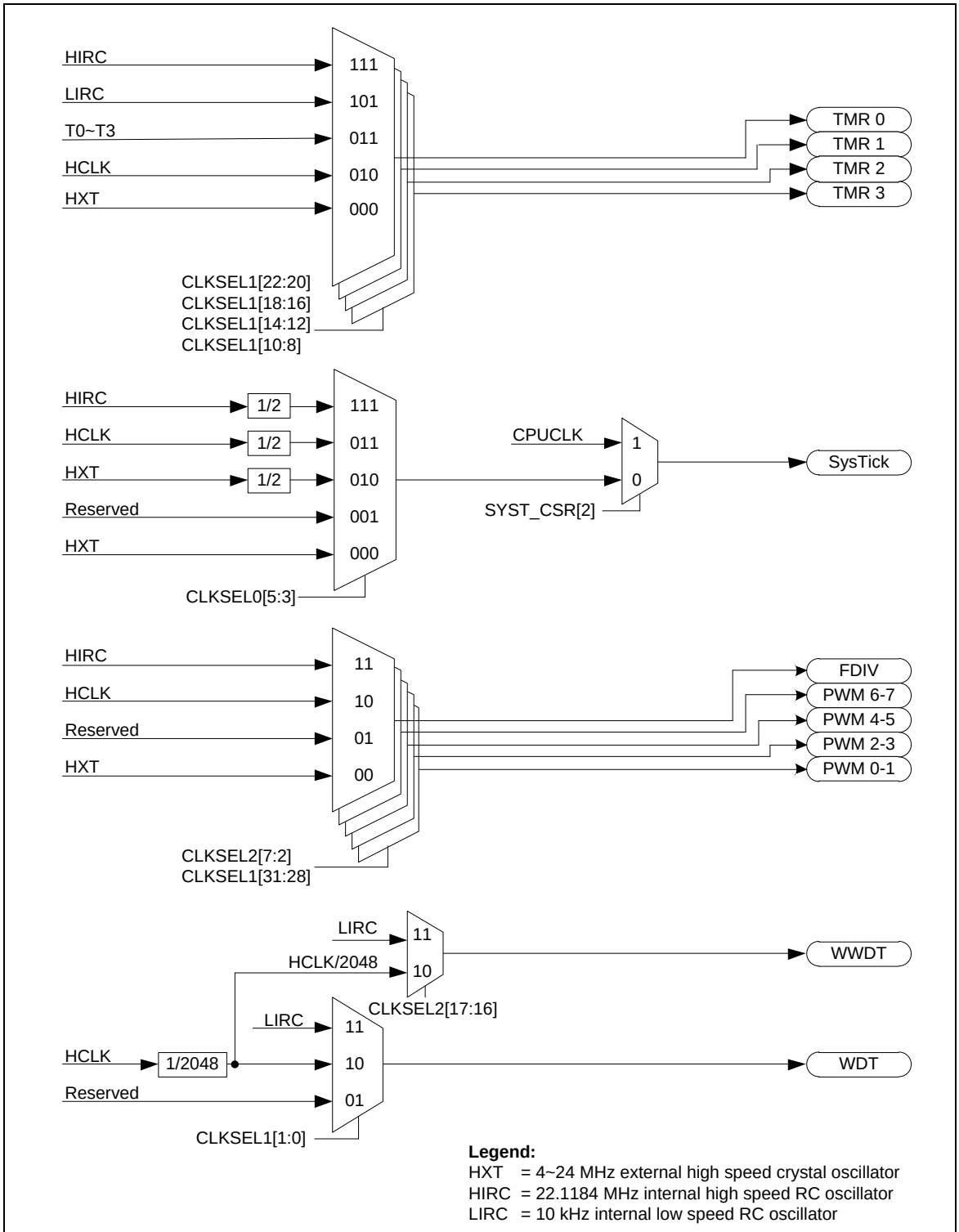
Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-6 NuMicro® NUC029xAN Clock Generator Block Diagram



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-7 NuMicro® NUC029xAN Clock Source Controller Overview (1/2)

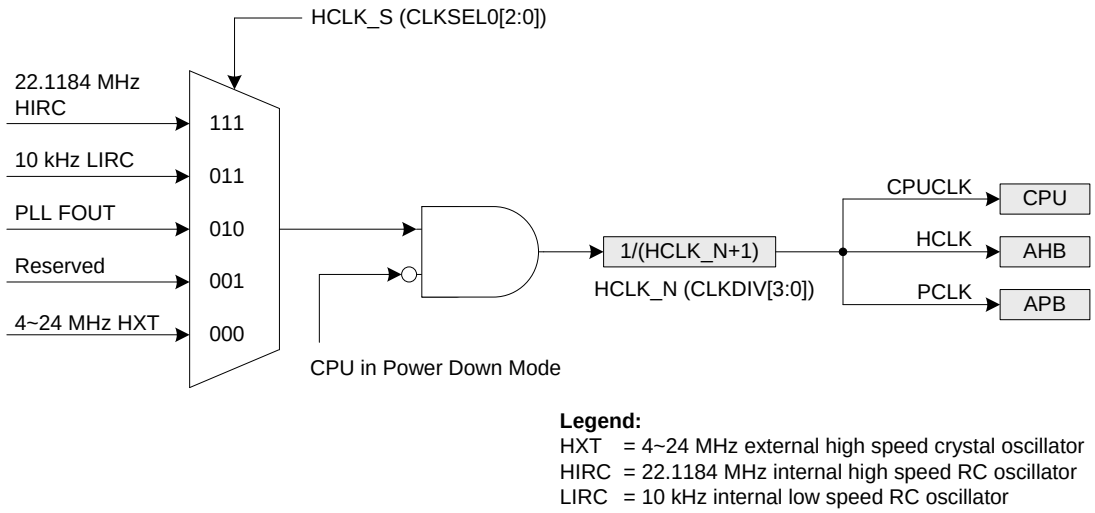


Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-8 NuMicro® NUC029xAN Clock Source Controller Overview (2/2)

5.3.2 System Clock and SysTick Clock

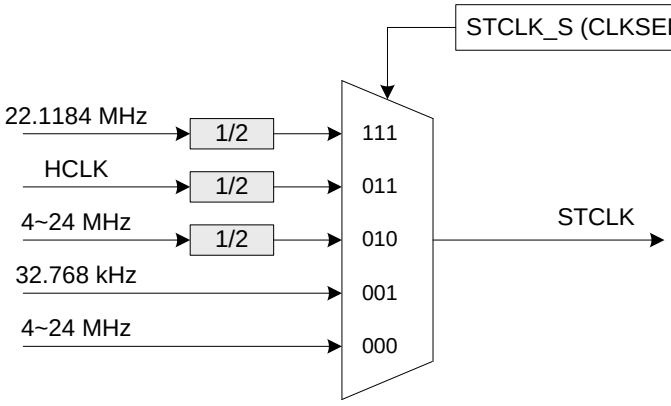
The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 5-9.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-9 NuMicro® NUC029xAN System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 5-10.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-10 NuMicro® NUC029xAN SysTick Clock Control Block Diagram

5.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

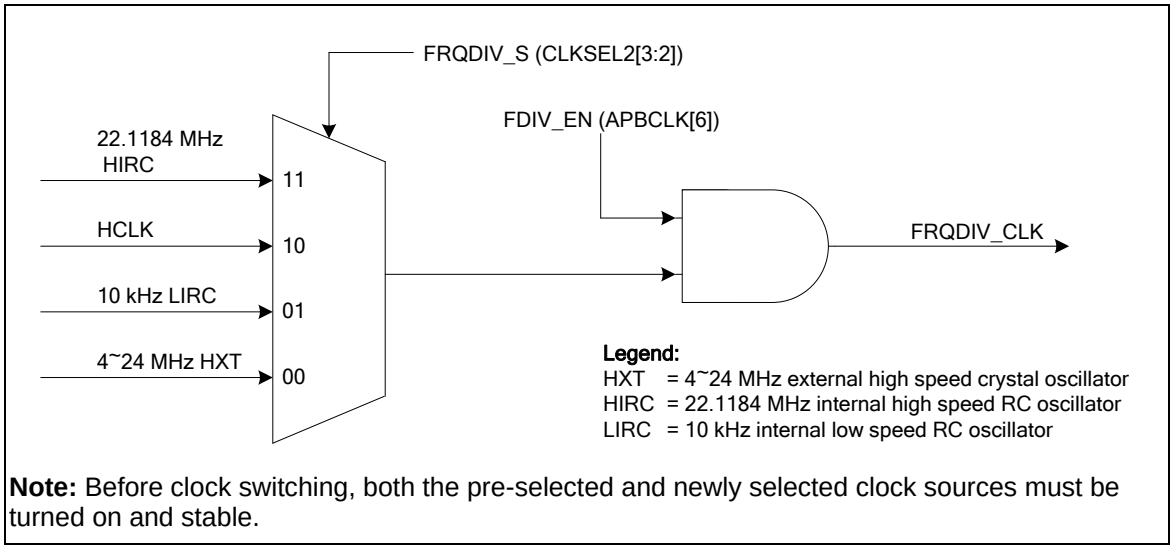
- Clock Generator
  - 10 kHz internal low speed RC oscillator clock (LIRC)
- Peripherals Clock (when 10 kHz intertnal low speed RC oscillator is adopted as clock source)

5.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-11 NuMicro® NUC029xAN Clock Source of Frequency Divider

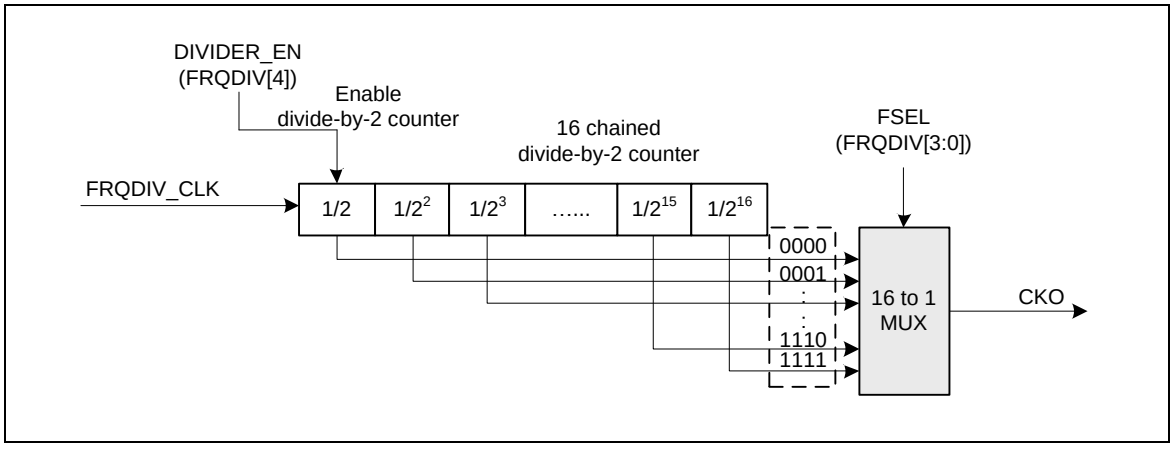


Figure 5-12 NuMicro® NUC029xAN Frequency Divider Block Diagram

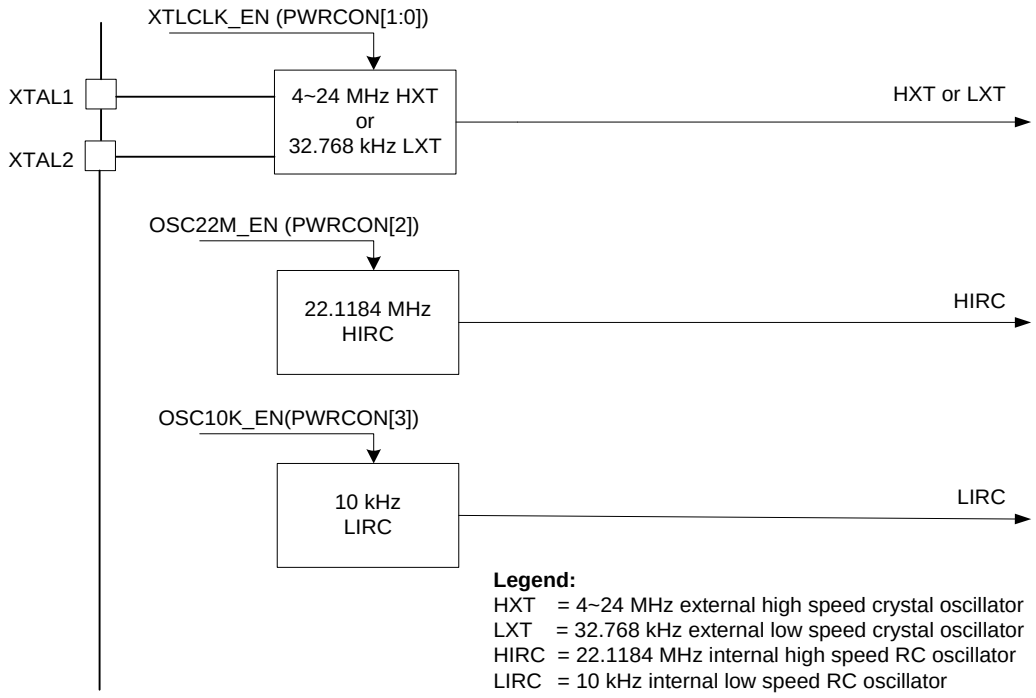
5.4 Clock Controller of NuMicro® NUC029FAE

5.4.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC)to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 3 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT) or 32.768 kHz external low speed crystal oscillator (LXT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

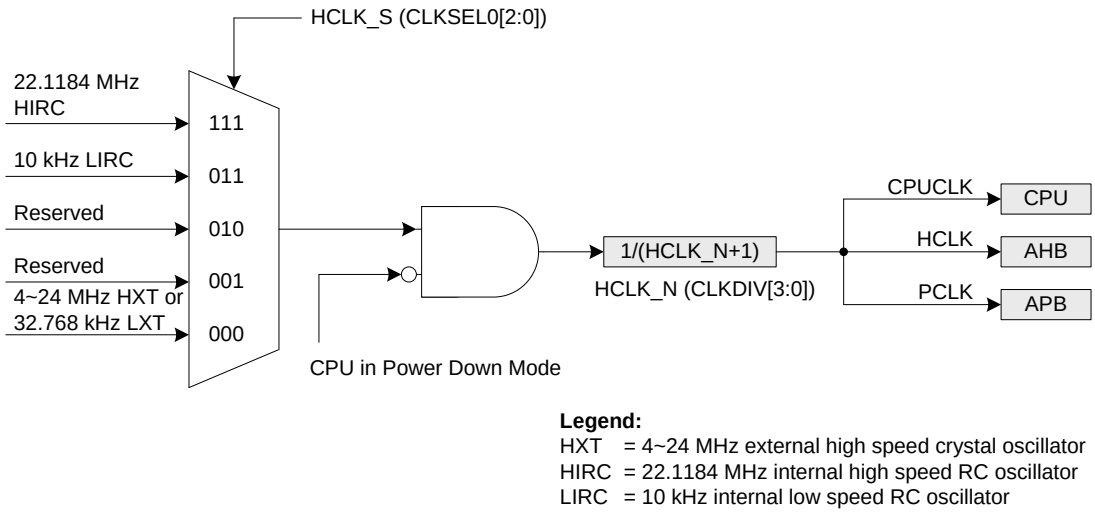


Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-13 NuMicro® NUC029FAE Clock Generator Block Diagram

5.4.2 System Clock and SysTick Clock

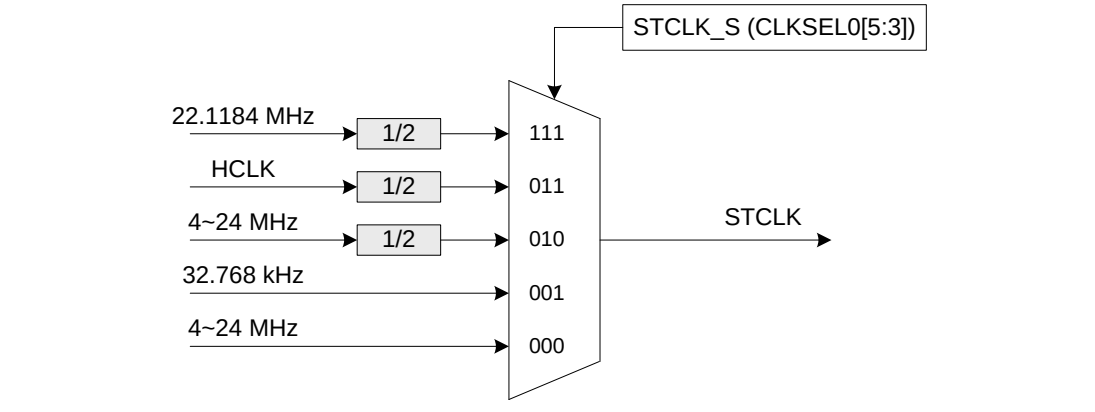
The system clock has 3 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 5-14.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-14 NuMicro® NUC029FAE System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 5-15.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 5-15 NuMicro® NUC029FAE SysTick Clock Control Block Diagram

5.4.3 ISP Clock Source Selection

The clock source of ISP is from AHB clock (HCLK). Please refer to the register AHBCLK.

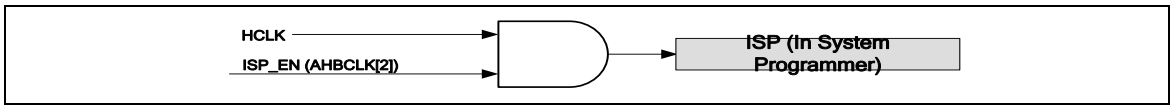


Figure 5-16 NuMicro® NUC029FAE AHB Clock Source for HCLK

5.4.4 Module Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals.

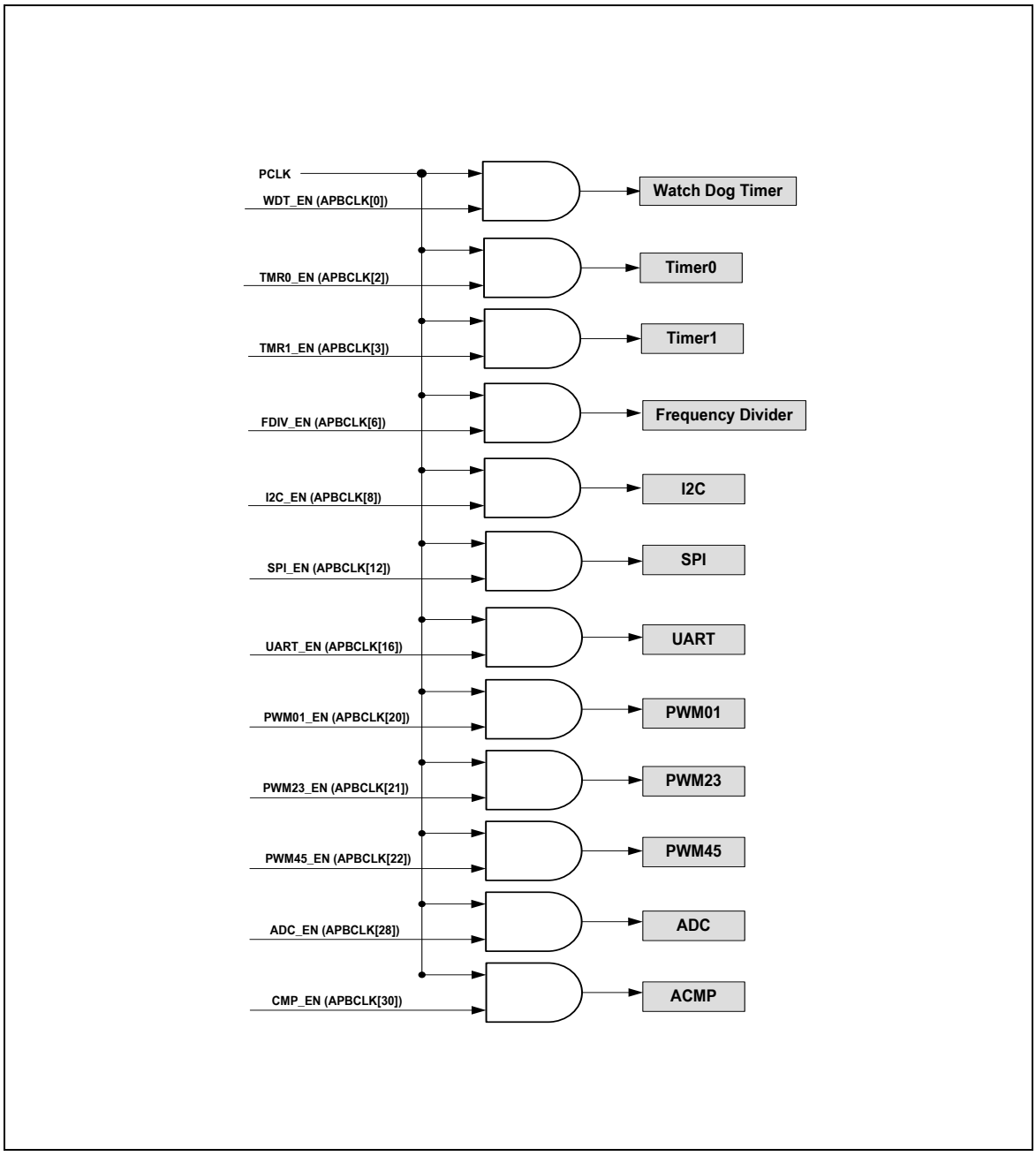


Figure 5-17 NuMicro® NUC029FAE Peripherals Clock Source Selection for PCLK

	Ext. CLK (HXT Or LXT)	HIRC	LIRC	PCLK
WDT	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes
I^2C	No	No	No	Yes
SPI	No	No	No	Yes
UART	Yes	Yes	No	No
PWM	No	No	No	Yes
ADC	Yes	Yes	No	Yes
ACMP	No	No	No	Yes

Table 5-7 NuMicro® NUC029FAE Peripheral Clock Source Selection Table

5.4.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator clock (LIRC)
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PD_32K = 1 and XTLCLK_EN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

5.5 Flash Memory Controller (FMC)

5.5.1 Overview

The NuMicro® NUC029 series has 64/32/16K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0.

The NuMicro® NUC029 series also provides additional Data Flash for user to store some application dependent data before chip power off. The NUC029xAN provides additional 4 Kbytes DATA Flash, and NUC029FAE provides Data Flash that is shared with APROM and its start address is configurable and defined by user in CONFIG1.

5.5.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access
- 64/32/16 KB application program memory (APROM)
- Up to 4KB In-System-Programming (ISP) loader program memory (LDROM)
- Fixed 4KB Data Flash for NUC029xAN
- Configurable Data Flash size and Programmable Data Flash start address for NUC029FAE
- All embedded flash memory supports 512 bytes page erase
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

5.6 External Bus Interface (EBI) (NUC029LAN/NUC029NAN Only)

5.6.1 Overview

The NuMicro® NUC029LAN/NUC029NAN has an external bus interface (EBI) to access external device. To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. Also, address latch enable (ALE) signal is used to differentiate the address and data cycle.

5.6.2 Features

- Supports external devices with maximum 64 KB size (8-bit data width) / 128 KB (16-bit data width)
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports 8-bit or 16-bit data width
- Supports variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD)
- Supports address bus and data bus multiplex mode to save the address pins
- Supports configurable idle cycle for different access condition: Write command finish (W2X), Read-to-Read (R2R)
- Supports zero address hold time with read/write operation and write buffer for write operation to enhance read/write performance

5.7 General Purpose I/O (GPIO)

5.7.1 Overview

The NuMicro® NUC029 series has up to 40 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 40 pins are arranged in 6 ports named as P0, P1, P2, P3, P4 and P5. Each port has the maximum of 8 pins. Each of the 40 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. Each I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

5.7.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by Px_TYPE[15:0] in Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by CIOINI(CONFIG[10]) setting
  - For NUC029xAN:
    - If CIOINI is 0, all GPIO pins in input tri-state mode after chip reset
    - If CIOINI is 1, all GPIO pins in Quasi-bidirectional mode after chip reset (Default)

    After reset, the I/O mode of all pins are stay in Quasi-bidirectional mode and each port data register Px_DOUT[7:0] resets to 0x000_00FF.
  - For NUC029FAE:
    - If CIOINI is 0, all GPIO pins in Quasi-bidirectional mode after chip reset
    - If CIOINI is 1, all GPIO pins in input tri-state mode after chip reset (Default)
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

5.8 Timer Controller (TIMER)

5.8.1 Overview

The timer controller includes up to 4 sets 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

5.8.2 Features

- Up to 4 sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external counter pin (T0~T3)
- 24-bit capture value is readable through TCAP (Timer Capture Data Register)
- Supports external pin capture (T0EX~T3EX) for interval measurement
- Supports external pin capture (T0EX~T3EX) for reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports internal capture triggered while internal ACMP output signal transition (NUC029xAN only)
- Supports Inter-Timer trigger mode (NUC029xAN only)
- Supports internal signal (CPO0, CPO1) for interval measurement (NUC029FAE only)

5.9 PWM Generator and Capture Timer (PWM) (NUC029xAN Only)

5.9.1 Overview

The NuMicro® NUC029xAN has 2 sets of PWM group supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide 8 independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DZEN01 (PCR[4]) is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then starts decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (CCR0[1]) (Rising latch Interrupt enable) and CFL_IE0 (CCR0[2]) (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CRL_IE1 (CCR0[17]) and CFL_IE1 (CCR0[18]). And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0.

5.9.2 Features

5.9.2.1 PWM Function:

- Up to 2 PWM groups (PWMA/PWMB) to support 8 PWM channels or 4 complementary PWM paired channels
- Each PWM group has two PWM generators with each PWM generator supporting one 8-bit prescaler, one clock divider, two PWM-timers, one Dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- One-shot or Auto-reload mode
- Edge-aligned type or Center-aligned type option
- PWM trigger ADC start-to-conversion

5.9.2.2 Capture Function:

- Timing control logic shared with PWM Generators
- Supports 8 Capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLRx), one falling latch register (CFLRx) and Capture interrupt flag (CAPIFx)

5.10 Enhanced PWM Generator (NUC029FAE Only)

5.10.1 Overview

The NuMicro® NUC029FAE has built one PWM unit which is specially designed for motor driving control applications. The PWM unit supports six PWM generators which can be configured as three independent PWM outputs, PWM2, PWM3 and PWM5, or as three complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with three programmable dead-zone generators.

Every complementary PWM pairs share one 8-bit prescaler. There are six clock dividers providing five divided frequencies (1, 1/2, 1/4, 1/8, 1/16) for each channel. Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide twelve independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer, ACMP and ADC to work together. In order to control motor more precisely, we provide some registers that not only configure PWM but also Timer, ADC and ACMP, by doing so, it can save more CPU time and control motor with ease especially in BLDC.

5.10.2 Features

The PWM unit supports the following features:

- Independent 16-bit PWM duty control units with maximum six port pins:
  - Three independent PWM outputs –PWM2, PWM3 and PWM5
  - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-zone insertion – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
- Group control bit – PWM2 and PWM4 are synchronized with PWM0, PWM3 and PWM5 are synchronized with PWM1
- One-shot (only support edge alignment mode) or Auto-reload mode PWM
- Up to 16-bit resolution
- Supports Edge-aligned and Center-aligned mode
- Programmable dead-zone insertion between complementary paired PWMs
- Each pin of PWM0 to PWM5 has independent polarity setting control
- Hardware fault brake protections
  - Two Interrupt source types:

- Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned mode) or underflow (edge-aligned mode)
- Requested when external fault brake asserted
  - BKP0: EINT0 or CPO1

- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register
- Supports independently rising CMR matching (in Center-aligned mode), CNR matching (in Center-aligned mode), falling CMR matching, period matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Provides interrupt accumulation function

5.11 Watchdog Timer (WDT)

5.11.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

5.11.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period (NUC029xAN only)
  - Selectable it includes (1026、130、18 or 3) * WDT_CLK reset delay period
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG0[31] Watchdog Enable) bit is set to 0 (NUC029xAN only)
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

5.12 Window Watchdog Timer (WWDT) (NUC029xAN Only)

5.12.1 Overview

The NuMicro® NUC029xAN supports The Window Watchdog Timer (WWDT). WWDT is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

5.12.2 Features

- 6-bit down counter value WWDTCVAL (WWDTVAL[5:0]) and 6-bit compare window value WINCMP (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value to programmable maximum 11-bit prescale counter period of WWDT counter

5.13 UART Interface Controller (UART)

5.13.1 Overview

The NuMicro® NUC029 series provides up to 2 channels of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART, and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function and RS-485 function mode. The NUC029xAN also supports LIN master/slave function mode. Each UART Controller channel supports six types of interrupts. NUC029xAN has seventh interrupt, LIN receiver break field detected interrupt (LIN_RX_BREAK_INT).

5.13.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports 3-/16-bit duration for normal mode
- Supports RS-485 function mode.
  - Supports RS-485 9-bit mode
  - Supports hardware or software enable to control RS-485 transmission direction by programming RTS pin
- Supports LIN function mode (NUC029xAN only)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver

5.14 I²C Serial Interface Controller (I²C)

5.14.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

5.14.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Support FIFO function (NUC029FAE only)

5.15 Serial Peripheral Interface (SPI)

5.15.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro® NUC029 series contains up to 2 sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

5.15.2 Features

- Up to 2 sets of SPI controllers
- Supports Master or Slave mode operation
- Configurable bit length of a transaction word from 8 to 32 bits
- Provides separate 4-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports Slave 3-wire mode
- Supports PLL clock source (NUC029xAN only)

5.16 Analog-to-Digital Converter (ADC)

5.16.1 Overview

The NuMicro® NUC029xAN contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels, and The NuMicro® NUC029FAE contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels.

The A/D converter of NUC029xAN supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode, and the A/D converter of NUC029xAN only supports Single mode.

The A/D converter can be started by software, PWM trigger and external STADC pin.

5.16.2 Features

- Analog input voltage range: 0~AV_{DD}
- 12-bit resolution and 10-bit accuracy is guaranteed (NUC029xAN only)
- 10-bit resolution and 8-bit accuracy is guaranteed (NUC029FAE only)
- Up to 8 single-end analog input channels
  - Or 4 differential analog input channels (NUC029xAN only)
- Up to 760 kSPS sample rate for NUC029xAN
- 300 KSPS (V_{DD} 4.5V - 5.5V) and 200 KSPS (V_{DD} 2.5V - 5.5V) conversion rate for NUC029FAE
- Four operating modes (NUC029FAE only supports Single mode)
  - Single mode: A/D conversion is performed one time on a specified channel
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous Scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
  - Writing 1 to ADST bit (ADCR[11]) through software
  - PWM trigger with optional start delay period
  - External pin STADC
- Each conversion result is held in data register with valid and overrun indicators
- Each channel has individual data regiter (NUC029xAN only)
- The conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 3 input sources:
  - external analog voltage
  - internal Band-gap voltage

- internal temperature sensor output (NUC029xAN only)

5.17 Analog Comparator (ACMP)

5.17.1 Overview

The NuMicro® NUC029 series contains up to four sets of comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input voltage is greater than negative input voltage; otherwise the output is logic 0. Each comparator can be configured to generate interrupt request when the comparator output value changes.

5.17.2 Features

- Up to four sets of Comparator analog modules
- Analog input voltage range: 0~ V_{DD}
- Supports Hysteresis function
- Optional internal reference voltage source for each comparator negative input
- Two interrupt vectors for the four analog comparators
- External input or internal band-gap voltage selectable at negative node
- Interrupt when compared results change
- Power-down wake-up

5.18 Hardware Divider (HDIV) (NUC029xAN Only)

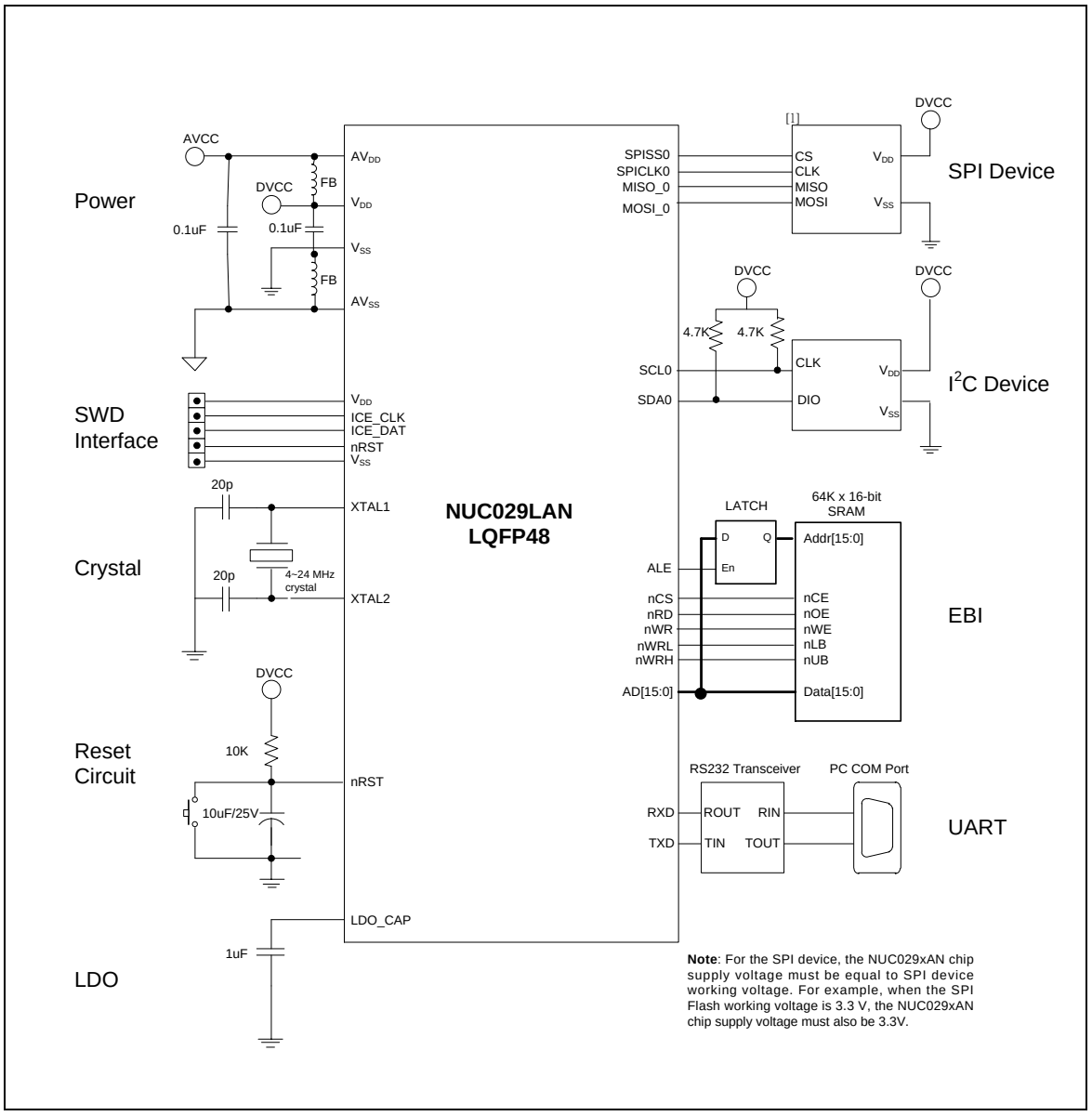
5.18.1 Overview

The NuMicro® NUC029xAN has the hardware divider (HDIV). HDIV is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

5.18.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6 APPLICATION CIRCUIT



Note: For the SPI device, the NUC029xAN chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the NUC029xAN chip supply voltage must also be 3.3V.

7 NUC029XAN ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}	I_{DD}	-	120	mA
Maximum Current out of V_{SS}	I_{SS}	-	120	mA
Maximum Current sunk by a I/O pin	I_{IO}	-	35	mA
Maximum Current sourced by a I/O pin		-	35	mA
Maximum Current sunk by total I/O pins		-	100	mA
Maximum Current sourced by total I/O pins		-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=5.5 V, T_A = 25°C)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation Voltage	V_{DD}	2.5	-	5.5	V	V_{DD} = 2.5V ~ 5.5V up to 50 MHz				
Power Ground	V_{SS} AV_{SS}	-0.3	-	-	V	-				
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} > 2.5V				
Band-gap Voltage	V_{BG}	1.16	1.20	1.24	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25°C				
		1.14	1.20	1.24	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40°C ~ 85°C				
Allowed Voltage Difference for V_{DD} and AV_{DD}	V_{DD}-AV_{DD}	-0.3	0	0.3	V	-				
Operating Current Normal Run Mode HCLK = 50 MHz while(1){} Excuted from Flash	I_{DD1}	-	21	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	12 MHz	X	V	V
	I_{DD2}	-	15	-	mA	5.5V	12 MHz	X	V	X
	I_{DD3}	-	20	-	mA	3.3V	12 MHz	X	V	V
	I_{DD4}	-	13	-	mA	3.3V	12 MHz	X	V	X
Operating Current Normal Run Mode HCLK = 22.184 MHz while(1){} Excuted from Flash	I_{DD5}	-	6.6	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	X	V	X	V
	I_{DD6}	-	3.7	-	mA	5.5V	X	V	X	X
	I_{DD7}	-	6.4	-	mA	3.3V	X	V	X	V
	I_{DD8}	-	3.6	-	mA	3.3V	X	V	X	X
Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Excuted from Flash	I_{DD9}	-	5.4	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	12 MHz	X	X	V
	I_{DD10}	-	3.6	-	mA	5.5V	12 MHz	X	X	X
	I_{DD11}	-	4.0	-	mA	3.3V	12 MHz	X	X	V
	I_{DD12}	-	2.3	-	mA	3.3V	12 MHz	X	X	X
Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Excuted from Flash	I_{DD13}	-	3.3	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	4 MHz	X	X	V
	I_{DD14}	-	2.5	-	mA	5.5V	4 MHz	X	X	X
	I_{DD15}	-	2.0	-	mA	3.3V	4 MHz	X	X	V
	I_{DD16}	-	1.3	-	mA	3.3V	4 MHz	X	X	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNIT						
Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Excuted from Flash	I_{DD17}	-	110	-	μA	V_{DD}	HXT	HIRC	LIRC	PLL	All digital modules
						5.5V	X	X	V	X	V[4]
	I_{DD18}	-	105	-	μA	5.5V	X	X	V	X	X
	I_{DD19}	-	92	-	μA	3.3V	X	X	V	X	V[4]
	I_{DD20}	-	90	-	μA	3.3V	X	X	V	X	X
Operating Current Idle Mode HCLK = 50 MHz	I_{IDLE1}	-	17	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	12 MHz	X	V	V	
	I_{IDLE2}	-	10	-	mA	5.5V	12 MHz	X	V	X	
	I_{IDLE3}	-	15	-	mA	3.3V	12 MHz	X	V	V	
	I_{IDLE4}	-	8	-	mA	3.3V	12 MHz	X	V	X	
Operating Current Idle Mode HCLK= 22.1184 MHz	I_{IDLE5}	-	4.5	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	X	V	X	V	
	I_{IDLE6}	-	1.6	-	mA	5.5V	X	V	X	X	
	I_{IDLE7}	-	4.4	-	mA	3.3V	X	V	X	V	
	I_{IDLE8}	-	1.6	-	mA	3.3V	X	V	X	X	
Operating Current Idle Mode HCLK = 12 MHz	I_{IDLE9}	-	4.1	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	12 MHz	X	X	V	
	I_{IDLE10}	-	2.4	-	mA	5.5V	12 MHz	X	X	X	
	I_{IDLE11}	-	2.8	-	mA	3.3V	12 MHz	X	X	V	
	I_{IDLE12}	-	1.2	-	mA	3.3V	12 MHz	X	X	X	
Operating Current Idle Mode HCLK = 4 MHz	I_{IDLE13}	-	2.9	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	4 MHz	X	X	V	
	I_{IDLE14}	-	2.1	-	mA	5.5V	4 MHz	X	X	X	
	I_{IDLE15}	-	1.6	-	mA	3.3V	4 MHz	X	X	V	
	I_{IDLE16}	-	0.9	-	mA	3.3V	4 MHz	X	X	X	
Operating Current Idle Mode HCLK = 10 kHz	I_{IDLE17}	-	106	-	μA	V_{DD}	HXT	HIRC	LIRC	PLL	All digital modules
						5.5V	X	X	V	X	V[4]
	I_{IDLE18}	-	104	-	μA	5.5V	X	X	V	X	X
	I_{IDLE19}	-	90	-	μA	3.3V	X	X	V	X	V[4]
	I_{IDLE20}	-	89	-	μA	3.3V	X	X	V	X	X
Standby Current	I_{PWD1}	-	10	-	μA	V_{DD} = 5.5V, All oscillators and analog blocks turned off					

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Power-down Mode (Deep Sleep Mode)	I_{PWD2}	-	8	-	μA	V_{DD} = 3.3V, All oscillators and analog blocks turned off
Logic 0 Input Current P0/1/2/3/4 (Quasi-bidirectional mode)	I_{IL}	-	-65	-75	μA	V_{DD} = 5.5V, V_{IN} = 0V
Logic 1 to 0 Transition Current P0/1/2/3/4 (Quasi-bidirectional mode)	I_{TL} [3]	-	-690	-750	μA	V_{DD} = 5.5V, V_{IN} = 2.0V
Input Leakage Current P0/1/2/3/4	I_{LK}	-1	-	+1	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD} Open-drain or input only mode
Input Low Voltage P0/1/2/3/4 (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6	V	V_{DD} = 2.5V
Input High Voltage P0/1/2/3/4 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.3	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.3	V	V_{DD} =3.0V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4	V	V_{DD} = 2.5V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.3	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.3	V	V_{DD} = 3.0V
Negative going threshold (Schmitt input), nRST	V_{ILS}	-0.3	-	0.2 V_{DD}	V	-
Positive going threshold (Schmitt input), nRST	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V	-
Internal nRST Pin Pull-up Resistor	R_{RST}	40		150	kΩ	-
Negative going threshold (Schmitt input), P0/1/2/3/4	V_{ILS}	-0.3	-	0.3 V_{DD}	V	-
Positive going threshold (Schmitt input), P0/1/2/3/4	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V	-
Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	I_{SR11}	-300	-420	-	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-75	-	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-67	-	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current P0/1/2/3/4 (Push-pull Mode)	I_{SR21}	-20	-26	-	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-3	-5	-	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-2.5	-4.2	-	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current P0/1/2/3/4 (Quasi-bidirectional and Push-pull Mode)	I_{SK11}	10	16	-	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK12}	6	9	-	mA	V_{DD} = 2.7V, V_S = 0.45V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{SK13}	5	8	-	mA	V_{DD} = 2.5V, V_S = 0.45V

Note 1: nRST pin is a Schmitt trigger input.

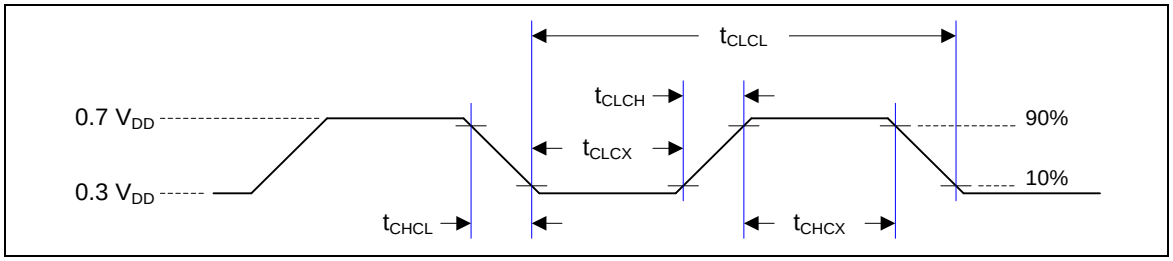
Note 2: XTAL1 is a CMOS input.

Note 3: Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD} = 5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

Note 4: Only enable modules which support 10 kHz LIRC clock source.

7.3 AC Electrical Characteristics

7.3.1 External Input Clock



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time	-	10	-	-	ns
t_{CLCX}	Clock Low Time	-	10	-	-	ns
t_{CLCH}	Clock Rise Time	-	2	-	15	ns
t_{CHCL}	Clock Fall Time	-	2	-	15	ns

7.3.2 External 4~24 MHz High Speed Crystal (HXT)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HXT}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
T_A	Temperature	-	-40	-	85	℃
I_{HXT}	Operating Current	12 MHz at V_{DD} = 5V	-	2	-	mA
		12 MHz at V_{DD} = 3.3V	-	0.8	-	mA
f_{HXT}	Clock Frequency	-	4	-	24	MHz

7.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	10~20pF	10~20pF

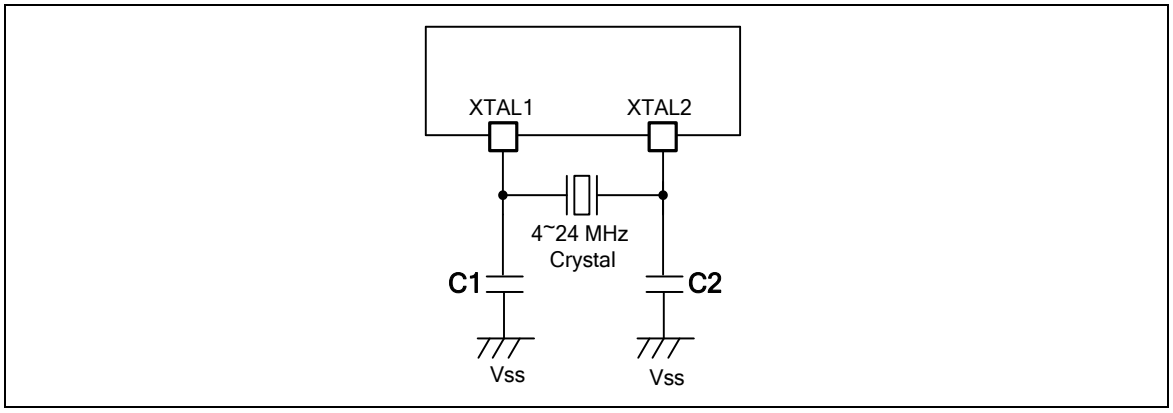


Figure 7-1 NUC029xAN Typical Crystal Application Circuit

7.3.3 Internal 22.1184 MHz High Speed RC Oscillator (HIRC)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HRC}[1]	Operation Voltage V_{DD}	-	1.62	1.8	1.98	V
f_{HRC}	Center Frequency	-	-	22.1184	-	MHz
	Calibrated Internal Oscillator Frequency	T_A = 25 ℃, V_{DD} = 5 V	-1	-	+1	%
		T_A = -40 ~ 85 ℃, V_{DD} = 2.5 V ~ 5.5 V	-3	-	+3	%
I_{HRC}	Operation Current	T_A = 25 ℃, V_{DD} = 5 V	-	800	-	uA

Note: Operation voltage comes from internal LDO.

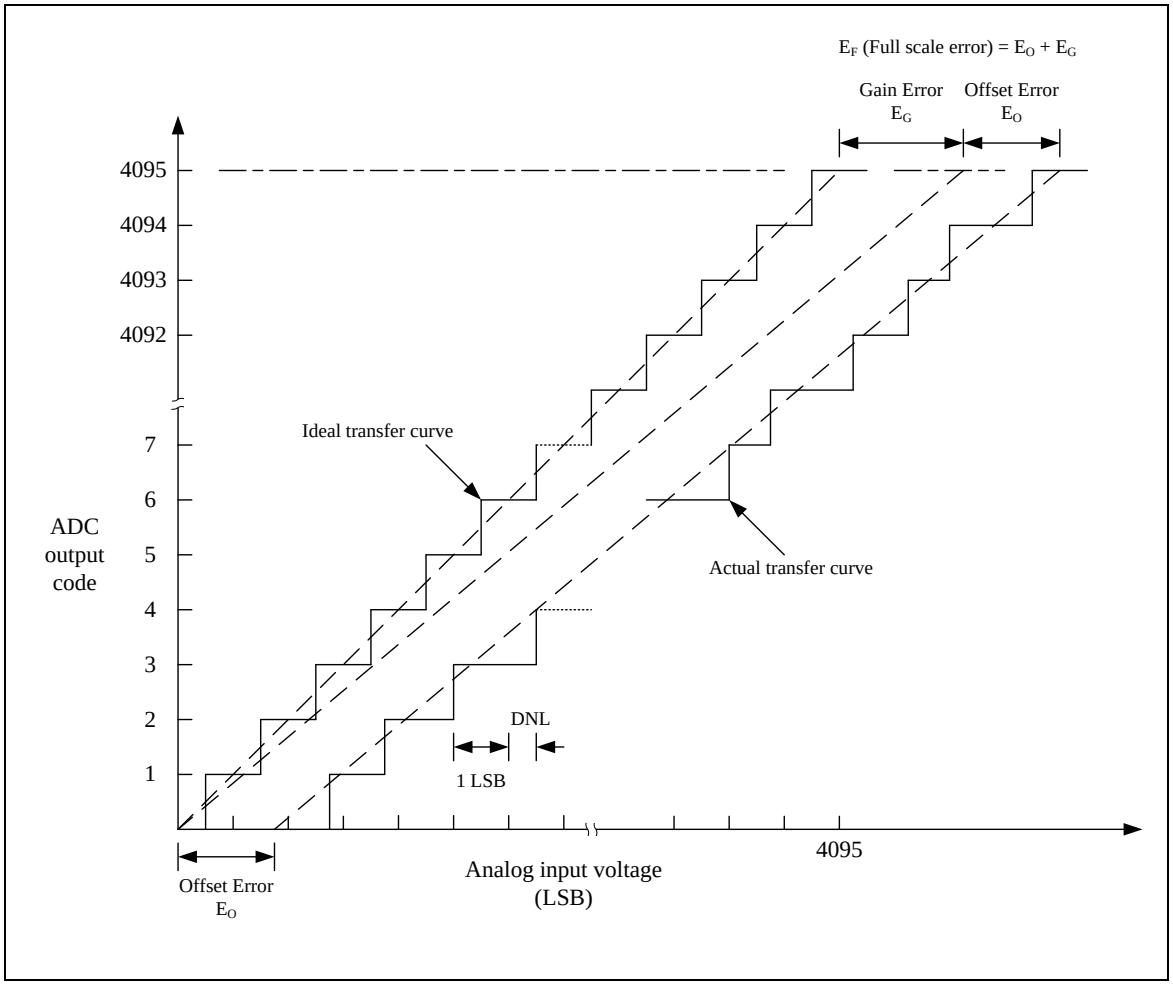
7.3.4 Internal 10 kHz Low Speed RC Oscillator (LIRC)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{LRC}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
f_{LRC}	Center Frequency	-	-	10	-	kHz
	Calibrated Internal Oscillator Frequency	T_A = 25 ℃, V_{DD} = 2.5 V ~ 5.5 V	-10	-	+10	%
		T_A = -40 ~ 85 ℃, V_{DD} = 2.5 V ~ 5.5 V	-40	-	+40	%

7.4 Analog Characteristics

7.4.1 12-bit SAR ADC Specification

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	±1	-1~4	LSB
INL	Integral nonlinearity error	-	±2	±4	LSB
E_O	Offset error	-	2	4	LSB
E_G	Gain error (Transfer gain)	-	-2	-4	LSB
E_A	Absolute Error	-	3	4	LSB
-	Monotonic	Guaranteed			
F_{ADC}	ADC clock frequency (AV_{DD} = 4.5V ~ 5.5V)	-	-	16	MHz
	ADC clock frequency (AV_{DD} = 2.5V ~ 5.5V)	-	-	8	MHz
F_S	Sample rate (F_{ADC}/T_{CONV}) (AV_{DD} = 4.5V ~ 5.5V)	-	-	800	kSPS
	Sample rate (F_{ADC}/T_{CONV}) (AV_{DD} = 2.5V ~ 5.5V)	-	-	400	kSPS
T_{ACQ}	Acquisition Time (Sample Stage)	7			1/ F_{ADC}
T_{CONV}	Total Conversion Time	20			1/ F_{ADC}
AV_{DD}	Supply voltage	2.5	-	5.5	V
I_{DDA}	Supply current (Avg.) (AV_{DD} = 5V)	-	2.9	-	mA
V_{IN}	Analog Input voltage	0	-	AV_{DD}	V
C_{IN}	Input Capacitance	-	3.2	-	pF
R_{IN}	Input Load	-	6	-	kΩ



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

7.4.2 LDO and Power Management Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	Input Voltage V_{DD}	-	2.5		5.5	V
V_{LDO}	Output Voltage	-	1.62	1.8	1.98	V
T_A	Operating Temperature	-	-40	25	85	℃
C_{LDO}	Capacitor	R_{ESR} = 1 Ω	-	1	-	μF

Note 1: It is recommended that a 0.1 uF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

Note 2: To ensure power stability, a 1 μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

7.4.3 Low Voltage Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Input Voltage AV_{DD}	-	0	-	5.5	V
T_A	Operating Temperature	-	-40	25	85	℃
I_{LVR}	Capacitor	AV_{DD} = 5.5 V	-	1	5	μF
V_{LVR}	Threshold Voltage	T_A = 25 ℃	1.90	2.00	2.20	V
		T_A = -40 ℃	2.00	2.10	2.40	V
		T_A = 85 ℃	1.70	1.90	2.10	V

7.4.4 Brown-out Detector Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Input Voltage AV_{DD}	-	0	-	5.5	V
T_A	Operating Temperature	-	-40	25	85	℃
I_{BOD}	Quiescent Current	AV_{DD} = 5.5 V	-	-	140	μA
V_{BOD}	Brown-out Voltage (Falling edge)	BOD_VL[1:0]=11	4.2	4.38	4.55	V
		BOD_VL [1:0]=10	3.5	3.68	3.85	V
		BOD_VL [1:0]=01	2.5	2.68	2.85	V
		BOD_VL [1:0]=00	2.0	2.18	2.35	V
V_{BOD}	Brown-out Voltage (Rising edge)	BOD_VL[1:0]=11	4.3	4.52	4.75	V
		BOD_VL [1:0]=10	3.5	3.8	4.05	V
		BOD_VL [1:0]=01	2.5	2.77	3.05	V
		BOD_VL [1:0]=00	2.0	2.25	2.55	V

7.4.5 Power-on Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_A	Operating Temperature	-	-40	25	85	℃
V_{POR}	Reset Voltage	V+	-	2	-	V
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	-	100	mV
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	-	0.025	-	-	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	-	0.5	-	-	ms

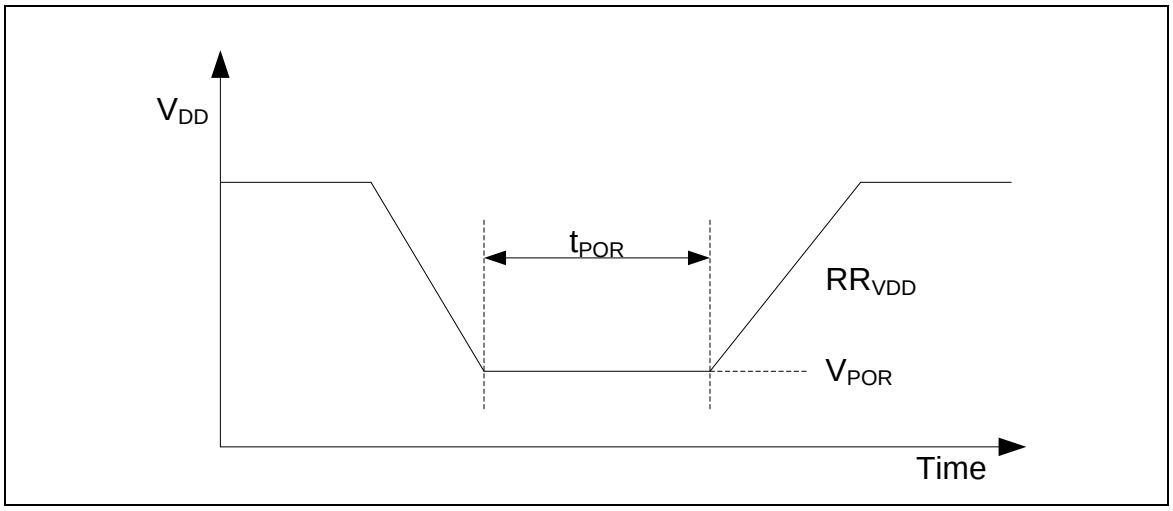


Figure 7-2 NUC029xAN Power-up Ramp Condition

7.4.6 Temperature Sensor Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{TEMP}[1]	Operating Voltage	-	1.62	1.8	1.98	V
T_A	Operating Temperature	-	-40	25	85	℃
I_{TEMP}	Current Consumption	-	-	16	-	μA
-	Gain	-	-1.65	-1.75	-1.85	mV/℃
-	Offset Voltage	T_A = 0 ℃	714	724	734	mV

Note 1: Operation voltage comes from internal LDO.

Note 2: The temperature sensor formula for the output voltage (Vtemp) is as below equation.

Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

7.4.7 Comparator Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CMP}	Operation Voltage AV_{DD}	-	2.5	-	5.5	V
T_A	Operation Temperature	-	-40	25	85	℃
I_{CMP}	Operation Current	AV_{DD} = 5 V	-	50	100	μA
V_{OFF}	Input Offset Voltage	-	-	10	20	mV
V_{SW}	Output Swing	-	0.1	-	AV_{DD}-0.1	V
V_{COM}	Input Common Mode Range	-	0.1	-	AV_{DD}-0.1	V
-	DC Gain	-	40	70	-	dB
T_{PGD}	Propagation Delay	V_{COM} = 1.2 V, V_{DIFF} = 0.1 V	-	200	-	ns
V_{HYS}	Hysteresis	-	-	±20	±30	mV
T_{STB}	Stable Time	-	-	-	1	μs

7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{FLA}[1]	Operation Voltage	-	1.62	1.8	1.98	V
T_{RET}	Data Retention	T_A = 25℃	10	-	-	year
T_{ERASE}	Page Erase Time	-	-	3	-	ms
T_{PROG}	Program Time	-	-	40	-	μs
I_{DD1}	Read Current	-	-	0.25	-	V
I_{DD2}	Program Current	-	-	7	-	mA
I_{DD3}	Erase Current	-	-	20	-	mA

Note 1: Operation voltage comes from internal LDO.

Note 2: This table is guaranteed by design, not test in production.

8 NUC029FAE ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}	I_{DD}	-	120	mA
Maximum Current out of V_{SS}	I_{SS}	-	120	mA
Maximum Current sunk by a I/O pin	I_{IO}	-	35	mA
Maximum Current sourced by a I/O pin		-	35	mA
Maximum Current sunk by total I/O pins		-	100	mA
Maximum Current sourced by total I/O pins		-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

8.2 DC Electrical Characteristics

(V_{DD}-V_{SS} = 5.5 V, T_A = 25°C)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS			
		MIN.	TYP.	MAX.	UNIT				
Operation Voltage	V_{DD}	2.5	-	5.5	V	V_{DD} = 2.5V ~ 5.5V up to 24 MHz			
Power Ground	V_{SS} AV_{SS}	-0.3	-	-	V	-			
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} ≥ 2.5V			
Band-gap Voltage	V_{BG}	1.22	1.25	1.28	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25°C			
		1.18	1.25	1.32	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40°C ~ 105°C			
Allowed Voltage Difference for V_{DD} and AV_{DD}	V_{DD}-AV_{DD}	-0.3	0	0.3	V	-			
Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Excuted from Flash	I_{DD1}	-	9.2	-	mA	V_{DD}	HXT	HIRC	All digital modules
						5.5V	24 MHz	X	V
	I_{DD2}	-	7.0	-	mA	5.5V	24 MHz	X	X
	I_{DD3}	-	7.1	-	mA	3.3V	24 MHz	X	V
	I_{DD4}	-	5.0	-	mA	3.3V	24 MHz	X	X
Operating Current Normal Run Mode HCLK = 22.184 MHz while(1){} Excuted from Flash	I_{DD5}	-	6.1	-	mA	V_{DD}	HXT	HIRC	All digital modules
						5.5V	X	V	V
	I_{DD6}	-	3.9	-	mA	5.5V	X	V	X
	I_{DD7}	-	6.0	-	mA	3.3V	X	V	V
	I_{DD8}	-	3.9	-	mA	3.3V	X	V	X
Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Excuted from Flash	I_{DD9}	-	5.5	-	mA	V_{DD}	HXT	HIRC	All digital modules
						5.5V	12 MHz	X	V
	I_{DD10}	-	4.3	-	mA	5.5V	12 MHz	X	X
	I_{DD11}	-	3.9	-	mA	3.3V	12 MHz	X	V
	I_{DD12}	-	2.8	-	mA	3.3V	12 MHz	X	X
Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Excuted from Flash	I_{DD13}	-	3.2	-	mA	V_{DD}	HXT	HIRC	All digital modules
						5.5V	4 MHz	X	V
	I_{DD14}	-	2.8	-	mA	5.5V	4 MHz	X	X
	I_{DD15}	-	1.8	-	mA	3.3V	4 MHz	X	V
	I_{DD16}	-	1.4	-	mA	3.3V	4 MHz	X	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Excuted from Flash	I_{DD17}	-	225	-	µA	V_{DD}	HXT	HIRC	LIRC	All digital modules
						5.5V	X	X	V	V[4]
	I_{DD18}	-	225	-	µA	5.5V	X	X	V	X
	I_{DD19}	-	200	-	µA	3.3V	X	X	V	V[4]
	I_{DD20}	-	200	-	µA	3.3V	X	X	V	X
Operating Current Idle Mode HCLK = 24 MHz	I_{IDLE1}	-	7.1	-	mA	V_{DD}	HXT	HIRC	All digital modules	
						5.5V	24 MHz	X	V	
	I_{IDLE2}	-	4.9	-	mA	5.5V	24MHz	X	X	
	I_{IDLE3}	-	5.1	-	mA	3.3V	24 MHz	X	V	
	I_{IDLE4}	-	2.9	-	mA	3.3V	24 MHz	X	X	
Operating Current Idle Mode HCLK= 22.1184 MHz	I_{IDLE5}	-	4.1	-	mA	V_{DD}	HXT	HIRC	All digital modules	
						5.5V	X	V	V	
	I_{IDLE6}	-	2.0	-	mA	5.5V	X	V	X	
	I_{IDLE7}	-	4.1	-	mA	3.3V	X	V	V	
	I_{IDLE8}	-	1.9	-	mA	3.3V	X	V	X	
Operating Current Idle Mode HCLK = 12 MHz	I_{IDLE9}	-	4.4	-	mA	V_{DD}	HXT	HIRC	All digital modules	
						5.5V	12 MHz	X	V	
	I_{IDLE10}	-	3.3	-	mA	5.5V	12 MHz	X	X	
	I_{IDLE11}	-	2.9	-	mA	3.3V	12 MHz	X	V	
	I_{IDLE12}	-	1.8	-	mA	3.3V	12 MHz	X	X	
Operating Current Idle Mode HCLK = 4 MHz	I_{IDLE13}	-	2.9	-	mA	V_{DD}	HXT	HIRC	All digital modules	
						5.5V	4 MHz	X	V	
	I_{IDLE14}	-	2.5	-	mA	5.5V	4 MHz	X	X	
	I_{IDLE15}	-	1.5	-	mA	3.3V	4 MHz	X	V	
	I_{IDLE16}	-	1.1	-	mA	3.3V	4 MHz	X	X	
Operating Current Idle Mode HCLK = 10 kHz	I_{IDLE17}	-	225	-	µA	V_{DD}	HXT	HIRC	LIRC	All digital modules
						5.5V	X	X	V	V[4]
	I_{IDLE18}	-	225	-	µA	5.5V	X	X	V	X
	I_{IDLE19}	-	200	-	µA	3.3V	X	X	V	V[4]
	I_{IDLE20}	-	200	-	µA	3.3V	X	X	V	X
Standby Current	I_{PWD1}	-	10	-	µA	V_{DD} = 5.5V, All oscillators and analog blocks turned off				

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Power-down Mode (Deep Sleep Mode)	I_{PWD2}	-	9	-	μA	V_{DD} = 3.3V, All oscillators and analog blocks turned off
Logic 0 Input Current P0/1/2/3/4 (Quasi-bidirectional mode)	I_{IL}	-	-70	-75	μA	V_{DD} = 5.5V, V_{IN} = 0V
Logic 1 to 0 Transition Current P0/1/2/3/4 (Quasi-bidirectional mode)	I_{TL} [3]	-	-690	-750	μA	V_{DD} = 5.5V, V_{IN} = 2.0V
Input Leakage Current P0/1/2/3/4	I_{LK}	-1	-	+1	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD} Open-drain or input only mode
Input Low Voltage P0/1/2/3/4 (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage P0/1/2/3/4 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.3	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.3		V_{DD} =3.0V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 2.5V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.3	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.3		V_{DD} = 3.0V
Negative going threshold (Schmitt input), nRST	V_{ILS}	-0.3	-	0.2 V_{DD}	V	-
Positive going threshold (Schmitt input), nRST	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V	-
Internal nRST Pin Pull-up Resistor	R_{RST}	40		150	kΩ	V_{DD} = 2.5V ~ 5.5V
Negative going threshold (Schmitt input), P0/1/2/3/4	V_{ILS}	-0.3	-	0.3 V_{DD}	V	-
Positive going threshold (Schmitt input), P0/1/2/3/4	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V	-
Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	I_{SR11}	-300	-400	-	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-80	-	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-73	-	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current P0/1/2/3/4 (Push-pull Mode)	I_{SR21}	-20	-26	-	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-3	-5	-	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-2.5	-5	-	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current P0/1/2/3/4 (Quasi-bidirectional and Push-pull Mode)	I_{SK11}	10	15	-	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK12}	6	9	-	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK13}	5	8	-	mA	V_{DD} = 2.5V, V_S = 0.45V

Note 1: nRST pin is a Schmitt trigger input.

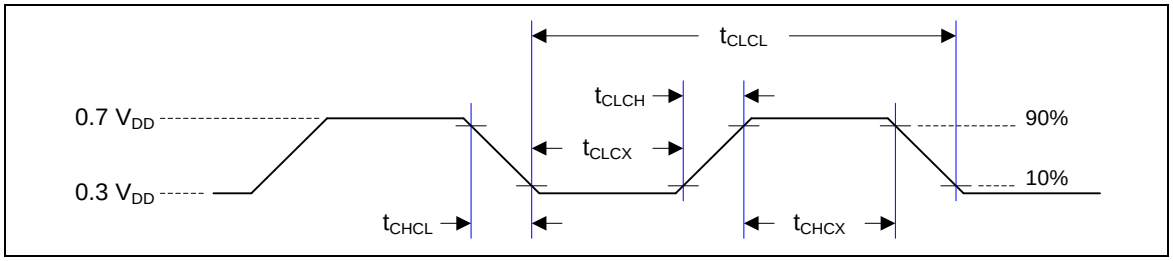
Note 2: XTAL1 is a CMOS input.

Note 3: Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD} = 5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

Note 4: Only enable modules which support 10 kHz LIRC clock source.

8.3 AC Electrical Characteristics

8.3.1 External Input Clock



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time	-	10	-	-	ns
t_{CLCX}	Clock Low Time	-	10	-	-	ns
t_{CLCH}	Clock Rise Time	-	2	-	15	ns
t_{CHCL}	Clock Fall Time	-	2	-	15	ns

8.3.2 External 4~24 MHz High Speed Crystal (HXT)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HXT}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
T_A	Temperature	-	-40	-	105	℃
I_{HXT}	Operating Current	12 MHz at V_{DD} = 5V	-	2.5	-	mA
		12 MHz at V_{DD} = 3.3V	-	1.0	-	mA
f_{HXT}	Clock Frequency	-	4	-	24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	10~20pF	10~20pF

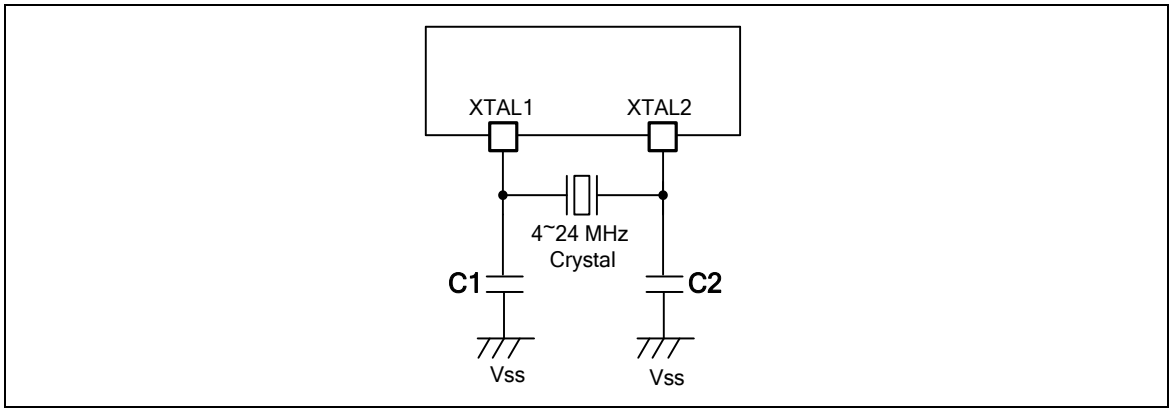
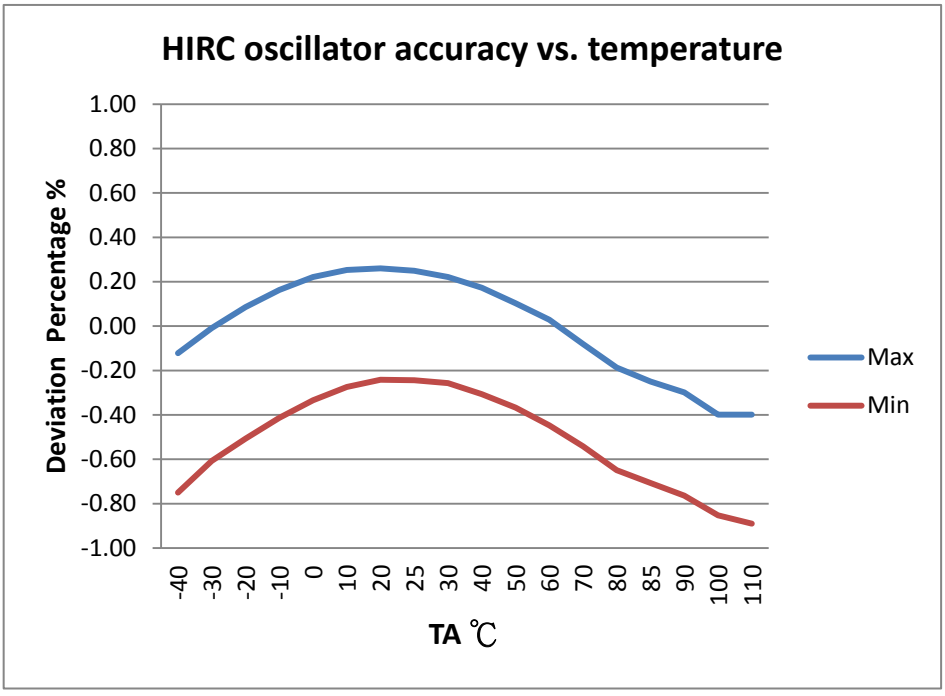


Figure 8-1 NUC029FAE Typical Crystal Application Circuit

8.3.3 Internal 22.1184 MHz High Speed RC Oscillator (HIRC)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HRC}[1]	Operation Voltage V_{DD}	-	1.62	1.8	1.98	V
f_{HRC}	Center Frequency	-	-	22.1184	-	MHz
	Calibrated Internal Oscillator Frequency	T_A = 25 ℃, V_{DD} = 5 V	-1	-	+1	%
		T_A = -40 ~ 105 ℃, V_{DD} = 2.5 V ~ 5.5 V	-3	-	+3	%
I_{HRC}	Operation Current	T_A = 25 ℃, V_{DD} = 5 V	-	700	-	uA

Note : Operation voltage comes from internal LDO.



8.3.4 Internal 10 kHz Low Speed RC Oscillator (LIRC)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{LRC}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
f_{LRC}	Center Frequency	-	-	10	-	kHz
	Calibrated Internal Oscillator Frequency	T_A = 25 ℃, V_{DD} = 2.5 V ~ 5.5 V	-10	-	+10	%
		T_A = -40 ~ 105 ℃, V_{DD} = 2.5 V ~ 5.5 V	-40	-	+40	%

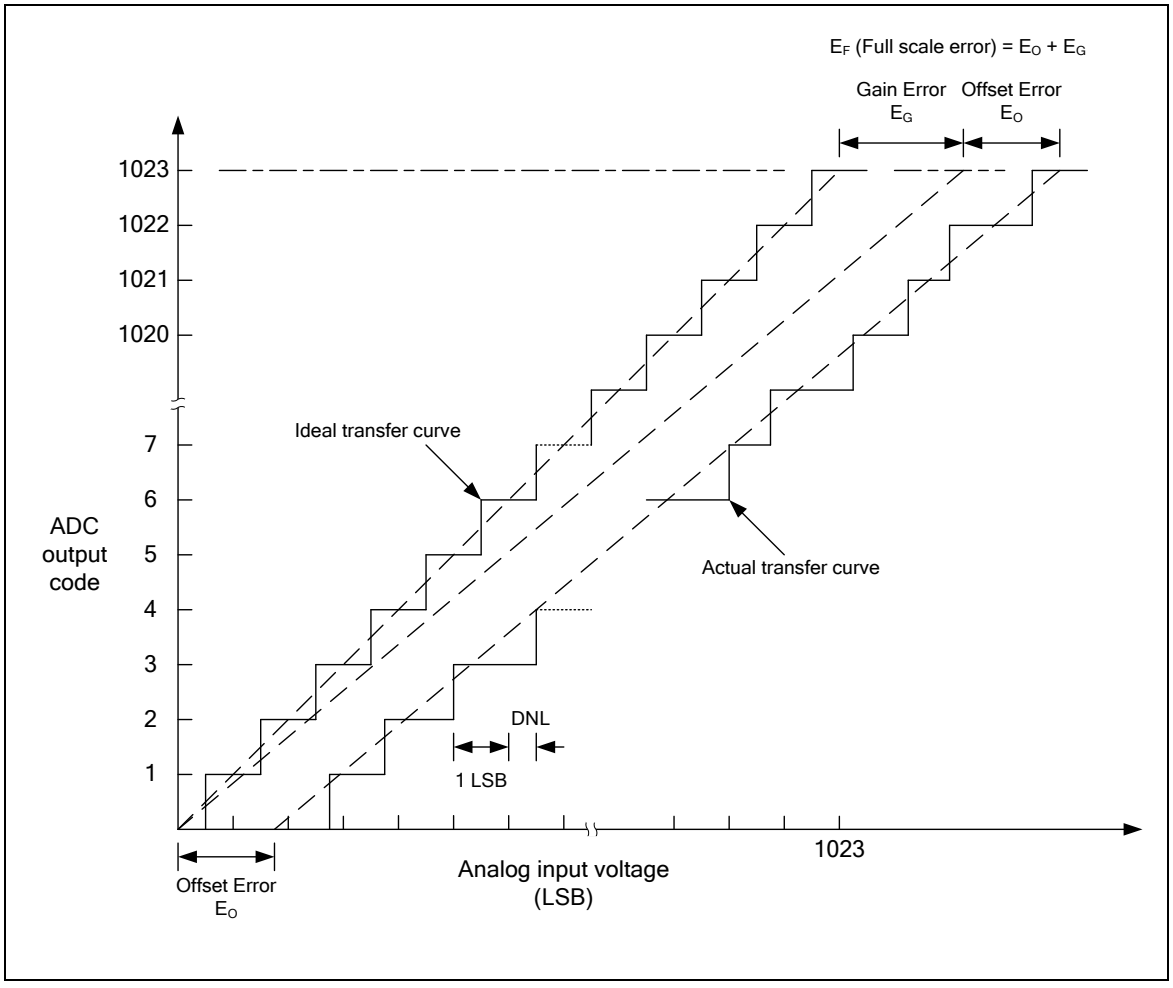
8.4 Analog Characteristics

8.4.1 10-bit SAR ADC Specification

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	10	Bit
DNL	Differential nonlinearity error	-	-1~1.5	-1~2.5	LSB
INL	Integral nonlinearity error	-	±1	±2	LSB
E_O	Offset error	-	1	2	LSB
E_G	Gain error (Transfer gain)	-	-1	-3	LSB
E_A	Absolute Error	-	3	4	LSB
-	Monotonic	Guaranteed			
F_{ADC}	ADC clock frequency (AV_{DD} = 4.5V ~ 5.5V)	-	-	4.2	MHz
	ADC clock frequency (AV_{DD} = 2.5V ~ 5.5V)	-	-	2.8	MHz
F_S	Sample rate (F_{ADC}/T_{CONV}) (AV_{DD} = 4.5V ~ 5.5V)	-	-	300	kSPS
	Sample rate (F_{ADC}/T_{CONV}) (AV_{DD} = 2.5V ~ 5.5V)	-	-	200	kSPS
T_{ACQ}	Acquisition Time (Sample Stage)	N+1[2]			1/ F_{ADC}
T_{CONV}	Total Conversion Time	N+14[2]			1/ F_{ADC}
AV_{DD}	Supply voltage	2.5	-	5.5	V
I_{DDA}	Supply current (Avg.) (AV_{DD} = 5.5V)	-	600	-	µA
V_{IN}	Analog Input voltage	0	-	AV_{DD}	V
C_{IN}	Input Capacitance	-	3.2	-	pF
R_{IN}	Input Load	-	6	-	kΩ

Note 1: ADC voltage reference is same with AV_{DD}.

Note 2: N is sampling counter, N=0, 1, 2, 4, 8, 16, 32, 4, 128, 256, 1024.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.4.2 LDO and Power Management Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	Input Voltage V_{DD}	-	2.5		5.5	V
V_{LDO}	Output Voltage	-	1.62	1.8	1.98	V
T_A	Operating Temperature	-	-40	25	105	℃

Note: It is recommended that a 0.1 uF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

8.4.3 Low Voltage Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Input Voltage AV_{DD}	-	2.5	-	5.5	V
T_A	Operating Temperature	-	-40	25	105	℃
I_{LVR}	Capacitor	AV_{DD} = 5.5 V	-	1	5	μF
V_{LVR}	Threshold Voltage	T_A = 25 ℃	1.90	2.00	2.10	V
		T_A = -40 ℃	1.70	1.90	2.05	V
		T_A = 105 ℃	2.00	2.20	2.45	V

8.4.4 Brown-out Detector Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Input Voltage AV_{DD}	-	2.5	-	5.5	V
T_A	Operating Temperature	-	-40	25	105	℃
I_{BOD}	Quiescent Current	AV_{DD} = 5.5 V	-	-	140	μA
V_{BOD}	Brown-out Voltage (Falling edge)	BOD_VL[1:0]=11	4.2	4.38	4.55	V
		BOD_VL [1:0]=10	3.5	3.68	3.85	V
		BOD_VL [1:0]=01	2.5	2.68	2.85	V
		BOD_VL [1:0]=00	2.0	2.18	2.35	V
V_{BOD}	Brown-out Voltage (Rising edge)	BOD_VL[1:0]=11	4.3	4.52	4.75	V
		BOD_VL [1:0]=10	3.5	3.8	4.05	V
		BOD_VL [1:0]=01	2.5	2.77	3.05	V
		BOD_VL [1:0]=00	2.0	2.25	2.55	V

8.4.5 Power-on Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_A	Operating Temperature	-	-40	25	85	℃
V_{POR}	Reset Voltage	V+	1.6	2	2.4	V
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	-	100	mV
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	-	0.025	-	-	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	-	0.5	-	-	ms

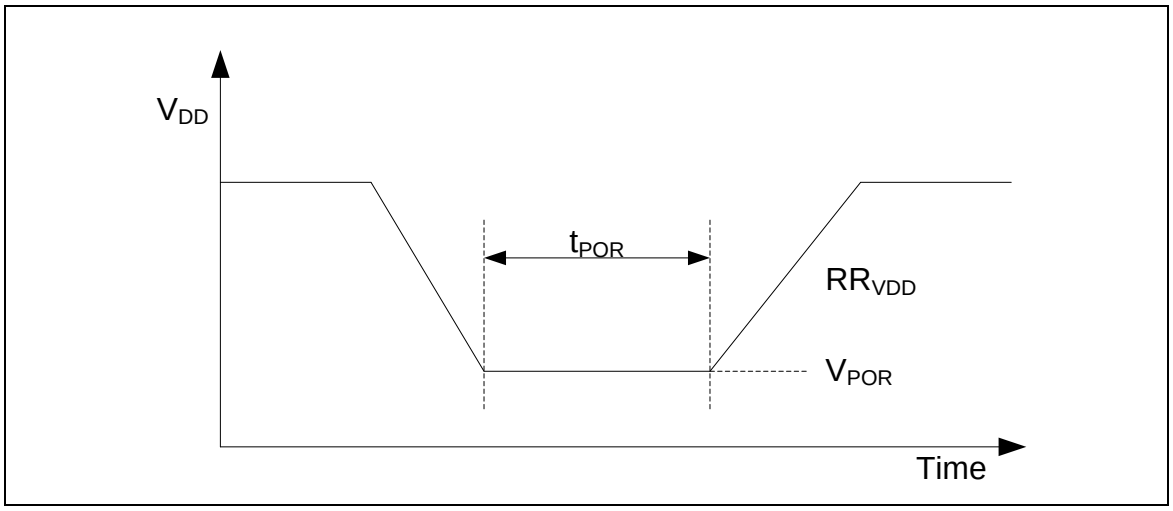


Figure 8-2 NUC029xAN Power-up Ramp Condition

8.4.6 Comparator Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CMP}	Operation Voltage AV_{DD}	-	2.5	-	5.5	V
T_A	Operation Temperature	-	-40	25	105	℃
I_{CMP}	Operation Current	AV_{DD} = 5 V	-	40	80	μA
V_{OFF}	Input Offset Voltage	-	-	10	20	mV
V_{SW}	Output Swing	-	0.1	-	AV_{DD}-0.1	V
V_{COM}	Input Common Mode Range	-	0.1	-	AV_{DD}-0.1	V
-	DC Gain	-	40	70	-	dB
T_{PGD}	Propagation Delay	V_{COM} = 1.2 V, V_{DIFF} = 0.1 V	-	200	-	ns
V_{HYS}	Hysteresis	V_{COM} = 1.2 V	-	±30	±60	mV
T_{STB}	Stable Time	-	-	-	1	μs

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{FLA}[1]	Operation Voltage	-	1.62	1.8	1.98	V
N_{ENDUR}	Endurance	-	20,000	-	-	cycles[2]
T_{RET}	Data Retention	T_A = 25℃	10	-	-	year
T_{ERASE}	Page Erase Time	-	-	3	-	ms
T_{PROG}	Program Time	-	-	40	-	μs
I_{DD1}	Read Current	-	-	0.25	-	V
I_{DD2}	Program Current	-	-	7	-	mA
I_{DD3}	Erase Current	-	-	20	-	mA

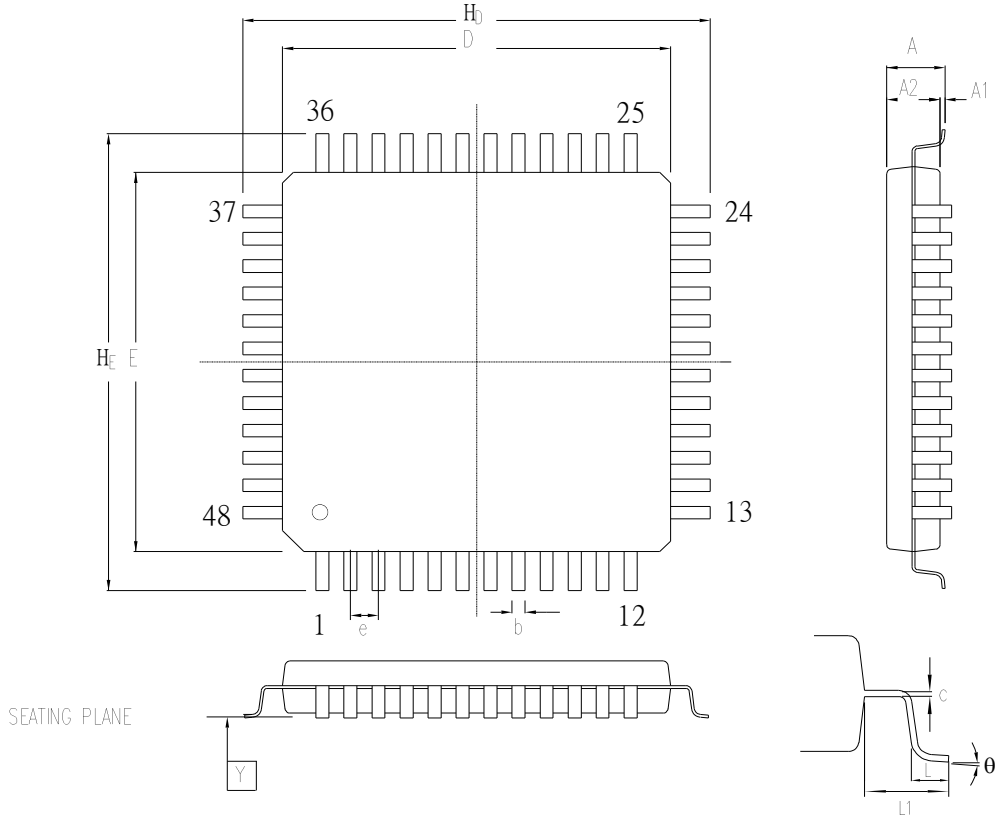
Note 1: Operation voltage comes from internal LDO.

Note 2: Number of program/erase cycles.

Note 3: This table is guaranteed by design, not test in production.

9 PACKAGE DIMENSIONS

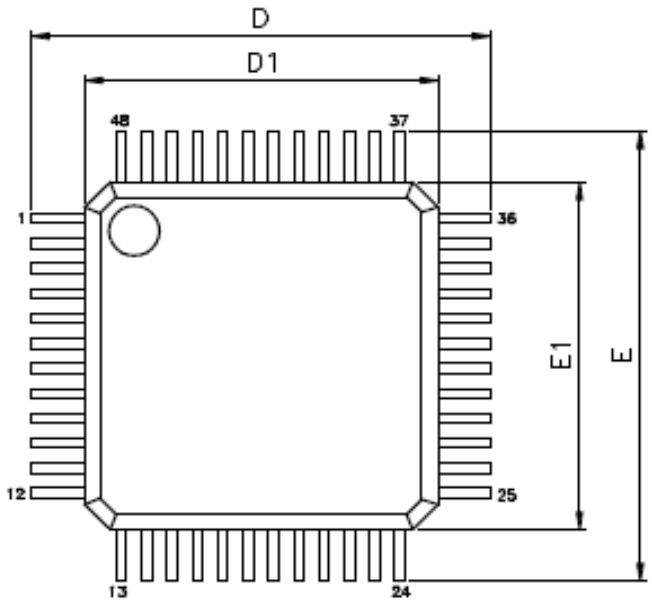
9.1 48-pin LQFP (7x7x1.4 mm)

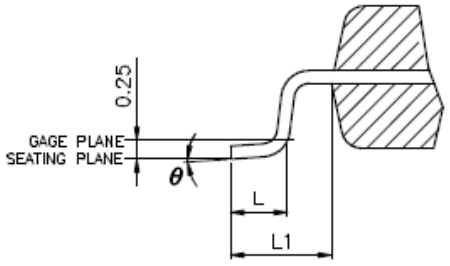


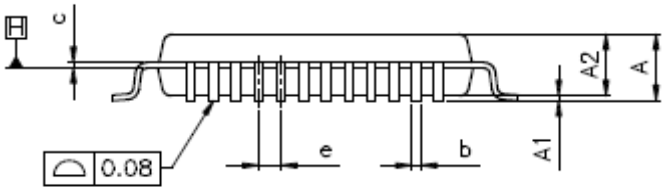
Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

9.2 48-pin QFN (7x7x0.8 mm)



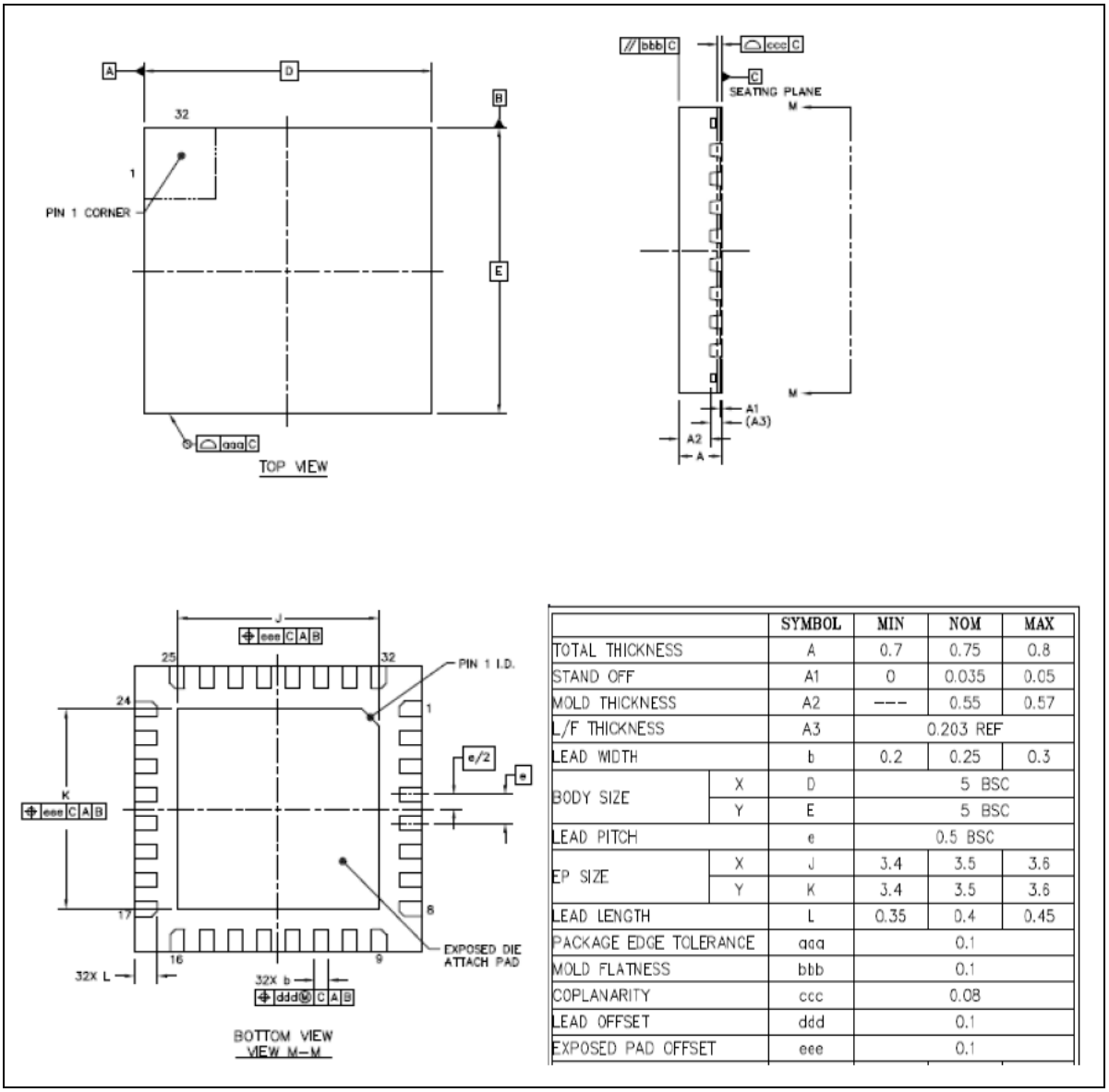




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

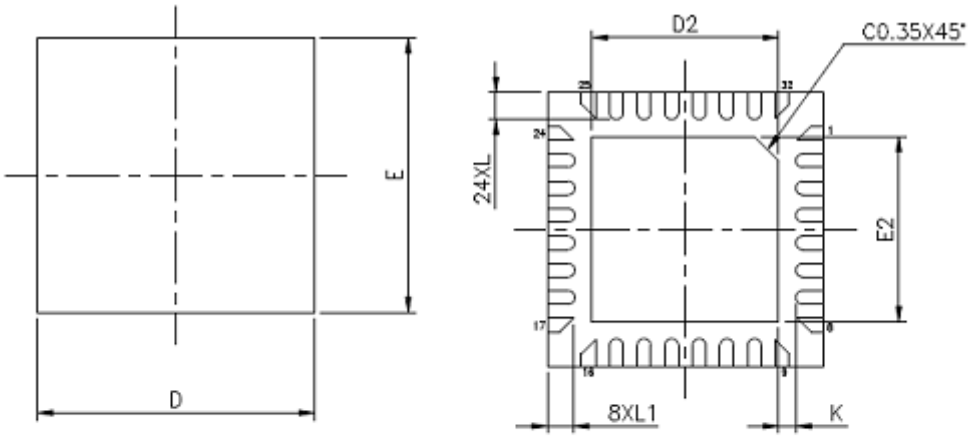
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

9.3 33-pin QFN (5x5x0.75 mm)

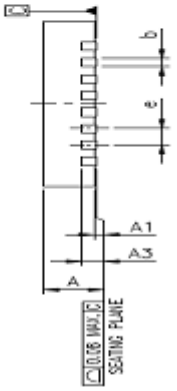


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

9.4 33-pin QFN (4x4x0.75 mm)

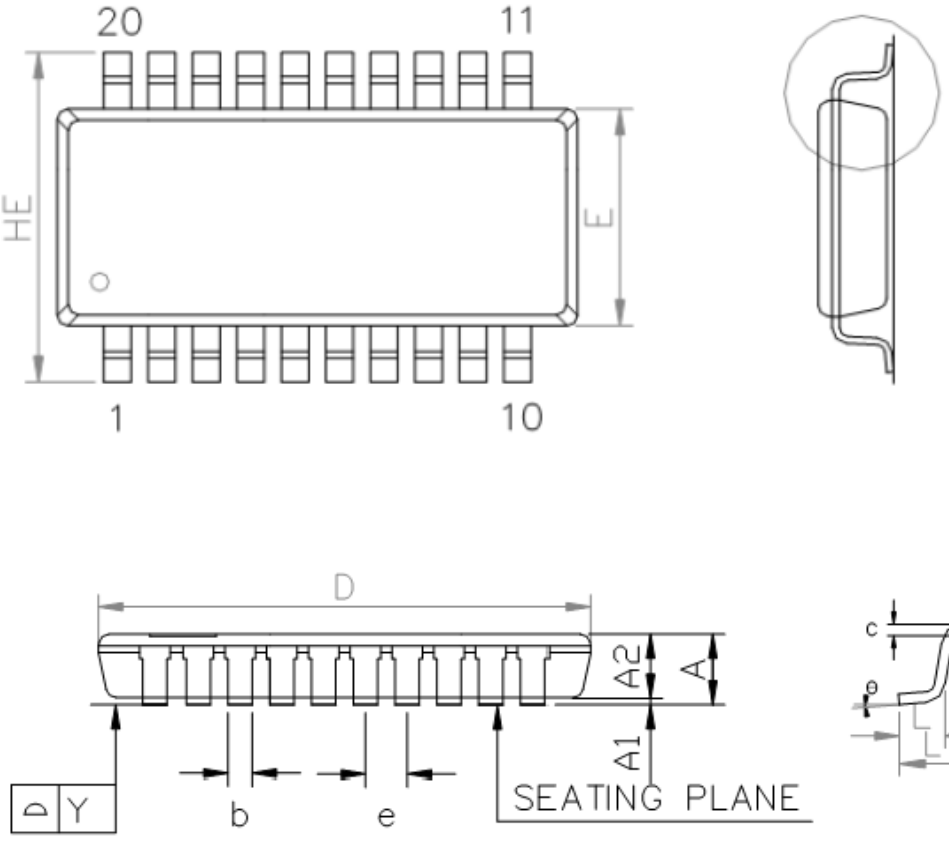


SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.35	0.40	0.45
K	0.20	—	—



Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.8
E2		2.6	2.7	2.8

9.5 20-pin TSSOP (6.5x4.4x1.2 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

10 REVISION HISTORY

Date	Revision	Description
2014.05.19	1.00	1. Preliminary version.
2014.08.26	1.01	1. Modified Figure 4-1 NuMicro® NUC029 Series Selection Code.
2015.05.18	1.02	1. Changed the order of Chapter 5 FUNCTIONAL DESCRIPTION. 2. Fixed typos and obscure description. 3. Added Chapter 5.2.5 Whole System Memory Mapping. 4. Fixed the description about Frequency Divider Output of NUC029xAN series in Chapter 5.3.4. 5. Added clock switching note in Chapter 5.3 and 5.4. 6. Removed description about ACMP output inverse function available on NUC029xAN series. 7. Modified NUC029xDN LVR and BOD specification. 8. Updated 33-pin QFN (4x4) package dimension in Chapter 9.4.
2017.06.23	1.03	1. Added new part number NUC029ZAN.
2017.12.11	1.04	1. Added new part number NUC029NAN.

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