X9318

Digitally Controlled Potentiometer (XDCP™)

FN8184
Rev 1.00
September 14, 2005

FEATURES

- **Solid-state potentiometer**
- **3-wire serial interface**
- **Terminal voltage, 0 to +8V**
- **100 wiper tap points**
  - **—Wiper position stored in nonvolatile memory and recalled on power-up**
- **99 resistive elements**
  - **—Temperature compensated**
  - **—End to end resistance range ± 20%**
- **Low power CMOS**
  - **—V_{CC} = 5V**
  - **—Active current, 3mA max.**
  - **—Standby current, 1mA max.**
- **High reliability**
  - **—Endurance, 100,000 data changes per bit**
  - **—Register data retention, 100 years**
- **R_{TOTAL} value = 10kΩ**
- **Packages**
  - **—8 Ld SOIC and DIP**
- **Pb-free plus anneal available (RoHS compliant)**

APPLICATIONS

- **LCD bias control**
- **DC bias adjustment**
- **Gain and offset trim**
- **Laser diode bias control**
- **Voltage regulator output control**

DESCRIPTION

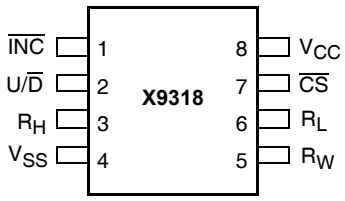
The Intersil X9318 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

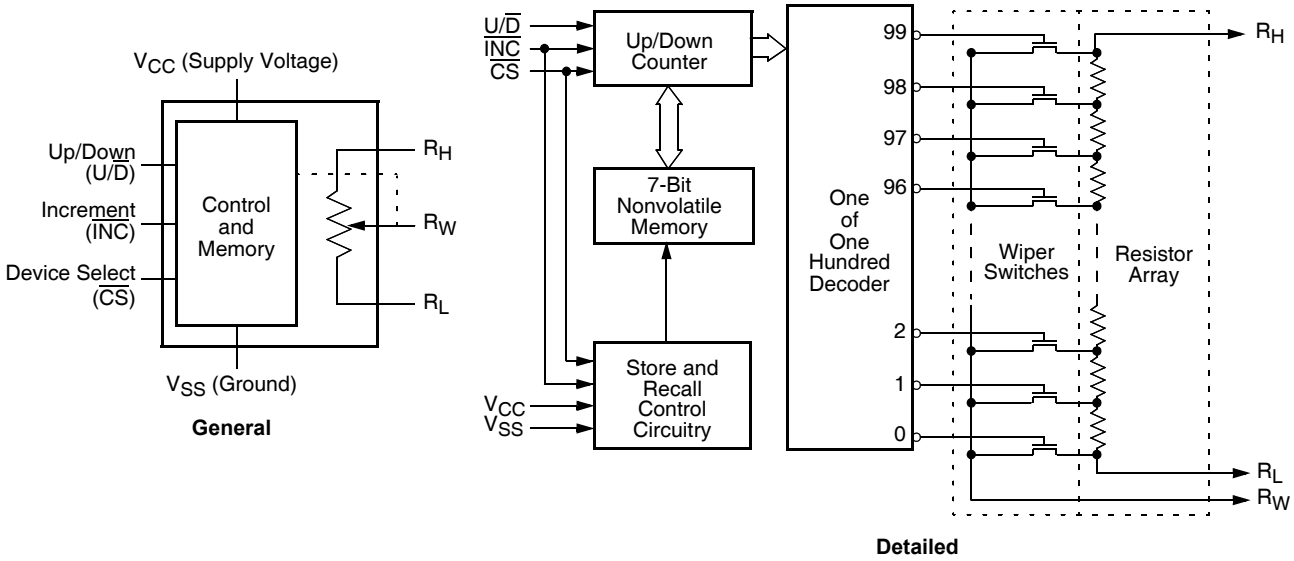
The device can be used as a three-terminal potentiometer for voltage control or as a two-terminal variable resistor for current control in a wide variety of applications.

PIN CONFIGURATION

DIP/SOIC



BLOCK DIAGRAM



Ordering Information

PART NUMBER	PART MARKING	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE
X9318WP8	X9318WP	10	0 to 70	8 Ld PDIP
X9318WP8I	X9318WP I		-40 to 85	8 Ld PDIP
X9318WS8*	X9318W		0 to 70	8 Ld SOIC (150 mil)
X9318WS8Z* (Note)	X9318W Z		0 to 70	8 Ld SOIC (150 mil) (Pb-free)
X9318WS8I*	X9318W I		-40 to 85	8 Ld SOIC (150 mil)
X9318WS8IZ* (Note)	X9318W Z I		-40 to 85	8 Ld SOIC (150 mil) (Pb-free)

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PIN DESCRIPTIONS

DIP/SOIC	Symbol	Brief Description
1	$\overline{INC}$	**Increment**. Toggling $\overline{INC}$ while $\overline{CS}$ is low moves the wiper either up or down.
2	U/$\overline{D}$	**Up/Down**. The U/$\overline{D}$ input controls the direction of the wiper movement.
3	R_H	The high terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
4	V_{SS}	**Ground.**
5	R_W	The wiper terminal is equivalent to the movable terminal of a mechanical potentiometer.
6	R_L	The low terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
7	$\overline{CS}$	**Chip Select**. The device is selected when the $\overline{CS}$ input is LOW, and de-selected when $\overline{CS}$ is high.
8	V_{CC}	**Supply Voltage.**

ABSOLUTE MAXIMUM RATINGS

Junction Temperature under bias..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with respect to V_{SS} ..... -1V to +7V
R_H, R_W, R_L to ground.....+10V
Lead temperature (soldering 10s) ..... 300°C
I_W (10s) .....±6mA

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POTENTIOMETER CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = Full Operating Temperature Range unless otherwise stated)

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.(4)	Max.	Unit	
	End to end resistance tolerance	-20		+20	%	See ordering information for values
V_{RH}/R_L	R_H/R_L terminal voltage	V_{SS}		8	V	V_{SS} = 0V
	Power rating			25	mW	
R_W	Wiper resistance		40	200	Ω	I_W = 1mA
I_W	Wiper current(5)	-3.0		+3.0	mA	See test circuit
	Noise(7)		-120		dBV	Ref: 1kHz
	Resolution		1		%	
	Absolute linearity(1)	-1		+1	MI(3)	V(RH) = 8V, V(RL) = 0V
	Relative linearity(2)	-0.2		+0.2	MI(3)	
	R_{TOTAL} temperature coefficient(5)		±300		ppm/°C	
	Ratiometric temperature coefficient(5),(6)	-20		+20	ppm/°C	
$C_H/C_L/C_W$(5)	Potentiometer capacitances		10/10/25		pF	See equivalent circuit
V_{CC}	Supply Voltage	4.5		5.5	V	

D.C. OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = Full Operating Temperature Range unless otherwise stated)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	V_{CC} active current (Increment)		1	3	mA	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V @ min. t_{CYC} R_L, R_H, R_W not connected
I_{SB}	Standby supply current		300	1000	µA	$\overline{CS}$ ≥ 2.4V, U/$\overline{D}$ and $\overline{INC}$ = 0.4V R_L, R_H, R_W not connected
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	-10		+10	µA	V_{IN} = V_{SS} to V_{CC}
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage	2		V_{CC} + 1	V	
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage	-1		0.8	V	
C_{IN}(5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance			10	pF	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz

ENDURANCE AND DATA RETENTION

(V_{CC} = 5V ± 10%, T_A = Full Operating Temperature Range)

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $[V(R_{W(n)(actual)}) - V(R_{W(n)(expected)})]/MI$ $V(R_{W(n)(expected)}) = n(V(R_H) - V(R_L))/99 + V(R_L)$, with n from 0 to 99.

(2) Relative linearity is a measure of the error in step size between taps = $[V(R_{W(n+1)}) - (V(R_{W(n)}) - MI)]/MI$

(3) 1 MI = Minimum Increment = $[V(R_H) - V(R_L)]/99$.

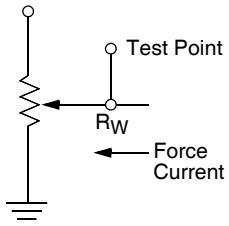
(4) Typical values are for T_A = 25°C and nominal supply voltage.

(5) This parameter is not 100% tested.

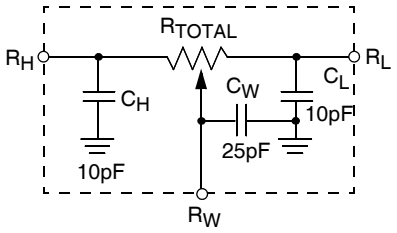
(6) Ratiometric temperature coefficient = $(V(R_W)_{T1(n)} - V(R_W)_{T2(n)})/[V(R_W)_{T1(n)}(T1 - T2) \times 10^6]$, with T1 & T2 being 2 temperatures, and n from 0 to 99.

(7) Measured with wiper at tap position 31, R_L grounded, using test circuit.

Test Circuit



Equivalent Circuit



A.C. CONDITIONS OF TEST

Input pulse levels	0.8V to 2.0V
Input rise and fall times	10ns
Input reference levels	1.4V

A.C. OPERATING CHARACTERISTICS

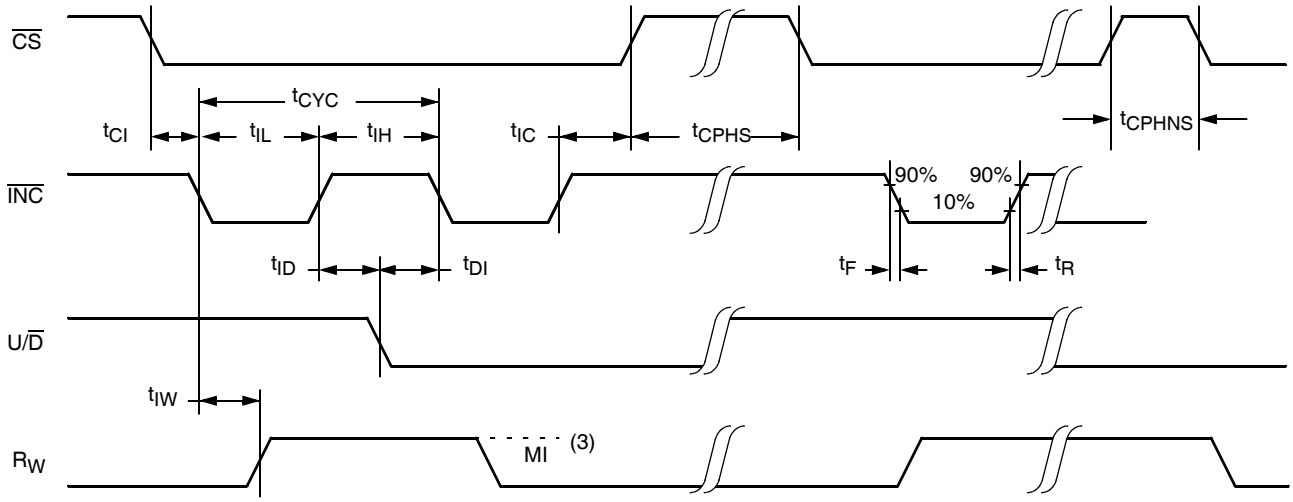
(V_{CC} = 5V ± 10%, T_A = Full Operating Temperature Range unless otherwise stated)

Symbol	Parameter	Limits			Unit
		Min.	Typ.(4)	Max.	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID}(5)	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI}(5)	U/$\overline{D}$ to $\overline{INC}$ setup	1			µs
t_{IL}	$\overline{INC}$ LOW period	1			µs
t_{IH}	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	1			µs
t_{CPHS}	$\overline{CS}$ deselect time (STORE)	20			ms
t_{CPHNS}(5)	$\overline{CS}$ deselect time (NO STORE)	1			µs
t_{IW}	$\overline{INC}$ to R_W change		100	500	µs
t_{CYC}	$\overline{INC}$ cycle time	4			µs
t_R, t_F(5)	$\overline{INC}$ input rise and fall time			500	µs
t_{PU}(5)	Power-up to wiper stable			500	µs
t_R V_{CC}(5)	V_{CC} power-up rate	0.2		50	V/ms

POWER-UP AND DOWN REQUIREMENTS

The recommended power-up sequence is to apply V_{CC}/V_{SS} first, then the potentiometer voltages. During power-up, the data sheet parameters for the DCP do not fully apply until 1 millisecond after V_{CC} reaches its final value. The V_{CC} ramp spec is always in effect. In order to prevent unwanted tap position changes, or an inadvertant store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on powerup.

A.C. TIMING



PIN DESCRIPTIONS

R_H and R_L

The high (R_H) and low (R_L) terminals of the X9318 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

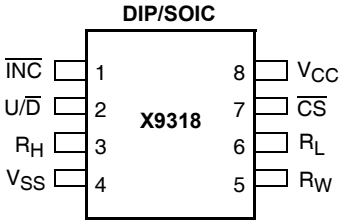
Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9318 will be placed in the low power standby mode until the device is selected once again.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
R_H	High terminal
R_W	Wiper terminal
R_L	Low terminal
V_{SS}	Ground
V_{CC}	Supply voltage
U/$\overline{D}$	Up/Down control input
$\overline{INC}$	Increment control input
$\overline{CS}$	Chip select control input

PRINCIPLES OF OPERATION

There are three sections of the X9318: the control section, the nonvolatile memory, and the resistor array. The control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. Electronic switches at either end of the array and between each resistor provide an electrical connection to the wiper pin, R_W.

The wiper acts like its mechanical equivalent and does not move beyond the first or last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

INSTRUCTIONS AND PROGRAMMING

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit counter. The output of this counter is decoded to select one of one hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9318, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a powerup/down cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

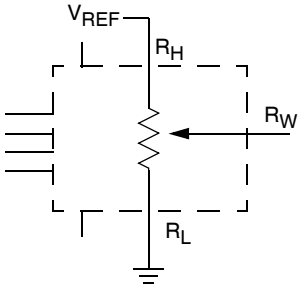
MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L		H	Wiper up
L		L	Wiper down
	H	X	Store wiper position to nonvolatile memory
H	X	X	Standby
	L	X	No store, return to standby
	L	H	Wiper Up (not recommended)
	L	L	Wiper Down (not recommended)

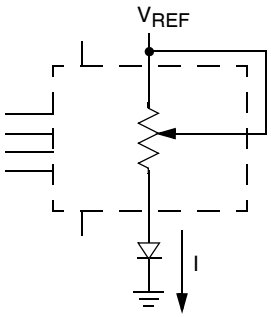
APPLICATIONS INFORMATION

Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



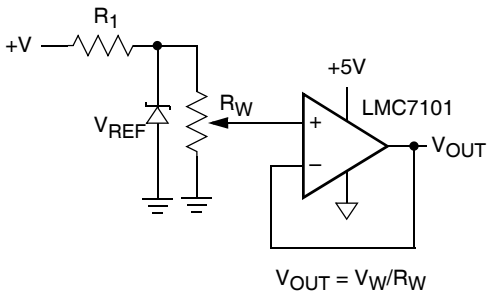
Three terminal potentiometer;
variable voltage divider



Two terminal variable resistor;
variable current

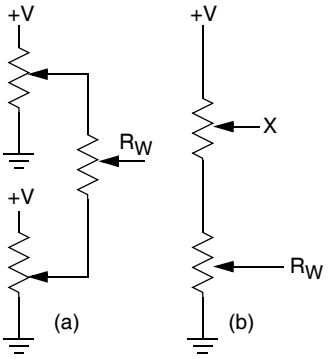
Basic Circuits

Buffered Reference Voltage

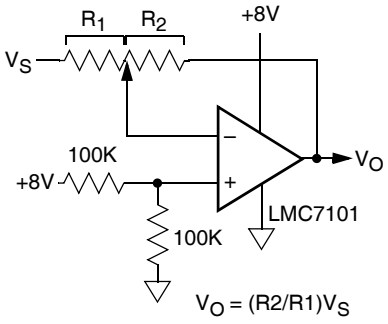


$V_{OUT} = V_W/R_W$

Cascading Techniques

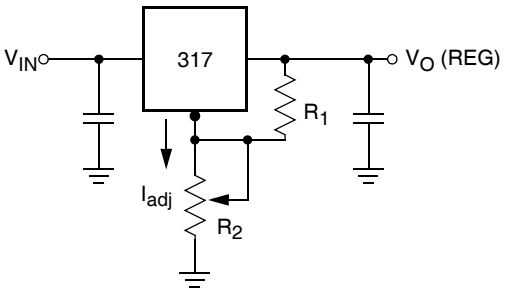


Single Supply Inverting Amplifier



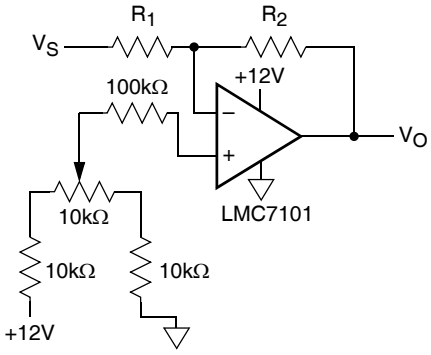
$V_O = (R2/R1)V_S$

Voltage Regulator

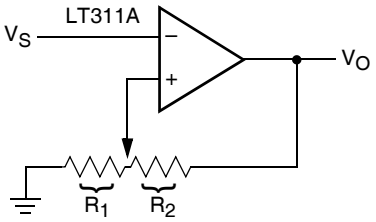


$V_O\,(REG) = 1.25V\,(1+R_2/R_1)+I_{adj}\,R_2$

Offset Voltage Adjustment



Comparator with Hysteresis

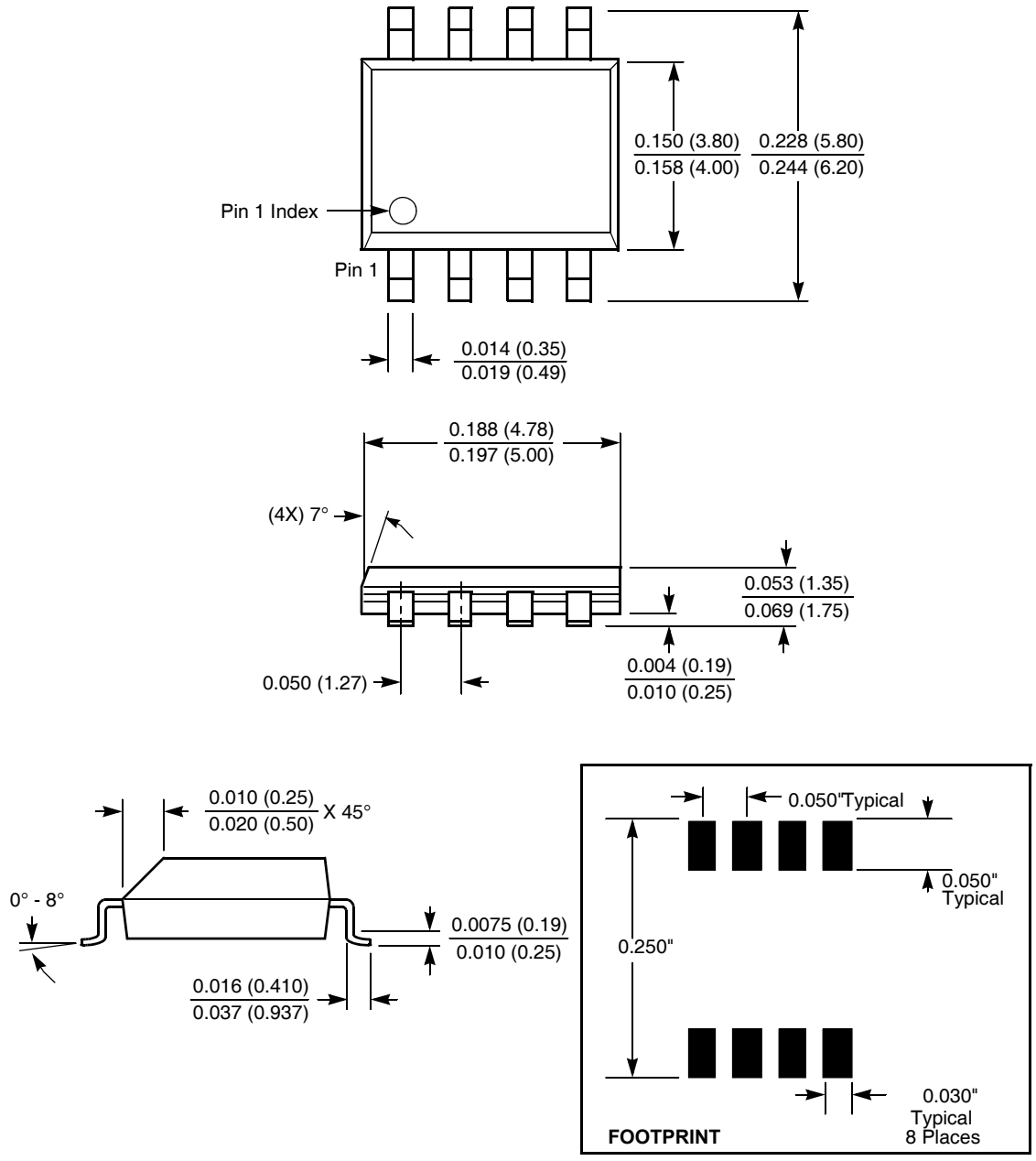


$V_{UL} = \{R_1/(R_1+R_2)\}\,V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\,V_O(min)$

(for additional circuits see AN115)

PACKAGING INFORMATION

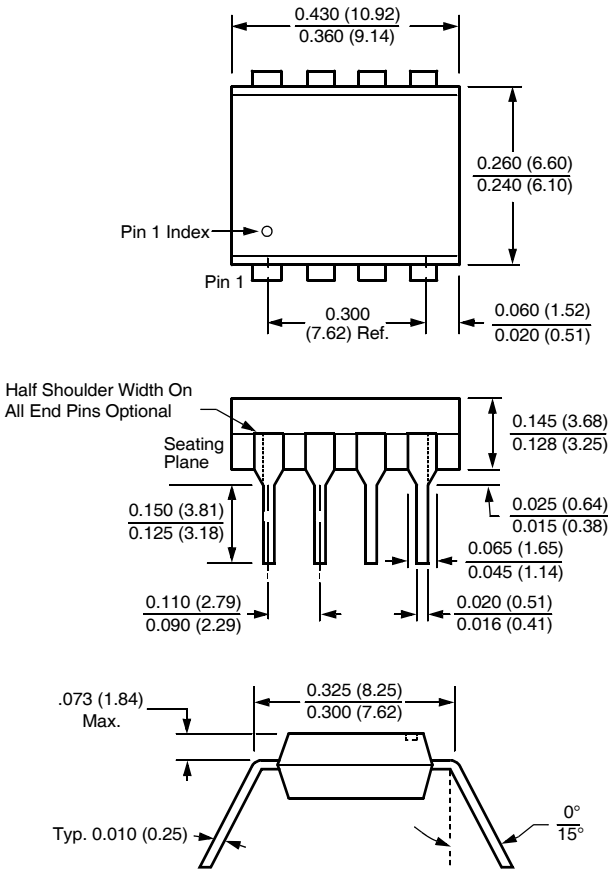
8-Lead Plastic Small Outline Package, Type S (8-lead SOIC)



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-Lead Plastic, DIP, Package Code P8



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

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