

### OVERVIEW

The SM5813AP/APT is a high-fidelity eight-times oversampling digital filter LSI for digital audio system, using the molibdenum gate C-MOS process developed solely by NPC.

This LSI has a two-channel FIR filter and three types of output modes (16bit/18bit/20bit). Since it has four kinds of system clocks --- 512fs/256fs/384fs/192fs, it can be used for not only CD players but also other audio systems.

### FEATURES

#### FILTER CHARACTERISTICS

| ITEMS                       | CHARACTERISTICS               |
|-----------------------------|-------------------------------|
| Pass band .....             | 0 to 0.4535fs                 |
| Stop band .....             | 0.5465fs to 7.4535fs          |
| Pass band ripple .....      | Within $\pm 0.00005\text{dB}$ |
| Stop band attenuation ..... | More than 110dB               |

— Linear phase (There is no group delay distortion.)

#### FILTER STRUCTURE

- Eight-times oversampling
- Two-channel filters
- Cascaded three-stage linear phase FIR filters (153+29+17 order)
- $20 \times 22$  bit multiplier
- 25bit accumulator
- Overflow limiter
- Crystal oscillation circuit
- Power supply voltage:  $5\text{V} \pm 0.5\text{V}$
- Molybdenam gate C-MOS process

#### Free running mode (Jitter-free)

#### INPUT/OUTPUT

- 16 bit serial data input  
(2's complement code, MSB first)
- 16/18/20bit serial data output  
(2's complement/Complemented offset binary, MSB first)

#### SYSTEM CLOCK

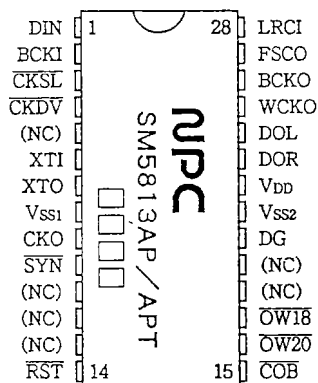
(512fs/256fs/384fs/192fs)

#### PACKAGE

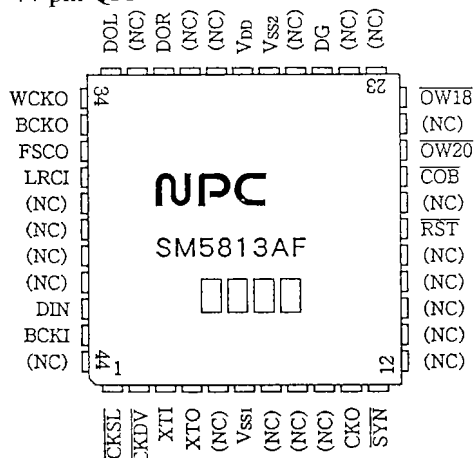
28-pin DIP, 44-pin QFP

### PIN OUT (TOP VIEW)

#### 28-pin DIP



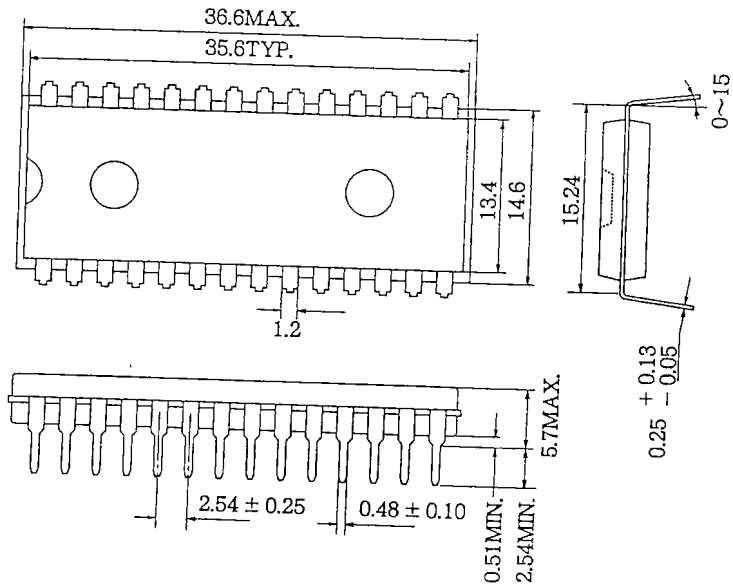
#### 44-pin QFP



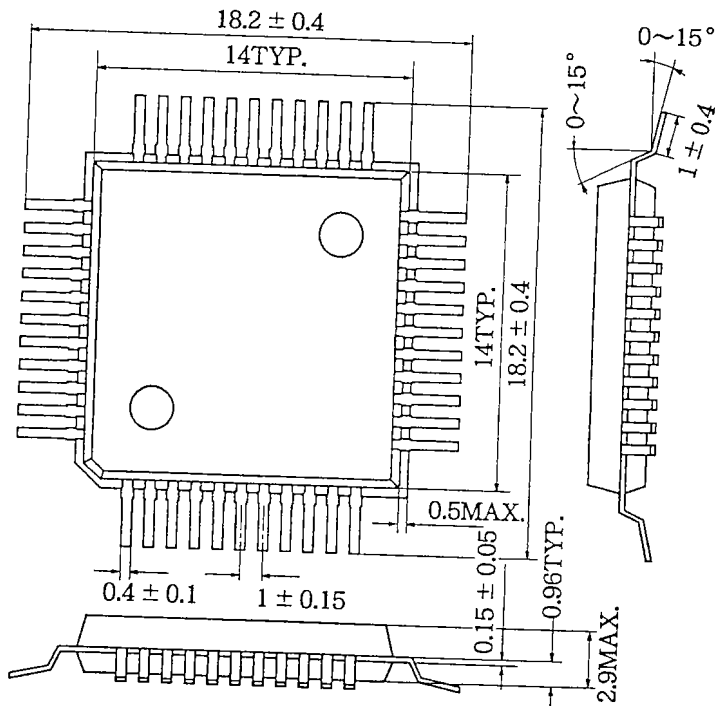
# ■ PACKAGE DIMENSION

(UNIT: mm)

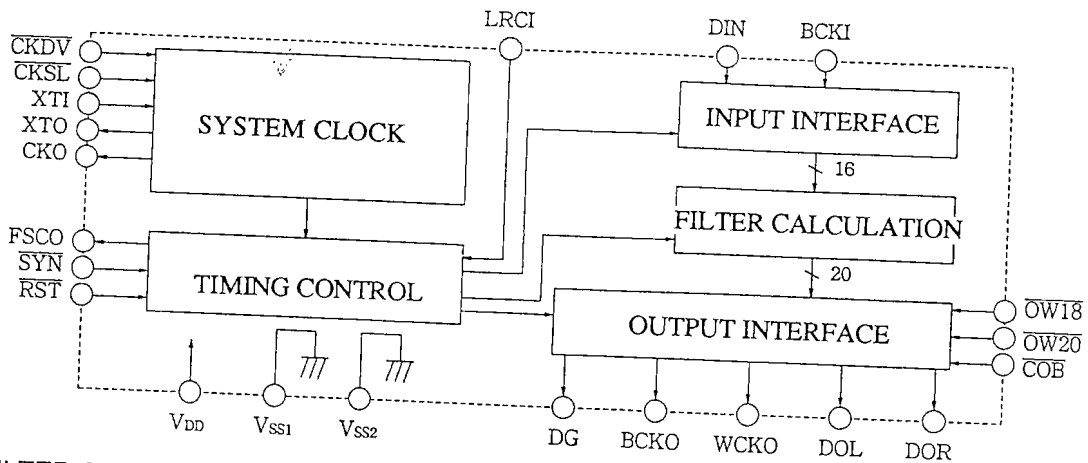
## • 28-pin DIP



## • 44-pin QFP



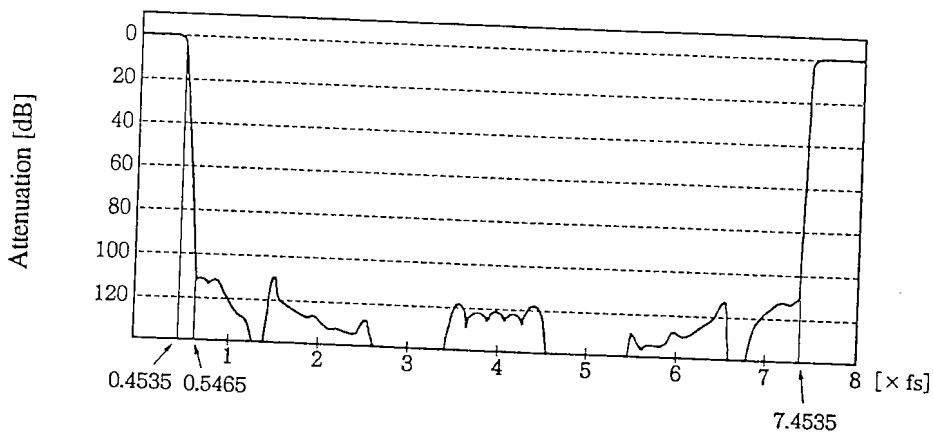
## ■ BLOCK DIAGRAM



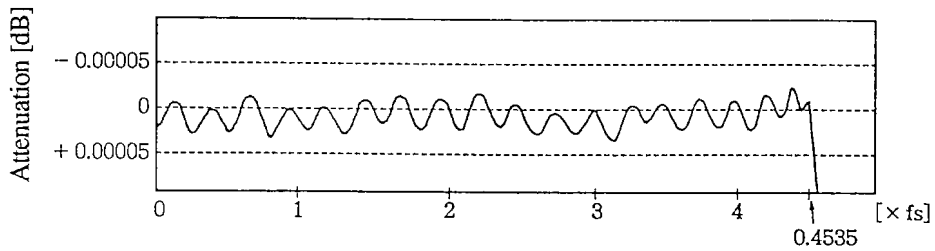
## ■ FILTER CHARACTERISTICS (THEORITICAL VALUE)

| ITEMS                 | CHARACTERISTICS       |
|-----------------------|-----------------------|
| Pass band             | 0 ~ 0.4535fs          |
| Stop band             | 0.5465fs ~ 7.4535fs   |
| Pass band ripple      | Within $\pm 0.00005B$ |
| Stop band attenuation | More than 110dB       |
| Group delay time      | Constant              |

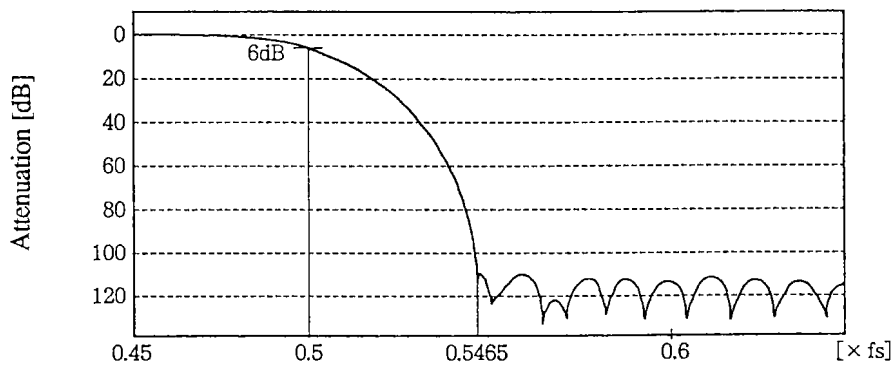
## STOP BAND ATTENUATION



## PASS BAND RIPPLE



## THE DOMAIN BETWEEN PASS BAND AND STOP BAND



# PIN DESCRIPTION

| NO. |     | NAME             | I/O* | DESCRIPTION                                                                           |
|-----|-----|------------------|------|---------------------------------------------------------------------------------------|
| DIP | QFP |                  |      |                                                                                       |
| 1   | 42  | DIN              | I    | Serial data input                                                                     |
| 2   | 43  | BCKI             | I    | Timing clock for serial input data                                                    |
| 3   | 1   | CKSL             | I    | Selecting system clock *2                                                             |
| 4   | 2   | CKDV             | I    |                                                                                       |
| 6   | 3   | XTI              | I    | Input for oscillator or external clock input (System clock)                           |
| 7   | 4   | XTO              | O    | Output for oscillator, No connect when using external clock                           |
| 8   | 6   | V <sub>ss1</sub> | -    | Ground 1                                                                              |
| 9   | 10  | CKO              | O    | Clock output (Same frequency as XTI input clock)                                      |
| 10  | 11  | SYN              | I    | H: Free running mode L: Forced synchronizing mode                                     |
| 14  | 17  | RST              | I    | H: Normal operation L: System reset                                                   |
| 15  | 19  | COB              | I    | Selecting output data format<br>H: 2's complement L: Complemented offset binary (COB) |
| 16  | 20  | OW20             | I    | Selecting number of output data bits *3                                               |
| 17  | 22  | OW18             | I    |                                                                                       |
| 20  | 25  | DG               | O    | Deglintch control clock                                                               |
| 21  | 27  | V <sub>ss2</sub> | -    | Ground 2                                                                              |
| 22  | 28  | VDD              | -    | Supply voltage (+5V)                                                                  |
| 23  | 31  | DOR              | O    | Rch serial data output (8fs rate)                                                     |
| 24  | 33  | DOL              | O    | Lch serial data output (8fs rate)                                                     |
| 25  | 34  | WCKO             | O    | Output timing control (Word clock)                                                    |
| 26  | 35  | BCKO             | O    | Output timing control for serial data (Bit clock)                                     |
| 27  | 36  | FSCO             | O    | Internal timing clock (fs rate)                                                       |
| 28  | 37  | LRCI             | I    | Multiplex clock for Lch/Rch input data (fs rate): H: Lch L: Rch                       |

- \*1) I: Input terminal  
Ip: Input terminal with pull-up resistance  
O: Output terminal

\*2)

| CKSL | CKDV | System clock (Input to XTI) |
|------|------|-----------------------------|
| H    | H    | 192fs                       |
| H    | L    | 384fs                       |
| L    | H    | 256fs                       |
| L    | L    | 512fs                       |

\*3)

| OW18 | OW20 | The number of output data bit |
|------|------|-------------------------------|
| H    | H    | 16 bit                        |
| L    | H    | 18 bit                        |
| H    | L    | 20 bit                        |

## ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub>=0V)

| ITEM                  | SYMBOL           | LIMITS                        | UNIT |
|-----------------------|------------------|-------------------------------|------|
| SUPPLY VOLTAGE        | V <sub>DD</sub>  | -0.3 to 7.0                   | V    |
| INPUT VOLTAGE         | V <sub>IN</sub>  | -0.3 to V <sub>DD</sub> + 0.3 | V    |
| STORAGE TEMPERATURE   | T <sub>STG</sub> | -40 to 125                    | °C   |
| POWER DISSIPATION     | P <sub>W</sub>   | 250                           | mW   |
| SOLDERING TEMPERATURE | T <sub>SLD</sub> | 255                           | °C   |
| SOLDERING TIME        | T <sub>SLD</sub> | 10                            | Sec  |

## ■ RECOMMENDATORY OPERATING CONDITIONS

(V<sub>SS</sub>=0V)

| ITEM                  | SYMBOL            | LIMITS       | UNIT |
|-----------------------|-------------------|--------------|------|
| SUPPLY VOLTAGE        | V <sub>DD</sub>   | 4.75 to 5.25 | V    |
| OPERATING TEMPERATURE | T <sub>OPRD</sub> | -20 to 70    | °C   |

## ■ ELECTRIC CHARACTERISTICS

- DC CHARACTERISTICS (T<sub>a</sub> = -20 to 70°C, V<sub>DD</sub> = 4.75 to 5.25V, V<sub>SS</sub> = 0V)

| ITEM                   | TER-MINAL       | SYMBOL           | CONDITION                                | MIN                | TYP | MAX                | UNIT |
|------------------------|-----------------|------------------|------------------------------------------|--------------------|-----|--------------------|------|
| CURRENT CONSUMPTION    | V <sub>DD</sub> | I <sub>DD</sub>  | V <sub>DD</sub> =5V, f <sub>sys</sub> *3 |                    |     | 45                 | mA   |
| INPUT VOLTAGE (1)      | XTI             | V <sub>IH1</sub> |                                          | 0.7V <sub>DD</sub> |     |                    | V    |
|                        |                 | V <sub>IL1</sub> |                                          |                    |     | 0.3V <sub>DD</sub> | V    |
| INPUT VOLTAGE (2)      | (*1)            | V <sub>IH2</sub> |                                          | 2.4                |     |                    | V    |
|                        |                 | V <sub>IL2</sub> |                                          |                    |     | 0.5                | V    |
| OUTPUT VOLTAGE         | (*2)            | V <sub>OH</sub>  | I <sub>OH</sub> = -0.4mA                 | 2.5                |     |                    | V    |
|                        |                 | V <sub>OL</sub>  | I <sub>OL</sub> = 1.6mA                  |                    |     | 0.4                | V    |
| INPUT LEAK CURRENT (1) | XTI             | I <sub>LH</sub>  | V <sub>IN</sub> = V <sub>DD</sub>        |                    | 10  | 20                 | μA   |
|                        |                 | I <sub>LL</sub>  | V <sub>IN</sub> = 0V                     |                    | 10  | 20                 | μA   |
| INPUT LEAK CURRENT (2) | (*1)            | I <sub>LH</sub>  | V <sub>IN</sub> = V <sub>DD</sub>        |                    |     | 1.0                | μA   |
| INPUT CURRENT          | (*2)            | I <sub>TI</sub>  | V <sub>TN</sub> = 0V                     |                    | 10  | 20                 | μA   |

&lt; TERMINAL &gt;

|    |                                                        |
|----|--------------------------------------------------------|
| *1 | LRCL, DIN, BCKI, CKSL, CKDV, SYN, RST, COB, OW20, OW18 |
| *2 | CKO, DG, DOL, DOR, WCKO, BCKO, FSCO                    |

(\*3) f<sub>sys</sub>: Frequency of internal system clock (AP ... 9.5MHz/APT ... 13MHz)

When CKDV = L f<sub>XTI</sub>/2

When CKDV = H f<sub>XTI</sub> (f<sub>XTI</sub>: Frequency of XTI input clock)

## ■ AC CHARACTERISTICS

### SM5813AP

(Ta = -20 to 70°C, V<sub>DD</sub> = 4.75 to 5.25V, V<sub>SS</sub> = 0V)

#### 1. XTI TERMINAL

##### a. In case of crystal oscillation

| ITEM                  | SYM-BOL          | MIN | TYP | MAX  | UNIT | CONDITION<br>CKSL CKDV | NOTE  |
|-----------------------|------------------|-----|-----|------|------|------------------------|-------|
| Oscillating frequency | f <sub>MAX</sub> | 1.0 |     | 9.5  | MHz  | H H                    | 192fs |
|                       |                  | 2.0 |     | 19.0 |      | H L                    | 384fs |
|                       |                  | 1.0 |     | 9.5  |      | L H                    | 256fs |
|                       |                  | 2.0 |     | 19.0 |      | L L                    | 512fs |

##### b. In case of terminal clock input

| ITEM                      | SYM-BOL | MIN | TYP | MAX  | UNIT | CONDITION<br>CKSL CKDV | NOTE  |
|---------------------------|---------|-----|-----|------|------|------------------------|-------|
| Width of clock pulse      | tcw     | 38  |     | 500  | nSec | H H                    | 192fs |
|                           |         | 15  |     | 250  |      | H L                    | 384fs |
|                           |         | 38  |     | 500  |      | L H                    | 256fs |
|                           |         | 15  |     | 250  |      | L L                    | 512fs |
| Cycle time of clock pulse | tcy     | 105 |     | 1000 | nSec | H H                    | 192fs |
|                           |         | 52  |     | 500  |      | H L                    | 384fs |
|                           |         | 105 |     | 1000 |      | L H                    | 256fs |
|                           |         | 52  |     | 500  |      | L L                    | 512fs |

#### 2. INPUT TIMING

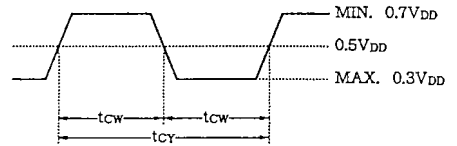
BCKI, DIN, LRCI terminal

| ITEM                                         | SYMBOL | MIN | TYP | MAX | UNIT |
|----------------------------------------------|--------|-----|-----|-----|------|
| BCKI, Pulse width                            | tbcw   | 100 |     |     | nSec |
| BCKI, Cycle time                             | tbcy   | 200 |     |     | nSec |
| DIN, Set up time                             | tds    | 75  |     |     | nSec |
| DIN, Hold time                               | tdh    | 75  |     |     | nSec |
| Rising edge of last BCKI<br>→ Edge of LRCI   | tBL    | 75  |     |     | nSec |
| Edge of LRCI<br>→ Rising edge of first BCKI  | tLB    | 75  |     |     | nSec |
| Falling edge of XTI<br>→ Rising edge of LRCI | txL    | 20  |     |     | nSec |
| Rising edge of LRCI<br>→ Falling edge of XTI | tlx    | 0   |     |     | nSec |

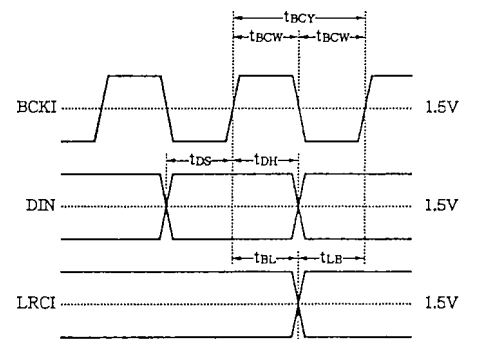
#### 3. OUPUT TIMING

| ITEM                     | SYMBOL | MIN | TYP | MAX | UNIT | NOTE      |
|--------------------------|--------|-----|-----|-----|------|-----------|
| BCKO delay time from XTI | txbH   | 35  |     | 120 | nSec | CKDV=L    |
|                          | txbL   | 35  |     | 120 |      |           |
|                          | txbH   | 35  |     | 120 | nSec | CKDV=H    |
|                          | txbL   | 35  |     | 120 |      |           |
| Output delay             | tbdL   | -10 | 0   | +10 | nSec | 15pF Load |
|                          | tbdH   | -10 | 0   | +10 |      |           |

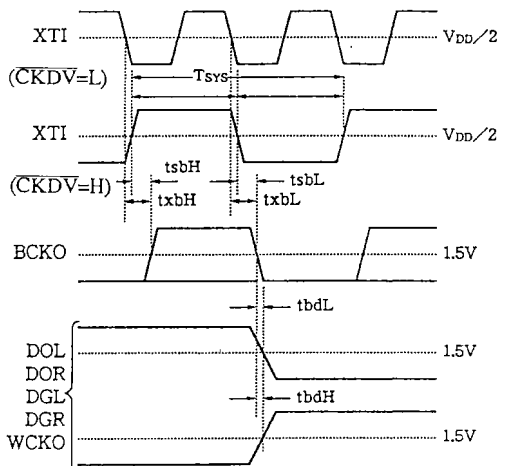
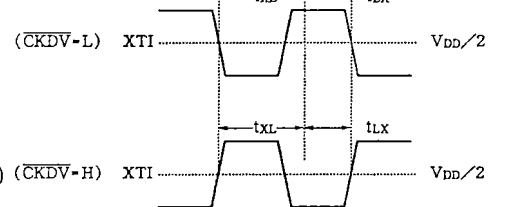
##### (1) XTI input clock



##### (2)



##### (3) (CKDV=H) XTI



## SM5813AP/APT/AF

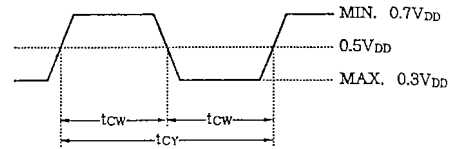
(Ta = -20 to 70°C, V<sub>DD</sub> = 4.75 to 5.25V, V<sub>SS</sub> = 0V)

## 1. XTI TERMINAL

## a. In case of crystal oscillation

| ITEM                  | SYM-BOL          | MIN | TYP | MAX  | UNIT | CONDITION<br>CKSL CKDV | NOTE  |
|-----------------------|------------------|-----|-----|------|------|------------------------|-------|
| Oscillating frequency | f <sub>MAX</sub> | 1.0 |     | 13.0 | MHz  | H H                    | 192fs |
|                       |                  | 2.0 |     | 26.0 |      | H L                    | 384fs |
|                       |                  | 1.0 |     | 13.0 |      | L H                    | 256fs |
|                       |                  | 2.0 |     | 26.0 |      | L L                    | 512fs |

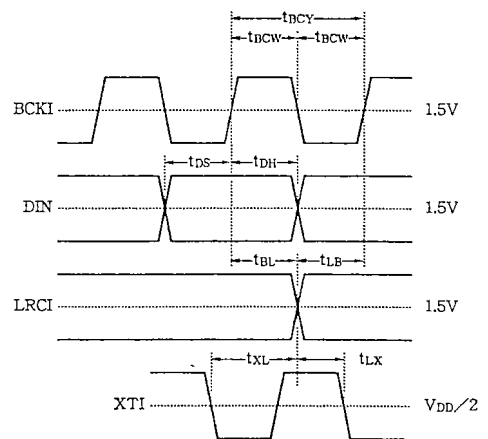
## (1) XTI input clock



## b. In case of external clock input

| ITEM                      | SYM-BOL         | MIN | TYP | MAX  | UNIT | CONDITION<br>CKSL CKDV | NOTE  |
|---------------------------|-----------------|-----|-----|------|------|------------------------|-------|
| Width of clock pulse      | t <sub>pw</sub> | 35  |     | 500  | nSec | H H                    | 192fs |
|                           |                 | 15  |     | 250  |      | H L                    | 384fs |
|                           |                 | 35  |     | 500  |      | L H                    | 256fs |
|                           |                 | 15  |     | 250  |      | L L                    | 512fs |
| Cycle time of clock pulse | t <sub>cy</sub> | 76  |     | 1000 | nSec | H H                    | 192fs |
|                           |                 | 38  |     | 500  |      | H L                    | 384fs |
|                           |                 | 76  |     | 1000 |      | L H                    | 256fs |
|                           |                 | 38  |     | 500  |      | L L                    | 512fs |

## (2)

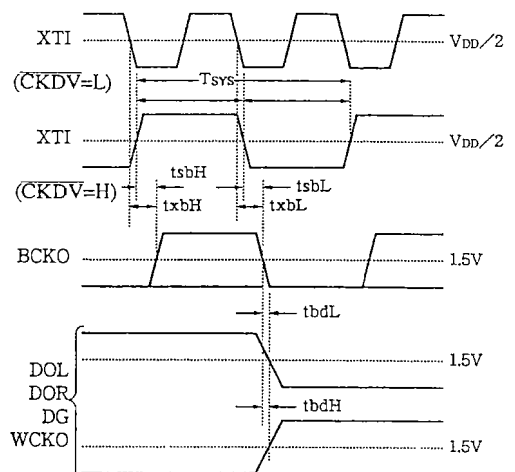


## 2. INPUT TIMING

BCKI, DIN, LRCI terminal

| ITEM                                         | SYMBOL          | MIN | TYP | MAX | UNIT |
|----------------------------------------------|-----------------|-----|-----|-----|------|
| BCKI, Pulse width                            | t <sub>pw</sub> | 100 |     |     | nSec |
| BCKI, Cycle time                             | t <sub>cy</sub> | 200 |     |     | nSec |
| DIN, Set up time                             | t <sub>ds</sub> | 75  |     |     | nSec |
| DIN, Hold time                               | t <sub>dh</sub> | 75  |     |     | nSec |
| Rising edge of last BCKI<br>→ Edge of LRCI   | t <sub>bl</sub> | 75  |     |     | nSec |
| Edge of LRCI<br>→ Rising edge of first BCKI  | t <sub>lb</sub> | 75  |     |     | nSec |
| Falling edge of XTI<br>→ Rising edge of LRCI | t <sub>xl</sub> | 20  |     |     | nSec |
| Rising edge of LRCI<br>→ Falling edge of XTI | t <sub>lx</sub> | 0   |     |     | nSec |

## (3)



## 3. OUTPUT TIMING

| ITEM                     | SYMBOL | MIN | TYP | MAX | UNIT | NOTE      |
|--------------------------|--------|-----|-----|-----|------|-----------|
| BCKO delay time from XTI | txbH   | 35  |     | 120 | nSec | CKDV=L    |
|                          | txbL   | 35  |     | 120 |      | CKDV=L    |
|                          | txbH   | 35  |     | 120 | nSec | CKDV=H    |
|                          | txbL   | 35  |     | 120 |      | CKDV=H    |
| Output delay             | tbdL   | -10 |     | +10 | nSec | 15pF Load |
|                          | tbdH   | -10 |     | +10 |      | 15pF Load |



## ■ FUNCTION

### 1. EIGHT-TIMES OVERSAMPLING

Input of  $f_s$  sampling rate to the SM5813 is output with  $8f_s$  sampling rate after calculating in the digital filter.

This LSI has cascaded three-stage FIR filter as follows:

### 2. SYSTEM CLOCK

#### • SELECTION OF SYSTEM CLOCK

The SM5813AP/APT/AF has an internal clock generator that may be used by connecting a crystal of the appropriate frequency between pins XTI and XTO. Alternatively, an externally generated clock can be input on XTI. The clock frequency  $F_{xi}$  is selected by the CKDV and CKSL inputs from one of the four multiples of the sample frequency shown in the right table, where the clock period  $t_{xi}=1/F_{xi}$ . For the 384fs and 512fs clock frequencies, the clock is divided by two for internal use. The system clock signal, of the same frequency as the signal on pin XTI, is available on the CKO output pin.

| CONDITION |      | XTI clock ( $F_{xi}$ ) | Cycle time of internal system clock |
|-----------|------|------------------------|-------------------------------------|
| CKDV      | CKSL |                        |                                     |
| H         | H    | 192fs                  |                                     |
| H         | L    | 256fs                  | $1/F_{xi}$                          |
| L         | H    | 384fs                  |                                     |
| L         | L    | 512fs                  | $2/F_{xi}$                          |

### 3. AUDIO DATA INPUT

Input data is processed MSB first and 2's complement. Each bit of serial data input on the DIN pin is read into the SIPO register (serial to parallel conversion register) at the rising-edge of BCKI bit clock and converted to parallel data. The SIPO output is transferred to the Lch/Rch input register, respectively, at the rising-edge/falling-edge of the LRCI clock. (See Figure A and B)

The timing of the operation part and output part are independent from the timing of the input part, so that it is not affected by jitter of the input part.

### 4. JITTER-FREE MODE AND FORCED SYNCHRONIZATION MODE SELECTION ( $\overline{SYN}$ , FSCO)

The timing of the internal operation and output (internal timing) are determined by the system clock (the XTI input), which is independent of the input clock timing (BCKI, LRCI).

The internal timing is provided with 2 kinds of "jitter-free mode," and "forced synchronization mode" to cope with jitter on the LRCI clock input. The setting of  $\overline{SYN}$  enables selection.

Figure A. Input SIPO

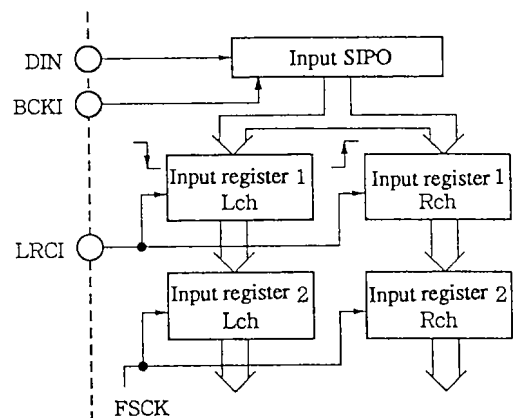
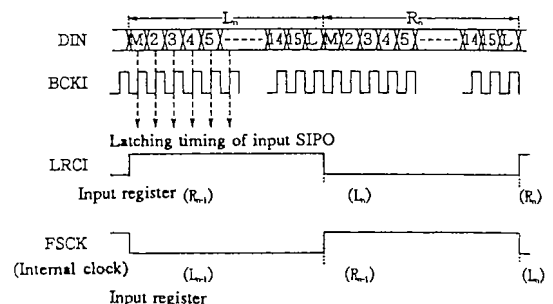


Figure B. Input timing of audio data



● Jitter-free mode ( $\overline{\text{SYN}}=\text{H}$ )

When the phase difference between the LRCI clock and the internal timing is within  $+3/8$  to  $-3/8$  of the input sampling frequency ( $1/f_s$ ), the internal timing is not adjusted. Thus jitter on the LRCI clock does not affect the internal timing to prevent malfunctions and jitter transmission.

If the phase difference exceeds the said range, the phase of internal timing is adjusted synchronously with the starting-side edge of the LRCI clock. When a reset is input, the phase is also adjusted.

● Forced synchronization mode ( $\overline{\text{SYN}}=\text{L}$ )

In this mode, the internal timing is always reset at the starting-edge of the LRCI input.

In this case, malfunction occurs if a cycle which does not satisfy the required system clock cycle due to jitter on the LRCI input exists. To the contrary, if a cycle which is longer than the specified clock cycle exists, the intervals of the output timing are not the same though operation is performed correctly.

● FSCO clock (output)

The  $f_s$  frequency clock obtained by dividing the XTI clock.

5. DATA AND DAC CONTROL SIGNAL OUTPUT

(DOL, DOR, BCKO, WCKO, DG,  $\overline{\text{COB}}$ ,  $\overline{\text{OW18}}$ ,  $\overline{\text{OW20}}$ )

Table B. Output timing

| Item                        | Sym-<br>bol | CKSL    |         |
|-----------------------------|-------------|---------|---------|
| Internal system clock freq. |             | 192fs   | 256fs   |
| Bit clock cycle             | Tb          | Tsys    | Tsys    |
| Data word length            | Tw          | 24×Tsys | 32×Tsys |

● Output data format

(1) MSB first

(2) 2's complement and COB (complemented offset binary) switch

COB format ( $\overline{\text{COB}}=\text{H}$ )

COB format ( $\overline{\text{COB}}=\text{L}$ )

● Bit number selection of output data ( $\overline{\text{OW18}}$ ,  $\overline{\text{OW20}}$ )

Bit number of output data can be selected from among 16, 18 and 20.

16-bit output ( $\overline{\text{OW18}}=\text{H}$ ,  $\overline{\text{OW20}}=\text{H}$ )

18-bit output ( $\overline{\text{OW18}}=\text{L}$ ,  $\overline{\text{OW20}}=\text{H}$ )

20-bit output ( $\overline{\text{OW18}}=\text{H}$ ,  $\overline{\text{OW20}}=\text{L}$ )

● Output timing

The timing of audio output part is determined corresponding to the system clock frequency of each part. (See Table B, Figure C)

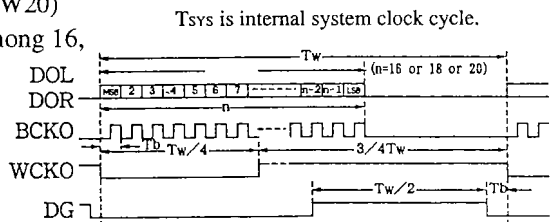


Table C. Output timing

6. SYSTEM RESET ( $\overline{\text{RST}}$ )

When a reset is input in the jitter-free mode, the internal operation timing is reset synchronously with the rising-edge of the following LRCI clock input. Taking advantage of this, the output timing in the jitter-free mode can match to LRCI.

The reset pulse (L level) should be longer than 50ns after power-on. A reset is also unnecessary in the jitter-free mode if the output timing is not required to match with the LRCI input.

In the case of performing the system reset at power-on, connect a 100pF or so capacitor to the RST pin. (See Figure D).

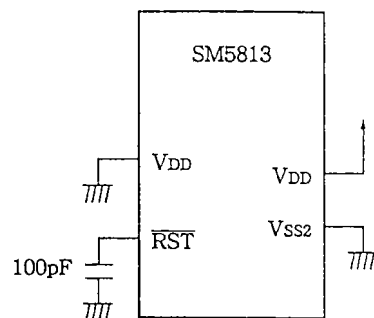
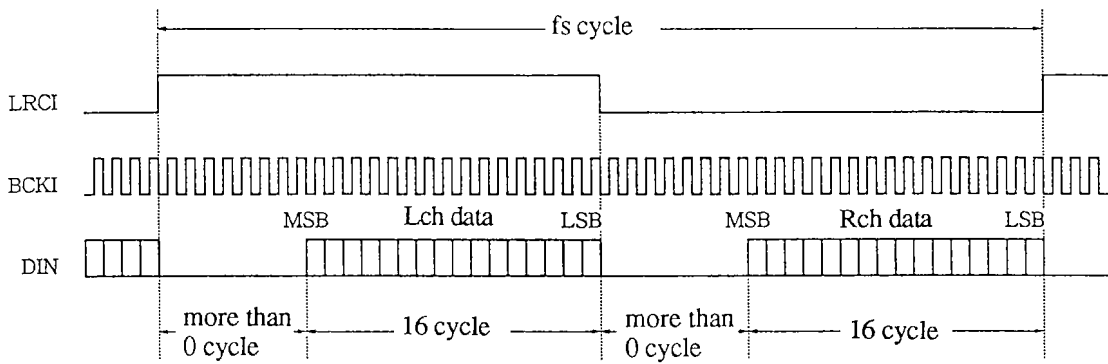


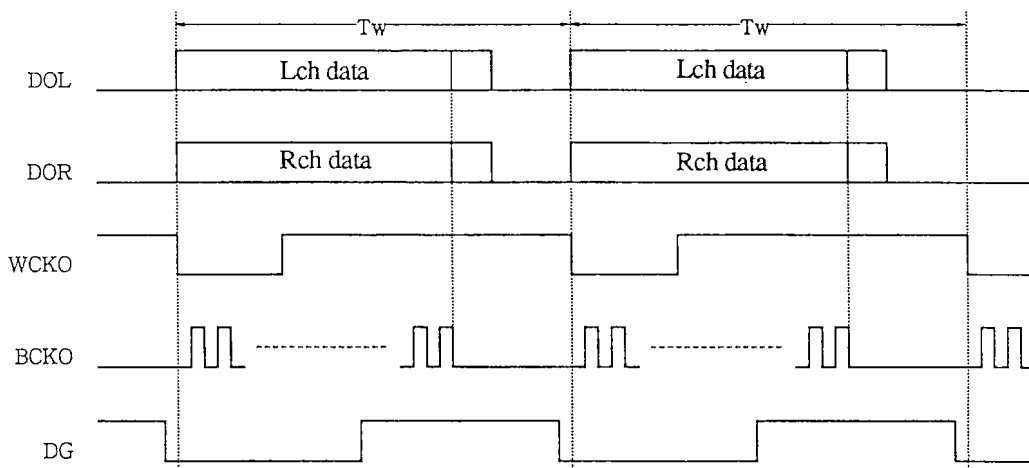
Table D. System reset circuit sample at power-on

## ■ TIMING CHART

### 1. SERIAL INPUT TIMING

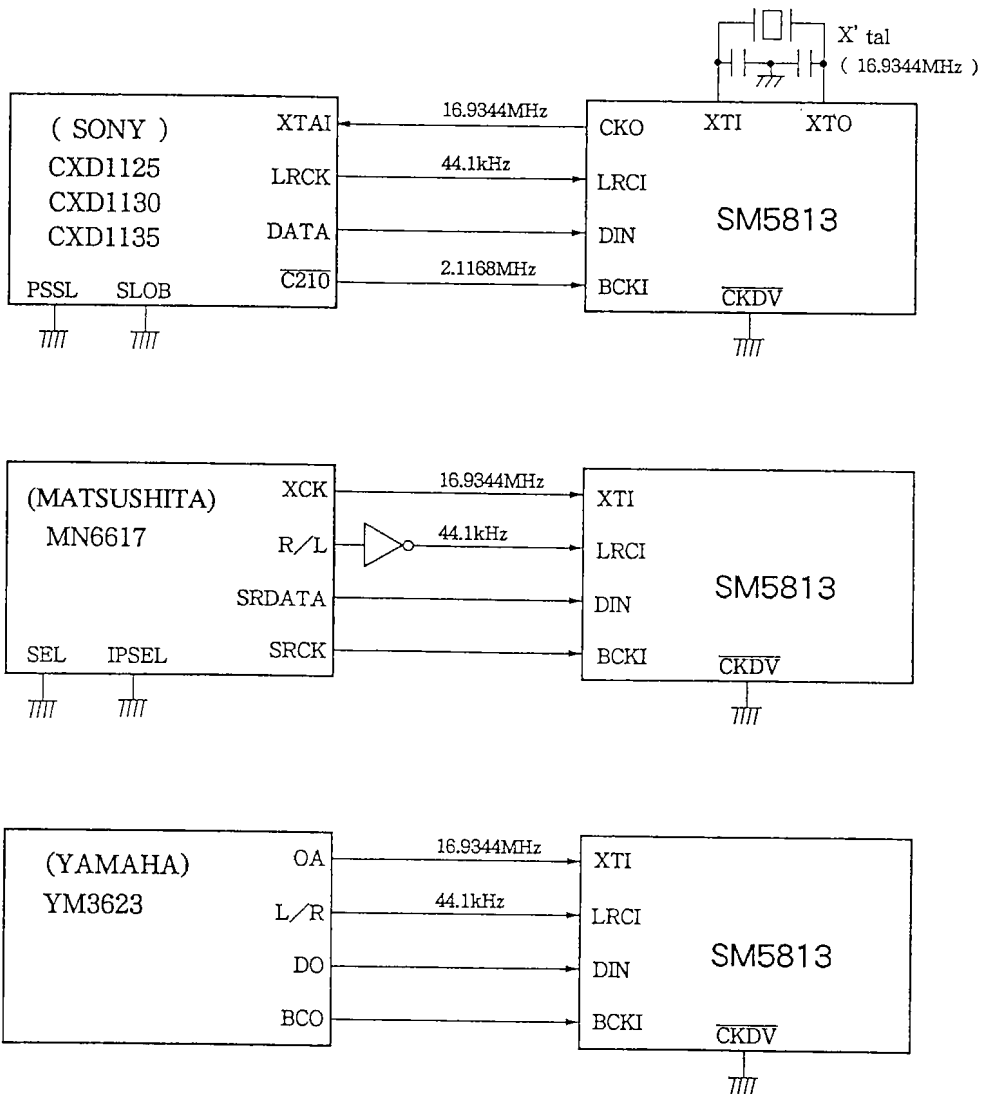


### 2. SERIAL OUTPUT TIMING



## ■ TYPICAL APPLICATION

### 1. INPUT



## 2. OUTPUT

