National Semiconductor

March 1999

DS90C031B
LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031B is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C031B accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 11 mW typical.

In addition, the DS90C031B provides power-off high impedance LVDS outputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present.

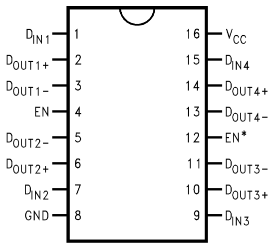
The DS90C031B and companion line receiver (DS90C032B) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- High impedance LVDS outputs with power-off
- ±350 mV differential signaling
- Ultra low power dissipation
- 400 ps maximum differential skew (5V, 25˚C)
- 3.5 ns maximum propagation delay
- Industrial operating temperature range
- Pin compatible with DS26C31, MB571 (PECL) and 41LG (PECL)
- Conforms to ANSI/TIA/EIA-644 LVDS standard
- Offered in narrow and wide body SOIC package
- Fail-safe logic for floating inputs

Connection Diagram

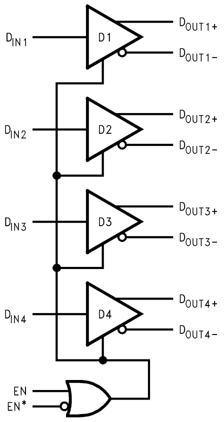
Dual-In-Line



DS100989-1

Order Number
DS90C031BTM,
or DS90C031BTWM
See NS Package Number
M16A or M16B

Functional Diagram



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Driver Truth Table

Enables		Input	Outputs	
EN	EN*	D_{IN}	D_{OUT+}	D_{OUT-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-})	−0.3V to +5.8V
Short Circuit Duration (D_{OUT+}, D_{OUT-})	Continuous
Maximum Package Power Dissipation @ +25˚C	
M Package	1068 mW
WM Package	1562 mW
Derate M Package	8.5 mW/˚C above +25˚C
Derate WM Package	12.5 mW/˚C above +25˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range Soldering (4 sec.)	+260˚C
Maximum Junction Temperature	+150˚C
ESD Rating (Note 7)	
(HBM, 1.5 kΩ, 100 pF)	≥ 2kV
(EIAJ, 0 Ω, 200 pF)	≥ 250V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Operating Free Air Temperature (T_A)				
DS90C031BT	−40	+25	+85	˚C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (*Figure 1*)	D_{OUT-}, D_{OUT+}	250	345	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.10	1.25	1.35	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High	R_L = 100Ω			1.41	1.60	V
V_{OL}	Output Voltage Low			0.90	1.07		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_I	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V		−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 8)	D_{OUT-}, D_{OUT+}		−3.5	−5.0	mA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V, V_{OUT} = 0V or V_{CC}		−10	±1	+10	µA
I_{OFF}	Power - Off Leakage	V_O = 0V or 2.4V, V_{CC} = 0V or Open		−10	±1	+10	µA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		1.7	3.0	mA
		D_{IN} = 2.5V or 0.4V			4.0	6.5	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω (all channels) V_{IN} = V_{CC} or GND (all inputs)			15.4	21.0	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND EN = GND, EN* = V_{CC}			2.2	4.0	mA

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C (Notes 3, 6, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (*Figure 2* and *Figure 3*)	1.0	2.0	3.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	2.1	3.0	ns
t_{SKD}	Differential Skew |t_{PHLD} – t_{PLHD}|		0	80	400	ps
t_{SK1}	Channel-to-Channel Skew (Note 4)		0	300	600	ps
t_{TLH}	Rise Time			0.35	1.5	ns
t_{THL}	Fall Time			0.35	1.5	ns

Switching Characteristics (Continued)

V_{CC} = +5.0V, T_A = +25˚C (Notes 3, 6, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 5 pF (*Figure 4* and *Figure 5*)		2.5	10	ns
t_{PLZ}	Disable Time Low to Z			2.5	10	ns
t_{PZH}	Enable Time Z to High			2.5	10	ns
t_{PZL}	Enable Time Z to Low			2.5	10	ns

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −40˚C to +85˚C (Notes 3, 6, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (*Figure 2* and *Figure 3*)	0.5	2.0	3.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.5	2.1	3.5	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	80	900	ps
t_{SK1}	Channel-to-Channel Skew (Note 4)		0	0.3	1.0	ns
t_{SK2}	Chip to Chip Skew (Note 5)				3.0	ns
t_{TLH}	Rise Time			0.35	2.0	ns
t_{THL}	Fall Time			0.35	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 5 pF (*Figure 4* and *Figure 5*)		2.5	15	ns
t_{PLZ}	Disable Time Low to Z			2.5	15	ns
t_{PZH}	Enable Time Z to High			2.5	15	ns
t_{PZL}	Enable Time Z to Low			2.5	15	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = +25˚C.

Note 4: Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.

Note 5: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Note 6: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, $t_r \le 6$ ns, and $t_f \le 6$ ns.

Note 7: ESD Ratings:

HBM (1.5 kΩ, 100 pF) ≥ 2kV

EIAJ (0Ω, 200 pF) ≥ 250V

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 9: C_L includes probe and jig capacitance.

Parameter Measurement Information

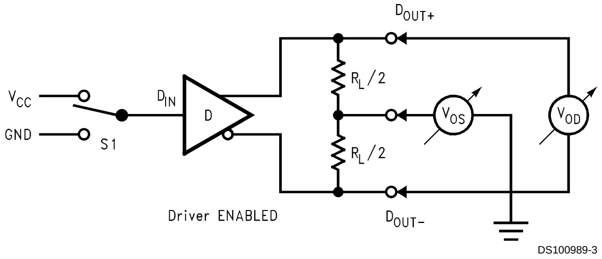

FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit

Parameter Measurement Information (Continued)

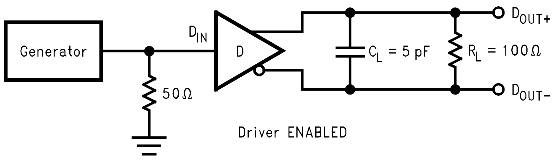

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FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

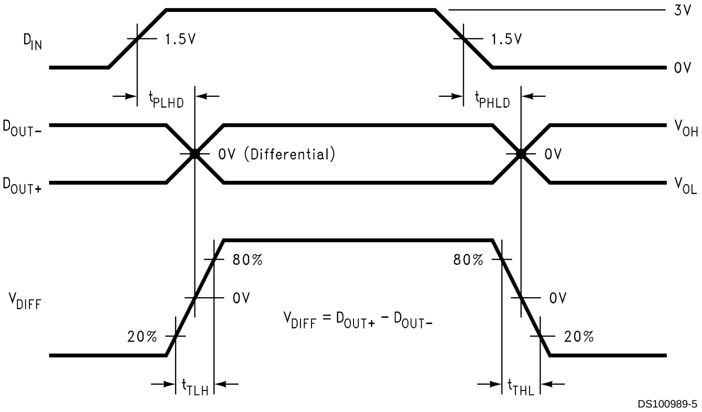

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FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

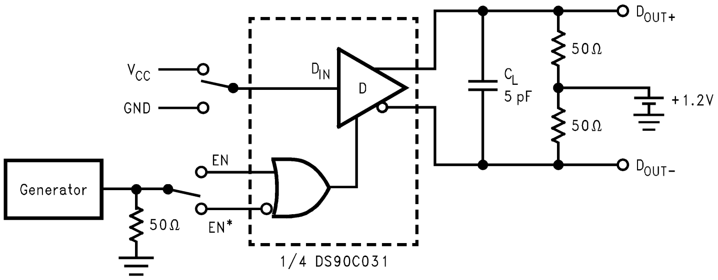

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FIGURE 4. Driver TRI-STATE Delay Test Circuit

Parameter Measurement Information (Continued)

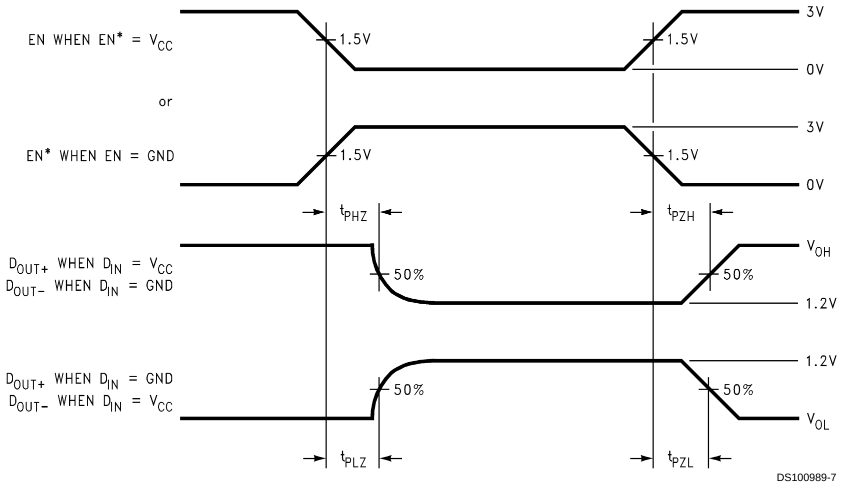


FIGURE 5. Driver TRI-STATE Delay Waveform

Typical Application

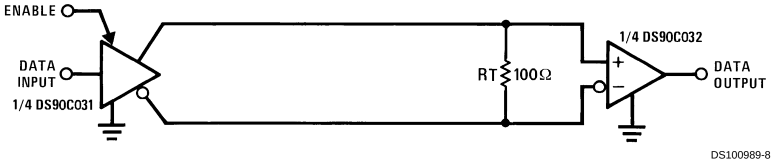


FIGURE 6. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 6*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C031B differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is a mere 3.4 mA with a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in *Figure 6*. AC or unterminated configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the 100Ω termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340 mV – 100 mV = 240 mV). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in*Figure 7*. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The fail-safe circuitry guarantees that the outputs are enabled and at a logic ’0’ (the true output is low and the complement output is high) when the inputs are floating.

Applications Information (Continued)

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90C031B is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver.

The DS90C031B is electrically similar to the DS90C031, but differs by supporting high impedance LVDS outputs under power-off condition. This allows for multiple or redundant drivers to be used in certain applications. The DS90C031B is offered in a 300 mil. wide SOIC, allowing direct conversion to Quad PECL drivers to LVDS. It is also offered in a space saving narrow SOIC (150 mil.) package.

For additional LVDS application information, please refer to National's LVDS Owner's Manual available through National's website www.national.com/appinfo/lvds.

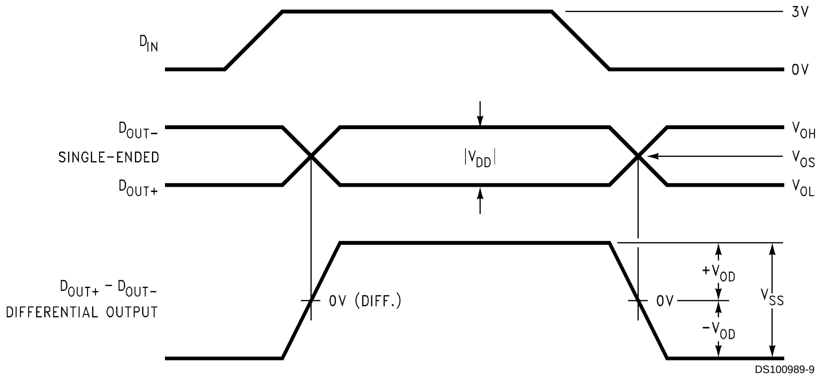


FIGURE 7. Driver Output Levels

Pin Descriptions

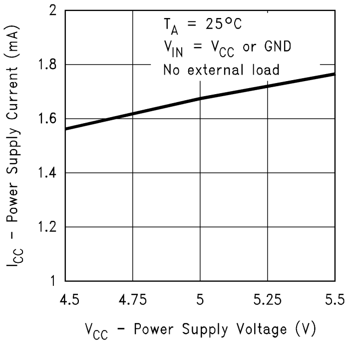
Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{OUT+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ± 10%
8	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40˚C to +85˚C	SOP/M16A	DS90C031BTM
−40˚C to +85˚C	SOP/M16B	DS90C031BTWM

Typical Performance Characteristics

Power Supply Current vs Power Supply Voltage



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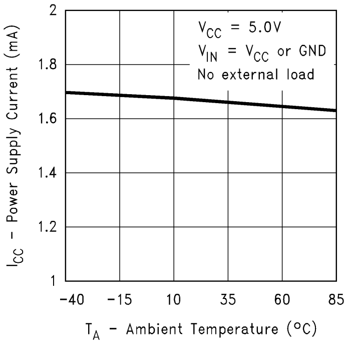
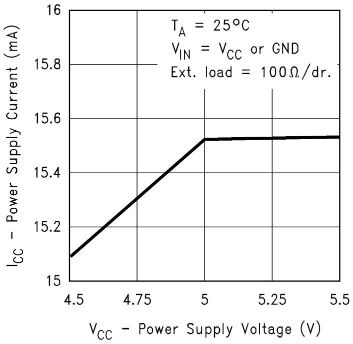
Power Supply Current vs Temperature



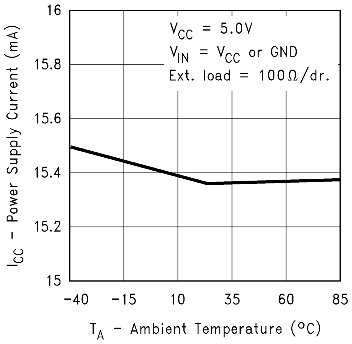
DS100989-11

Power Supply Current vs Power Supply Voltage



DS100989-12

Power Supply Current vs Temperature



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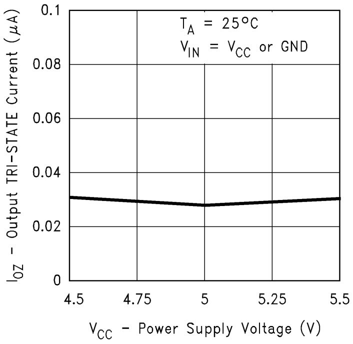
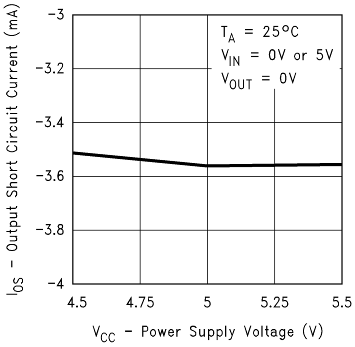
Output TRI-STATE Current vs Power Supply Voltage



DS100989-14

Output Short Circuit Current vs Power Supply Voltage



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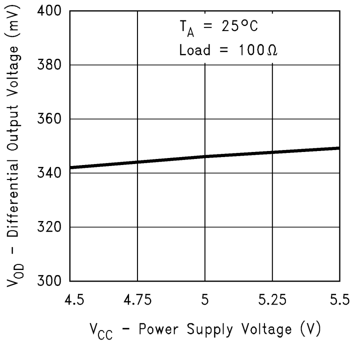
Typical Performance Characteristics (Continued)

Differential Output Voltage vs Power Supply Voltage



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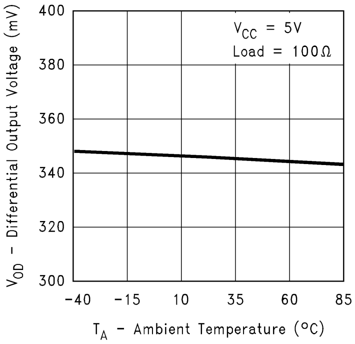
Differential Output Voltage vs Ambient Temperature



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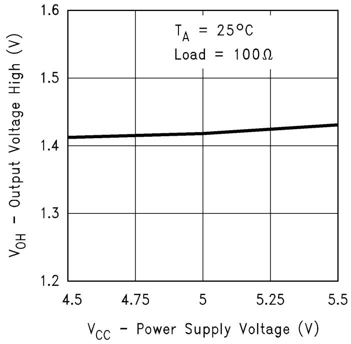
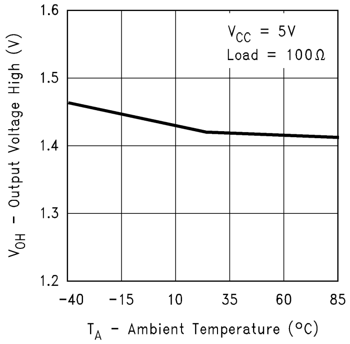
Output Voltage High vs Power Supply Voltage



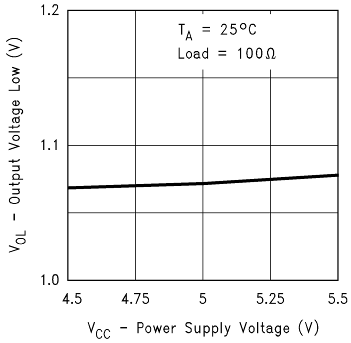
DS100989-18

Output Voltage High vs Ambient Temperature



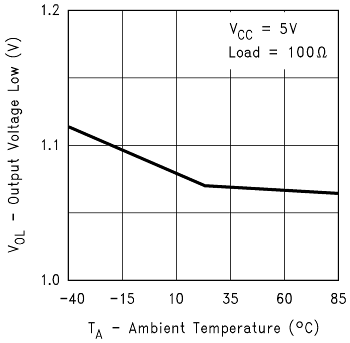
DS100989-19

Output Voltage Low vs Power Supply Voltage



DS100989-20

Output Voltage Low vs Ambient Temperature



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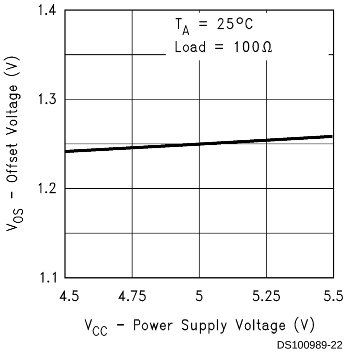
Typical Performance Characteristics (Continued)

Offset Voltage vs Power Supply Voltage



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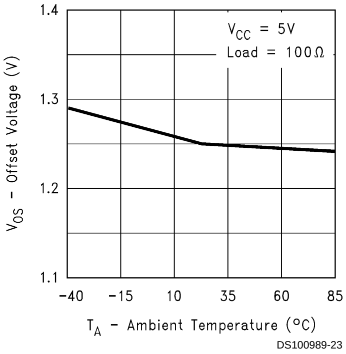
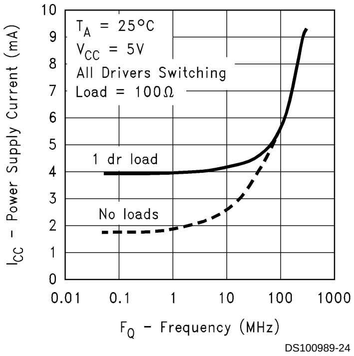
Offset Voltage vs Ambient Temperature



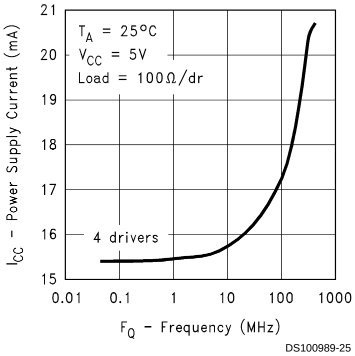
DS100989-23

Power Supply Current vs Frequency



DS100989-24

Power Supply Current vs Frequency



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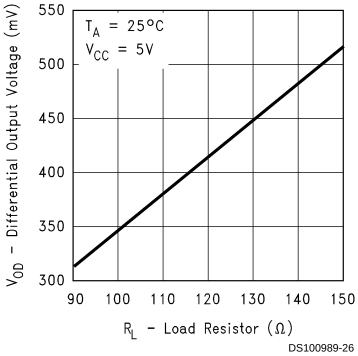
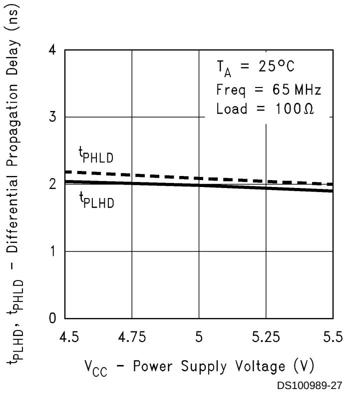
Differential Output Voltage vs Load Resistor



DS100989-26

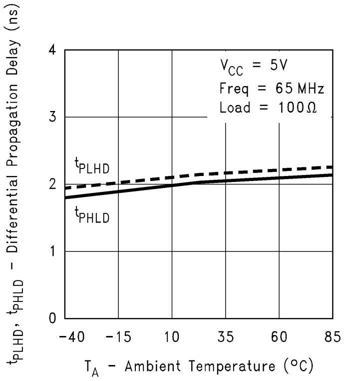
Differential Propagation Delay vs Power Supply Voltage



DS100989-27

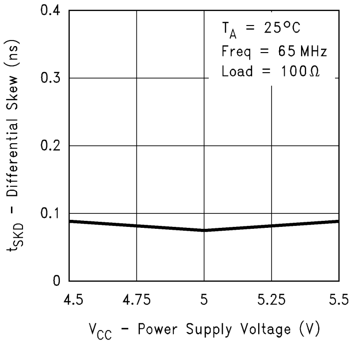
Typical Performance Characteristics (Continued)

Differential Propagation Delay vs Ambient Temperature



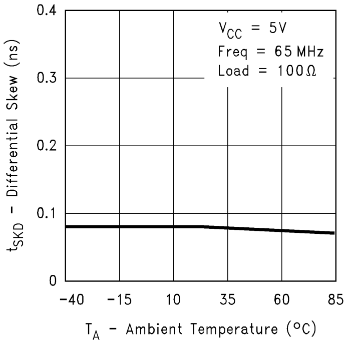
DS100989-28

Differential Skew vs Power Supply Voltage



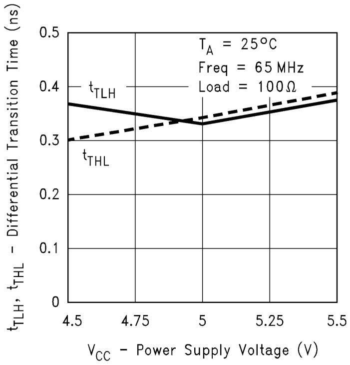
DS100989-29

Differential Skew vs Ambient Temperature



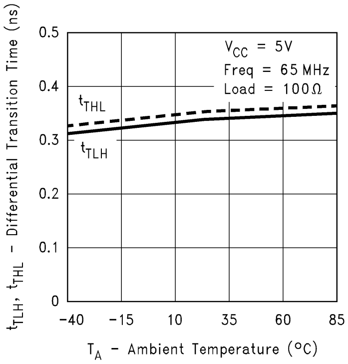
DS100989-30

Differential Transition Time vs Power Supply Voltage



DS100989-31

Differential Transition Time vs Ambient Temperature



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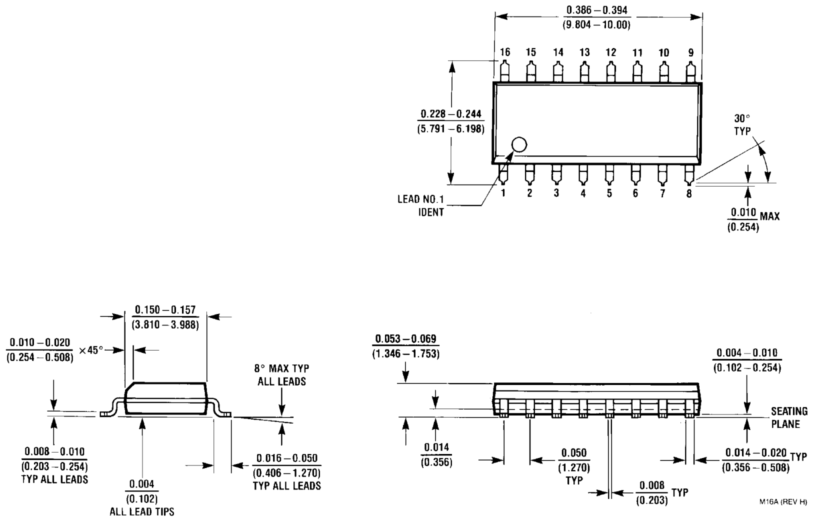
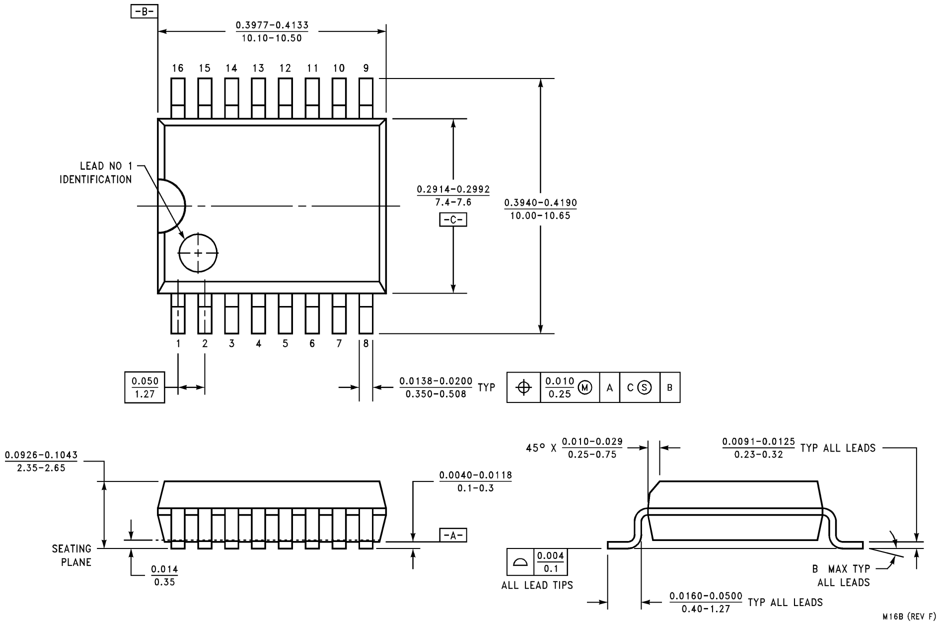
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS90C031BTM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
Order Number DS90C031BTWM
NS Package Number M16B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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