TPS65988DJ Dual Port USB Type-C and USB PD Controller with Integrated Power Switches

1 Features

- USB Power Delivery (PD) controller
  - USB PD 3.0 compliant (TID: 1099)
  - Fast role swap support
  - Physical layer and policy engine
  - Configurable at boot and host-controlled
- USB Type-C specification compliant
  - Cable attach and orientation detection
  - Default, 1.5-A, or 3-A power advertisement
  - Up to 600-mA VConn current
- Port power switch
  - Two 5 V to 20 V, 5-A bidirectional switches to or from VBUS
  - Up to 10-A Adjustable current limiting
  - Ideal diode reverse current protection
  - Undervoltage, and overvoltage protection
  - Slew rate control
  - 5-V, 600-mA VConn source
- BC1.2 Support
  - Advertisement as DCP and CDP
  - Automatic DCP modes selection:
    - Shorted mode per BC1.2 and YD/T 1591-2009
    - 2.7-V Divider 3 mode
    - 1.2-V Mode
  - Data contact detect
  - Primary and secondary detection
- I2C Master write control for alt mode muxes and variable DCDCs
- Alternate mode support
  - Displayport
  - Thunderbolt™
- Power management
  - Power supply from 3.3 V or VBUS source
  - 3.3-V LDO Output for dead battery support
- 7-mm × 7-mm QFN package
  - 0.4-mm Pitch
  - 56 Pin

2 Applications

- Notebook computers
- Docking systems
- Tablets and ultrabooks
- Displayport, and Thunderbolt™ systems

3 Description

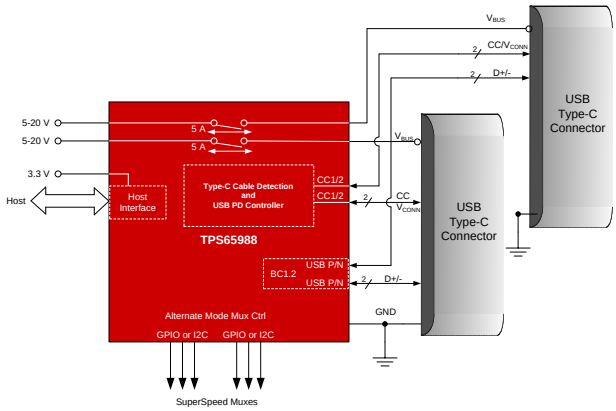
The TPS65988DJ is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C connectors. Upon cable detection, the TPS65988DJ communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988DJ enables the appropriate power path and configures alternate mode settings for external multiplexers.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65988DJ	QFN (56)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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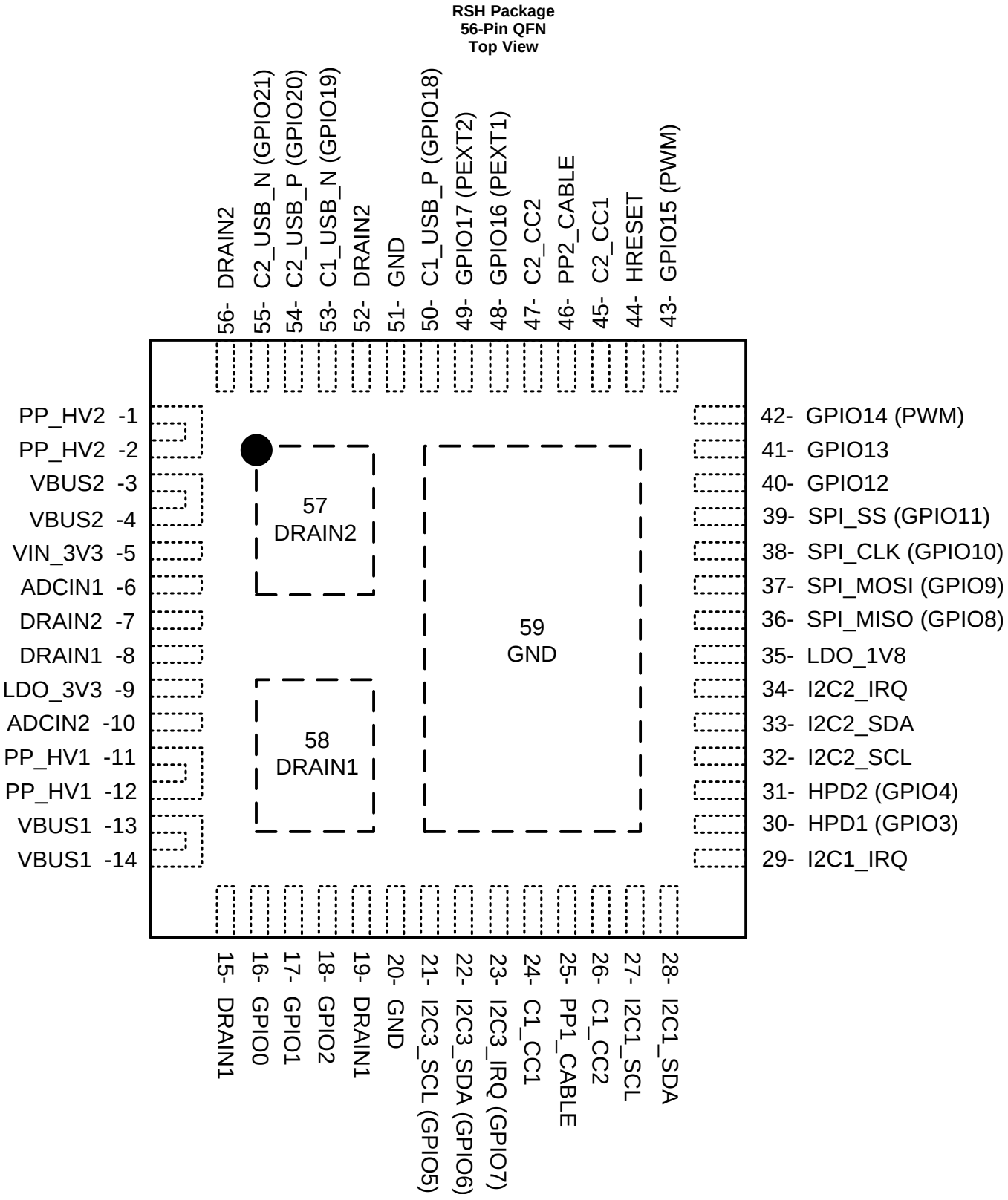
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4 Revision History

DATE	REVISION	NOTES
May 2019	*	Initial release.

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5 Pin Configuration and Functions



Pin Functions

PIN		TYPE(1)	RESET STATE(2)	DESCRIPTION
NAME	NO.			
ADCIN1	6	I	Input	Boot configuration Input. Connect to resistor divider between LDO_3V3 and GND.
ADCIN2	10	I	Input	I2C address configuration Input. Connect to resistor divider between LDO_3V3 and GND.
C1_CC1	24	I/O	High-Z	Output to Type-C CC or VCONN pin for port 1. Filter noise with capacitor to GND
C1_CC2	26	I/O	High-Z	Output to Type-C CC or VCONN pin for port 1. Filter noise with capacitor to GND
C1_USB_N (GPIO19)	53	I/O	Input (High-Z)	Port 1 USB D– connection for BC1.2 support
C1_USB_P (GPIO18)	50	I/O	Input (High-Z)	Port 1 USB D+ connection for BC1.2 support
C2_CC1	45	I/O	High-Z	Output to Type-C CC or VCONN pin for port 2. Filter noise with capacitor to GND
C2_CC2	47	I/O	High-Z	Output to Type-C CC or VCONN pin for port 2. Filter noise with capacitor to GND
C2_USB_N (GPIO21)	55	I/O	Input (High-Z)	Port 2 USB D– connection for BC1.2 support
C2_USB_P (GPIO20)	54	I/O	Input (High-Z)	Port 2 USB D+ connection for BC1.2 support
DRAIN1	8, 15, 19, 58	—	—	Drain of internal power path 1. Connect thermal pad 58 to as big of pad as possible on PCB for best thermal performance. Short the other pins to this thermal pad
DRAIN2	7, 52, 56, 57	—	—	Drain of internal power path 2. Connect thermal pad 57 to as big of pad as possible on PCB for best thermal performance. Short the other pins to this thermal pad
GND	20, 51	—	—	Unused pin. Tie to GND.
GPIO0	16	I/O	Input (High-Z)	General Purpose Digital I/O 0. Float pin when unused. GPIO0 is asserted low during the TPS65988DJ boot process. Once device configuration and patches are loaded GPIO0 is released
GPIO1	17	I/O	Input (High-Z)	General Purpose Digital I/O 1. Ground pin with a 1-MΩ resistor when unused in the application
GPIO2	18	I/O	Input (High-Z)	General Purpose Digital I/O 2. Float pin when unused
GPIO3 (HPD1)	30	I/O	Input (High-Z)	General Purpose Digital I/O 3. Configured as Hot Plug Detect (HPD) TX and RX for port 1 when DisplayPort alternate mode is enabled. Float pin when unused
GPIO4 (HPD2)	31	I/O	Input (High-Z)	General Purpose Digital I/O 4. Configured as Hot Plug Detect (HPD) TX and RX for port 2 when DisplayPort alternate mode is enabled. Float pin when unused
I2C3_SCL (GPIO5)	21	I/O	Input (High-Z)	I2C port 3 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used. Float pin when unused
I2C3_SDA (GPIO6)	22	I/O	Input (High-Z)	I2C port 3 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used. Float pin when unused
$\overline{\text{I2C3_IRQ}}$ (GPIO7)	23	I/O	Input (High-Z)	I2C port 3 interrupt detection (port 3 operates as an I2C Master Only). Active low detection. Connect to the I2C slave's interrupt line to detect when the slave issues an interrupt. Float pin when unused
GPIO12	40	I/O	Input (High-Z)	General Purpose Digital I/O 12. Float pin when unused

(1) I = input, O = output, I/O = bidirectional, GND = ground, PWR = power, NC = no connect
(2) Reset State indicates the state of a given pin immediately following power application, prior to any configuration from firmware.

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Pin Functions (continued)

PIN		TYPE(1)	RESET STATE(2)	DESCRIPTION
NAME	NO.			
GPIO13	41	I/O	Input (High-Z)	General Purpose Digital I/O 13. Float pin when unused
GPIO14 (PWM)	42	I/O	Input (High-Z)	General Purpose Digital I/O 14. May also function as a PWM output. Float pin when unused
GPIO15 (PWM)	43	I/O	Input (High-Z)	General Purpose Digital I/O 15. May also function as a PWM output. Float pin when unused
GPIO16 (PP_EXT1)	48	I/O	Input (High-Z)	General Purpose Digital I/O 16. May also function as single wire enable signal for external power path 1. Pull-down with external resistor when used for external path control. Float pin when unused
GPIO17 (PP_EXT2)	49	I/O	Input (High-Z)	General Purpose Digital I/O 17. May also function as single wire enable signal for external power path 2. Pull-down with external resistor when used for external path control. Float pin when unused
HRESET	44	I/O	Input	Active high hardware reset input. Will reinitialize all device settings. Ground pin when HRESET functionality will not be used
$\overline{\text{I2C1_IRQ}}$	29	O	High-Z	I2C port 1 interrupt. Active low. Implement externally as an open drain with a pull-up resistance. Float pin when unused
I2C1_SCL	27	I/O	High-Z	I2C port 1 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
I2C1_SDA	28	I/O	High-Z	I2C port 1 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
$\overline{\text{I2C2_IRQ}}$	34	O	High-Z	I2C port 2 interrupt. Active low. Implement externally as an open drain with a pull-up resistance. Float pin when unused
I2C2_SCL	32	I/O	High-Z	I2C port 2 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
I2C2_SDA	33	I/O	High-Z	I2C port 2 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
LDO_1V8	35	PWR	—	Output of the 1.8-V LDO for internal circuitry. Bypass with capacitor to GND
LDO_3V3	9	PWR	—	Output of the VBUS to 3.3-V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power external flash memory. Bypass with capacitor to GND
PP1_CABLE	25	PWR	—	5-V supply input for port 1 C_CC pins. Bypass with capacitor to GND
PP2_CABLE	46	PWR	—	5-V supply input for port 2 C_CC pins. Bypass with capacitor to GND
PP_HV1	11, 12	PWR	—	System side of first VBUS power switch. Bypass with capacitor to ground. Tie to ground when unused
PP_HV2	1, 2	PWR	—	System side of second VBUS power switch. Bypass with capacitor to ground. Tie to ground when unused
SPI_CLK	38	I/O	Input	SPI serial clock. Ground pin when unused
SPI_MISO	36	I/O	Input	SPI serial master input from slave. Ground pin when unused
SPI_MOSI	37	I/O	Input	SPI serial master output to slave. Ground pin when unused
$\overline{\text{SPI_SS}}$	39	I/O	Input	SPI slave select. Ground pin when unused

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Pin Functions (continued)

PIN		TYPE[1]	RESET STATE[2]	DESCRIPTION
NAME	NO.			
VBUS1	13, 14	PWR	—	Port side of first VBUS power switch. Bypass with capacitor to ground.
VBUS2	3, 4	PWR	—	Port side of second VBUS power switch. Bypass with capacitor to ground.
VIN_3V3	5	PWR	—	Supply for core circuitry and I/O. Bypass with capacitor to GND
Thermal Pad (PPAD)	59	GND	—	Ground reference for the device as well as thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad must be connected to a ground plane

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2)	PPx_CABLE	–0.3	6	V
	VIN_3V3	–0.3	3.6	
Output voltage(2)	LDO_1V8	–0.3	2	V
	LDO_3V3	–0.3	3.6	
	$\overline{\text{I2Cx_IRQ}}$, SPI_MOSI, SPI_CLK, $\overline{\text{SPI_SS}}$, SWD_CLK	–0.3	LDO_3V3 + 0.3 (3)	
I/O voltage (2)	PP_HVx, VBUSx(4)	–0.3	24	V
	I2Cx_SDA, I2Cx_SCL, SPI_MISO, GPIOn, HRESET, ADCINx	–0.3	LDO_3V3 + 0.3 (3)	
	Cx_USB_P, Cx_USB_N	–0.5	6	
	Cx_CC1, Cx_CC2	–0.5	6	
Operating junction temperature, T_J		–10	125	°C
Operating junction temperature PPHV switch, T_J		–10	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to underside power pad. The underside power pad should be directly connected to the ground plane of the board.
(3) Not to exceed 3.6V
(4) For VBUSx a TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltage, V_I(1)	VIN_3V3	3.135		3.45	V
	PP_CABLE	2.95		5.5	
	PP_HV	4.5		22	
I/O voltage, V_{IO}(1)	VBUS	4		22	V
	Cx_USB_P, Cx_USB_N	0		LDO_3V3	
	Cx_CC1, Cx_CC2	0		5.5	
	GPIOn, I2Cx_SDA, I2Cx_SCL, SPI, ADCIN1, ADCIN2	0		LDO_3V3	
Operating ambient temperature, T_A		–10		75	°C
Operating junction temperature, T_J		–10		125	

(1) All voltage values are with respect to underside power pad. Underside power pad must be directly connected to ground plane of the board.

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6.4 Thermal Information

THERMAL METRIC(1)		TPS65988 RSH (QFN) 48 PINS	UNIT
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance	36.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	°C/W
$R_{\theta JB}$(2)	Junction-to-board thermal resistance	13.7	°C/W
ψ_{JT}(2)	Junction-to-top characterization parameter	11.3	°C/W
ψ_{JB}(2)	Junction-to-board characterization parameter	13.6	°C/W
$R_{\theta JC(bot_Controller)}$	Junction-to-case (bottom GND pad) thermal resistance	0.7	°C/W
$R_{\theta JC(bot_FET)}$	Junction-to-case (bottom DRAIN1/2 pad) thermal resistance	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Thermal metrics are not JDEC standard values and are based on the TPS65988 evaluation board.

6.5 Power Supply Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL						
V_{IN_3V3}	Input 3.3-V supply		3.135	3.3	3.45	V
PP_CABLE	Input to power Vconn output on C_CC pins		2.95	5	5.5	V
PP_HV	Source power from PP_HV to VBUS		4.5	5	22	V
VBUS	Sink power from VBUS to PP_HV		4	5	22	V
C_{VIN_3V3}	Recommended capacitance on the VIN_3V3 pin		5	10		µF
C_{PP_CABLE}	Recommended capacitance on PPx_CABLE pins		2.5	4.7		µF
$C_{PP_HV_SRC}$	Recommended capacitance on PP_HVx pin when configured as a source		2.5	4.7		µF
$C_{PP_HV_SNK}$	Recommended capacitance on PP_HVx pin when configured as a sink		1	47	120	µF
C_{VBUS}	Recommended capacitance on VBUSx pins		0.5	1	12	µF
INTERNAL						
V_{LDO_3V3}	Output voltage of LDO from VBUS to LDO_3V3	VIN_3V3 = 0 V, VBUS1 ≥ 4 V, 0 ≤ I_{LOAD} ≤ 50mA	3.15	3.3	3.45	V
$V_{DO_LDO_3V3}$	Drop out voltage of LDO_3V3 from VBUS	I_{LOAD} = 50mA	250	500	850	mV
$I_{LDO_3V3_EX}$	Allowed External Load current on LDO_3V3 pin				25	mA
V_{LDO_1V8}	Output voltage of LDO_1V8	0 ≤ I_{LOAD} ≤ 20mA	1.75	1.8	1.85	V
V_{FWD_DROP}	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	I_{LOAD} = 50 mA			200	mV
C_{LDO_3V3}	Recommended capacitance on LDO_3V3 pin		5	10	25	µF
C_{LDO_1V8}	Recommended capacitance on LDO_1V8 pin		2.2	4.7	6	µF
SUPERVISORY						
UV_LDO3V3	Undervoltage threshold for LDO_3V3. Locks out 1.8-V LDOs	LDO_3V3 rising	2.2	2.325	2.45	V
UVH_LDO3V3	Undervoltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_PCBL	Undervoltage threshold for PP_CABLE	PP_CABLE rising	2.5	2.625	2.75	V

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Power Supply Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVH_PCBL	Undervoltage hysteresis for PP_PCABLE	PP_CABLE falling	20	50	80	mV
OV_VBUS	Overvoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS rising	5		24	V
OVLSB_VBUS	Overvoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS rising		328		mV
OVH_VBUS	Overvoltage hysteresis for VBUS	VBUS falling, % of OV_VBUS	1.4	1.65	1.9	%
UV_VBUS	Undervoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS falling	2.5		18.21	V
UVLSB_VBUS	Undervoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS falling		249		mV
UVH_VBUS	Undervoltage hysteresis for VBUS	VBUS rising, % of UV_VBUS	0.9	1.3	1.7	%

6.6 Power Consumption Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VIN_3V3} (1)	Sleep (Sink)	VIN_3V3 = 3.3 V, VBUS = 0 V, No cables connected, T_j = 25C, configured as sink, BC1.2 disabled		45		µA
	Sleep (Source/DRP)	VIN_3V3 = 3.3 V, VBUS = 0 V, No cables connected, T_j = 25C, configured as source or DRP, BC1.2 disabled		55		µA
I_{VIN_3V3} (1)	Idle (Attached)	VIN_3V3 = 3.3 V, Cables connected, No active PD communication, T_j = 25C		5		mA
I_{VIN_3V3} (1)	Active	VIN_3V3 = 3.3 V, T_j = 25C		8		mA

(1) Does not include current draw due to GPIO loading

6.7 Power Switch Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PPCC}	PP_CABLE to C_CCn power switch resistance	4.7 ≤ PP_CABLE ≤ 5.5		222	325	mΩ
		2.95 ≤ PP_CABLE < 4.7		269	414	mΩ
R_{PPHV}	PP_HVx to VBUSx power switch resistance	Tj = 25C		25	33	mΩ
I_{PPHV}	Continuous current capabillity of power path from PP_HVx to VBUSx	T_A < 60C (1)			5	A
I_{PPCC}	Continuous current capabillity of power path from PP_CABLEx to Cx_CCn	T_J = 125C			320	mA
		T_J = 85C			600	mA
I_{HVACT}	Active quiescent current from PP_HV pin, EN_HV = 1	Source Configuration, Comparator RCP function enabled, I_{LOAD} = 100mA			1	mA
I_{HVSD}	Shutdown quiescent current from PP_HV pin, EN_HV = 0	V_{PPHV} = 20V			100	µA

(1) Allowable ambient temperature is dependant on device board layout. Junction temperature of PPHV switch may not exceed 150C.

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Power Switch Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCC}	Over Current Clamp Firmware Selectable Settings		1.140	1.267	1.393	A
			1.380	1.533	1.687	A
			1.620	1.800	1.980	A
			1.860	2.067	2.273	A
			2.100	2.333	2.567	A
			2.34	2.600	2.860	A
			2.580	2.867	3.153	A
			2.820	3.133	3.447	A
			3.060	3.400	3.74	A
			3.300	3.667	4.033	A
			3.540	3.933	4.327	A
			3.780	4.200	4.620	A
			4.020	4.467	4.913	A
			4.260	4.733	5.207	A
			4.500	5.00	5.500	A
			4.740	5.267	5.793	A
			4.980	5.533	6.087	A
			5.220	5.800	6.380	A
			5.460	6.067	6.673	A
			5.697	6.330	6.963	A
I_{OCP}	PP_HV Quick Response Current Limit			10		A
$I_{LIMPPCC}$	PP_CABLE current limit		0.6	0.75	0.9	A
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I = 100 mA, Reverse current blocking disabled	3.9	6	8.1	A/V
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I = 200 mA	4.8	6	7.2	A/V
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I = 500 mA	5.28	6	6.72	A/V
$I_{HV_ACC\ 1}$	PP_HV current sense accuracy	I ≥ 1 A	5.4	6	6.6	A/V
t_{ON_HV}	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage	Configured as a source or as a sink with soft start disabled. PP_HV = 20 V, CVBUS = 10 µF, I_{LOAD} = 100 mA			8	ms
t_{ON_FRS}	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage during an FRS enable	Configured as a source. PP_HV = 5 V, CVBUS = 10 µF, I_{LOAD} = 100 mA			150	µs
t_{ON_CC}	PP_CABLE path turn on time from enable to C_CCn = 95% of the PP_CABLE voltage	PP_CABLE = 5 V, C_CCn = 500 nF, I_{LOAD} = 100 mA			2	ms
SS	Configurable soft start slew rate for sink configuration	I_{LOAD} = 100mA, setting 0	0.270	0.409	0.45	V/ms
		I_{LOAD} = 100mA, setting 1	0.6	0.787	1	V/ms
		I_{LOAD} = 100mA, setting 2	1.2	1.567	1.7	V/ms
		I_{LOAD} = 100mA, setting 3	2.3	3.388	3.6	V/ms
V_{REVPHV}	Reverse current blocking voltage threshold for PP_HV switch	Diode Mode		6	10	mV
		Comparator Mode		3	6	mV
V_{SAFE0V}	Voltage that is a safe 0 V per USB-PD specification		0		0.8	V
t_{SAFE0V}	Voltage transition time to VSAFE0V				650	ms
SRPOS	Maximum slew rate for positive voltage transitions				0.03	V/µs

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Power Switch Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SRNEG	Maximum slew rate for negative voltage transitions		–0.03			V/µs
t_{STABLE}	EN to stable time for both positive and negative voltage transitions				275	ms
$V_{SRCVALID}$	Supply output tolerance beyond V_{SRCNEW} during time t_{STABLE}		–0.5		0.5	V
V_{SRCNEW}	Supply output tolerance		–5		5	%
$t_{VCONNDIS}$	Time from cable detach to VVCONNDIS				250	ms
$V_{VCONNDIS}$	Voltage at which V_{CONN} is considered discharged				150	mV

6.8 Cable Detection Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{H_CC_USB}$	Source Current through each C_CC pin when in a disconnected state and Configured as a Source advertising Default USB current to a peripheral device		73.6	80	86.4	µA
$I_{H_CC_1P5}$	Source Current through each C_CC pin when in a disconnected state when Configured as a Source advertising 1.5A to a UFP		165.6	180	194.4	µA
$I_{H_CC_3P0}$	Source Current through each C_CC pin when in a disconnected state and Configured as a Source advertising 3.0A to a UFP.	VIN_3V3 ≥ 3.135 V, V_{CC} < 2.6 V	303.6	330	356.4	µA
$V_{D_CCH_USB}$	Voltage Threshold for detecting a Source attach when configured as a Sink and the Source is advertising Default USB current source capability		0.15	0.2	0.25	V
$V_{D_CCH_1P5}$	Voltage Threshold for detecting a Source advertising 1.5A source capability when configured as a Sink		0.61	0.66	0.7	V
$V_{D_CCH_3P0}$	Voltage Threshold for detecting a Source advertising 3A source capability when configured as a Sink		1.16	1.23	1.31	V
$V_{H_CCD_USB}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising Default USB current source capability.	IH_CC = IH_CC_USB	1.5	1.55	1.65	V
$V_{H_CCD_1P5}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising 1.5A source capability	IH_CC = IH_CC_1P5	1.5	1.55	1.65	V
$V_{H_CCD_3P0}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising 3.0A source capability.	IH_CC = IH_CC_3P0 VIN_3V3 ≥ 3.135V	2.45	2.55	2.615	V
$V_{H_CCA_USB}$	Voltage Threshold for detecting an active cable attach when configured as a Source and advertising Default USB current capability.		0.15	0.2	0.25	V
$V_{H_CCA_1P5}$	Voltage Threshold for detecting active cables attach when configured as a Source and advertising 1.5A capability.		0.35	0.4	0.45	V
$V_{H_CCA_3P0}$	Voltage Threshold for detecting active cables attach when configured as a Source and advertising 3A capability.		0.75	0.8	0.85	V
R_{D_CC}	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a Sink. LDO_3V3 powered.	V = 1V, 1.5V	4.59	5.1	5.61	kΩ

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Cable Detection Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{D_CC_OPEN}$	Pulldown resistance through each C_CC pin when in a disabled state. LDO_3V3 powered.	V = 0V to LDO_3V3	500			kΩ
R_{D_DB}	Pulldown resistance through each C_CC pin when LDO_3V3 unpowered	V = 1.5V, 2.0V	4.08	5.1	6.12	kΩ
R_{FRSWAP}	Fast Role Swap signal pull down				5	Ω
V_{TH_FRS}	Fast role swap request detection voltage threshold		490	520	550	mV

6.9 USB-PD Baseband Signal Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
PD_BITRATE	PD data bit rate		270	300	330	Kbps
UI (1)	Unit interval (1/PD_BITRATE)		3.03	3.33	3.7	µs
CCBLPLUG (2)	Capacitance for a cable plug (each plug on a cable may have up to this value)				25	pF
ZCABLE	Cable characteristic impedance		32		65	Ω
CRECEIVER (3)	Receiver capacitance. Capacitance looking into Cx_CCn pin when in receiver mode.			100		pF
TRANSMITTER						
ZDRIVER	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750kHz) while the source is driving the C_CCn line.		33		75	Ω
t_{RISE}	Rise time. 10 % to 90 % amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
t_{FALL}	Fall time. 90 % to 10 % amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
V_{TX}	Transmit high voltage		1.05	1.125	1.2	V
RECEIVER						
V_{RXTR}	Rx receive rising input threshold	Port configured as Source	840	875	910	mV
V_{RXTR}	Rx receive rising input threshold	Port configured as Sink	504	525	546	mV
V_{RXTF}	Rx receive falling input threshold	Port configured as Sink	240	250	260	mV
V_{RXTF}	Rx receive falling input threshold	Port configured as Source	576	600	624	mV
NCOUNT	Number of transitions for signal detection (number to count to detect non-idle bus).		3			
TTRANWIN	Time window for detecting non-idle bus.		12		20	µs

(1) UI denotes the time to transmit an unencoded data bit not the shortest high or low times on the wire after encoding with BMC. A single data bit cell has duration of 1 UI, but a data bit cell with value 1 will contain a centrally place 01 or 10 transition in addition to the transition at the start of the cell.
(2) The capacitance of the bulk cable is not included in the CCBLPLUG definition. It is modeled as a transmission line.
(3) CRECEIVER includes only the internal capacitance on a C_CCn pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications. TI recommends adding capacitance to bring the total pin capacitance to 300 pF for improved TX behavior.

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USB-PD Baseband Signal Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZBMCRX	Receiver input impedance	Does not include pull-up or pulldown resistance from cable detect. Transmitter is Hi-Z.	5			MΩ
TRXFILTER (4)	Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingression		100			ns

(4) Broadband noise ingression is because of coupling in the cable interconnect.

6.10 BC1.2 Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA CONTACT DETECT						
ID_{P_SRC}	DCD source current	LDO_3V3 = 3.3 V	7	10	13	µA
R_{DM_DWN}	DCD pulldown resistance		14.25	20	24.8	kΩ
R_{DP_DWN}	DCD pulldown resistance		14.25	20	24.8	kΩ
V_{LGC_HI}	Threshold for no connection	Cx_USB_P ≥ VLGC_HI, LDO_3V3 = 3.3 V	2			V
V_{LGC_LO}	Threshold for connection	Cx_USB_P ≤ VLGC_LO			0.8	V
PRIMARY AND SECONDARY DETECT						
V_{DX_SRC}	Source voltage		0.55	0.6	0.65	V
VDX_ILIM	VDX_SRC current limit		250		400	µA
I_{DX_SNK}	Sink Current	VC_USB_TN/BN ≥ 250 mV	25	75	125	µA
R_{DCP_DAT}	Dedicated Charging Port Resistance				200	Ω
DIVIDER MODE						
VCx_USB_P_2.7V	Cx_USB_P Output Voltage	No load on Cx_USB_P	2.57	2.7	2.79	V
VCx_USB_N_2.7V	Cx_USB_N Output Voltage	No load on Cx_USB_N	2.57	2.7	2.79	V
RCx_USB_P_30k	Cx_USB_P Output Impedance	5µA pulled from Cx_USB_P pin	24	30	36	kΩ
RCx_USB_N_30k	Cx_USB_N Output Impedance	5µA pulled from Cx_USB_N pin	24	30	36	kΩ
1.2V MODE						
RCx_USB_N_102k	Cx_USB_N Output Impedance	5µA pulled from Cx_USB_N pin	80	102	130	kΩ
VCx_USB_P_1.2V	Cx_USB_P Output Voltage	No load on Cx_USB_P	1.12	1.2	1.28	V
VCx_USB_N_1.2V	Cx_USB_N Output Voltage	No load on Cx_USB_N	1.12	1.2	1.28	V
RCx_USB_P_102k	Cx_USB_P Output Impedance	5µA pulled from Cx_USB_P pin	80	102	130	kΩ

6.11 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Thermal Shutdown Temperature of the main thermal shutdown	Temperature rising	145	160	175	°C
T_{SDH_MAIN}	Thermal Shutdown hysteresis of the main thermal shutdown	Temperature falling		20		°C

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Thermal Shutdown Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_PWR}	Thermal Shutdown Temperature of the power path block	Temperature rising	145	160	175	°C
T_{SDH_PWR}	Thermal Shutdown hysteresis of the power path block	Temperature falling		20		°C

6.12 Oscillator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC_24M}	24-MHz oscillator		22.8	24	25.2	MHz
f_{OSC_100K}	100-kHz oscillator		95	100	105	kHz

6.13 I/O Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
SPI_VIH	High-level input voltage	LDO_1V8 = 1.8V	1.3			V
SPI_VIL	Low input voltage	LDO_1V8 = 1.8V			0.63	V
SPI_HYS	Input hysteresis voltage	LDO_1V8 = 1.8V	0.09			V
SPI_ILKG	Leakage current	Output is Hi-Z, VIN = 0 to LDO_3V3	-1		1	µA
SPI_VOH	SPI output high voltage	IO = –2 mA, LDO_3V3 = 3.3 V	2.88			V
SPI_VOL	SPI output low voltage	IO = 2 mA			0.4	V
SWDIO						
SWDCLK						
GPIO						
GPIO_VIH	High-level input voltage	LDO_1V8 = 1.8 V	1.3			V
GPIO_VIL	Low input voltage	LDO_1V8 = 1.8 V			0.63	V
GPIO_HYS	Input hysteresis voltage	LDO_1V8 = 1.8 V	0.09			V
GPIO_ILKG	I/O leakage current	INPUT = 0 V to VDD	–1		1	µA
GPIO_RPU	Pullup resistance	Pullup enabled	50	100	150	kΩ
GPIO_RPD	Pulldown resistance	Pulldown enabled	50	100	150	kΩ
GPIO_DG	Digital input path deglitch			20		ns
GPIO_VOH	GPIO output high voltage	IO = –2 mA, LDO_3V3 = 3.3 V	2.88			V
GPIO_VOL	GPIO output low voltage	IO = 2 mA, LDO_3V3 = 3.3 V			0.4	V
I2C_IRQx						
OD_VOL	Low-level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, VIN = 0 to LDO_3V3	–1		1	µA

6.14 I²C Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA AND SCL COMMON CHARACTERISTICS						
I_{LEAK}	Input leakage current	Voltage on Pin = LDO_3V3	–3		3	µA
V_{OL}	SDA output low voltage	I_{OL} = 3 mA, LDO_3V3 = 3.3 V			0.4	V
I_{OL}	SDA max output low current	V_{OL} = 0.4 V	3			mA
		V_{OL} = 0.6 V	6			mA

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I²C Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low signal	LDO_3V3 = 3.3 V			0.99	V
		LDO_1V8 = 1.8 V			0.54	V
V_{IH}	Input high signal	LDO_3V3 = 3.3 V	2.31			V
		LDO_1V8 = 1.8 V	1.3			V
V_{HYS}	Input hysteresis	LDO_3V3 = 3.3 V	0.17			V
		LDO_1V8 = 1.8 V	0.09			V
t_{SP}	I²C pulse width suppressed				50	ns
C_I	Pin capacitance				10	pF
SDA AND SCL STANDARD MODE CHARACTERISTICS						
f_{SCL}	I²C clock frequency		0		100	kHz
t_{HIGH}	I²C clock high time		4			µs
t_{LOW}	I²C clock low time		4.7			µs
$t_{SU;DAT}$	I²C serial data setup time		250			ns
$t_{HD;DAT}$	I²C serial data hold time		0			ns
$t_{VD;DAT}$	I²C valid data time	SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.45	µs
t_{OCF}	I²C output fall time	10 pF to 400 pF bus			250	ns
t_{BUF}	I²C bus free time between stop and start		4.7			µs
$t_{SU;STA}$	I²C start or repeated Start condition setup time		4.7			µs
$t_{HD;STA}$	I²C Start or repeated Start condition hold time		4			µs
$t_{SU;STO}$	I²C Stop condition setup time		4			µs
SDA AND SCL FAST MODE CHARACTERISTICS						
f_{SCL}	I²C clock frequency	Configured as Slave	0		400	kHz
f_{SCL_MASTER}	I²C clock frequency	Configured as Master	0	320	400	kHz
t_{HIGH}	I²C clock high time		0.6			µs
t_{LOW}	I²C clock low time		1.3			µs
$t_{SU;DAT}$	I²C serial data setup time		100			ns
$t_{HD;DAT}$	I²C serial data hold time		0			ns
$t_{VD;DAT}$	I²C Valid data time	SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	I²C Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			0.9	µs
t_{OCF}	I²C output fall time	10 pF to 400 pF bus, V_{DD} = 3.3 V	12		250	ns
		10 pF to 400 pF bus, V_{DD} = 1.8 V	6.5		250	ns
t_{BUF}	I²C bus free time between stop and start		1.3			µs
$t_{SU;STA}$	I²C start or repeated Start condition setup time		0.6			µs
$t_{HD;STA}$	I²C Start or repeated Start condition hold time		0.6			µs
$t_{SU;STO}$	I²C Stop condition setup time		0.6			µs

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6.15 SPI Master Timing Requirements

			MIN	NOM	MAX	UNIT
f_{SPI}	Frequency of SPI_CLK		11.4	12	12.6	MHz
t_{PER}	Period of SPI_CLK (1/F_SPI)		79.36	83.33	87.72	ns
t_{WHI}	SPI_CLK high width		30			ns
t_{WLO}	SPI_CLK low width		30			ns
t_{DACT}	SPI_SZZ falling to SPI_CLK rising delay time		30		50	ns
t_{DINACT}	SPI_CLK falling to SPI_SSZ rising delay time		158		180	ns
t_{DMOSI}	SPI_CLK falling to SPI_MOSI Valid delay time		–10		10	ns
t_{SUMISO}	SPI_MISO valid to SPI_CLK falling setup time		33			ns
t_{HDMSIO}	SPI_CLK falling to SPI_MISO invalid hold time		0			ns
t_{RIN}	SPI_MISO input rise time				5	ns
t_{RSPI}	SPI_SSZ/CLK/MOSI rise time	10% to 90%, C_L = 5 to 50 pF, LDO_3V3 = 3.3 V	1		25	ns
t_{FSPI}	SPI_SSZ/CLK/MOSI fall time	90% to 10%, C_L = 5 to 50 pF, LDO_3V3 = 3.3 V	1		25	ns

6.16 HPD Timing Requirements

			MIN	NOM	MAX	UNIT
DP SOURCE SIDE (HPD TX)						
t_{IRQ_MIN}	HPD IRQ minimum assert time		675	750	825	µs
t_{2MS_MIN}	HPD assert 2-ms min time		3	3.33	3.67	ms
DP SINK SIDE (HPD RX)						
t_{HPD_HDB}	HPD high debounce time	HPD_HDB_SEL = 0	300	375	450	µs
		HPD_HDB_SEL = 1	100	111	122	ms
t_{HPD_LDB}	HPD low debounce time		300	375	450	µs
t_{HPD_IRQ}	HPD IRQ limit time		1.35	1.5	1.65	ms

6.17 Typical Characteristics

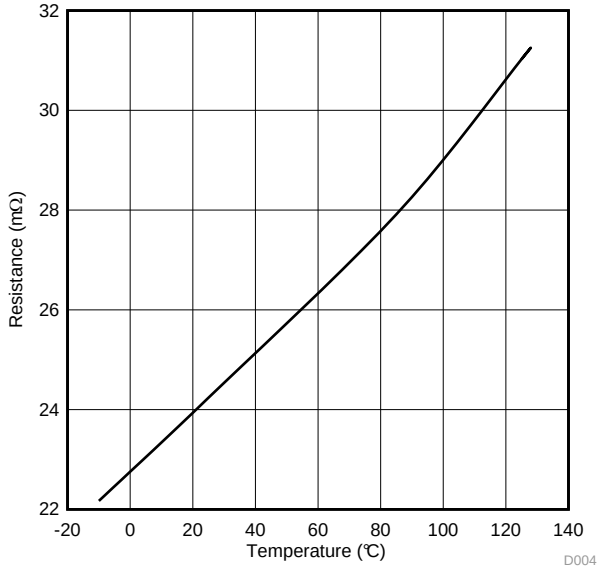


Figure 1. PPHVx Rdson vs Junction Temperature

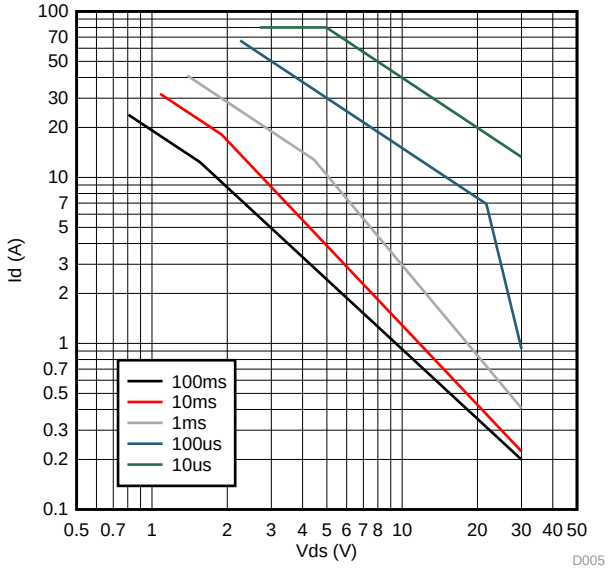


Figure 2. PPHVx SOA Curve

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7 Parameter Measurement Information

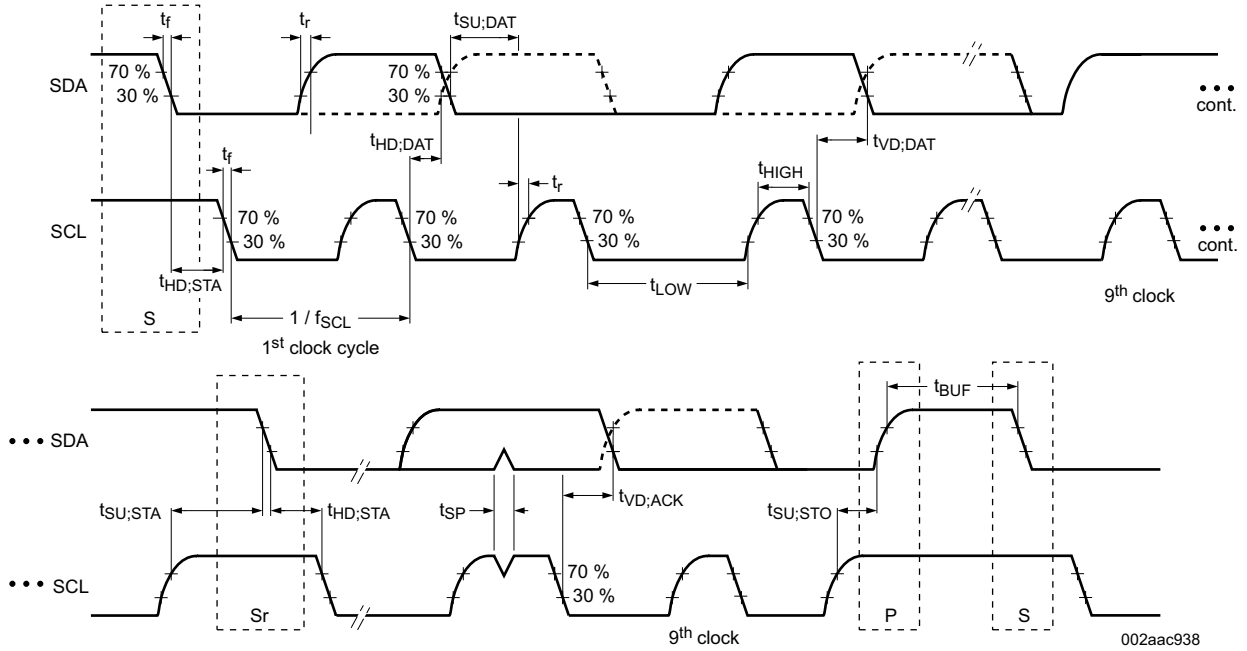


Figure 3. I²C Slave Interface Timing

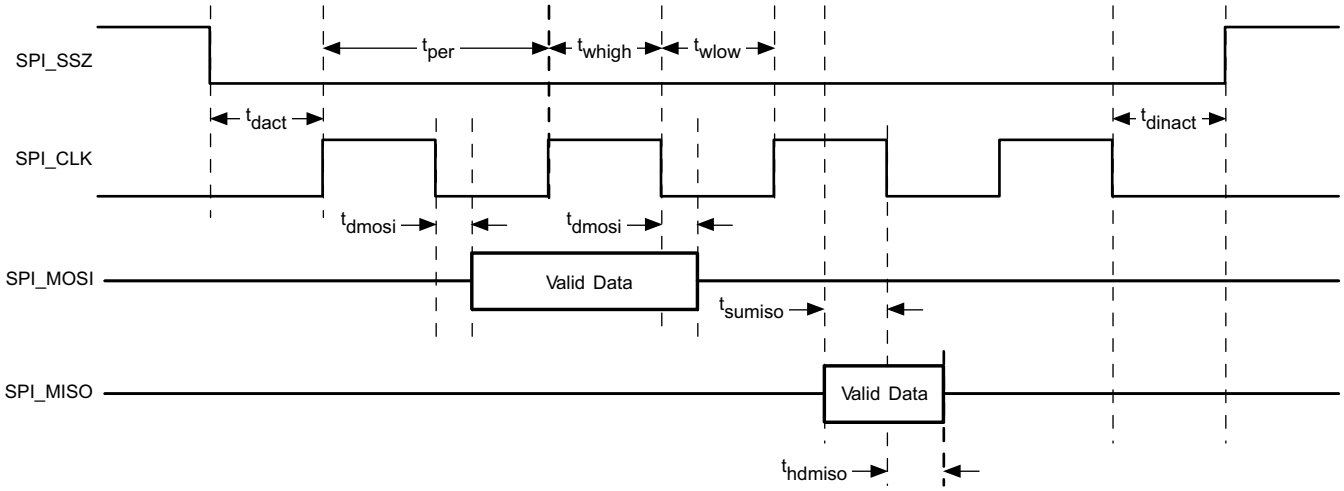


Figure 4. SPI Master Timing

8 Detailed Description

8.1 Overview

The TPS65988DJ is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for two USB Type-C and PD plug or receptacles. The TPS65988DJ communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port power switch, controls an external high current port power switch and negotiates alternate modes for each port. The TPS65988DJ may also control an attached super-speed multiplexer via GPIO or I^2C to simultaneously support USB3.0/3.1 data rates and DisplayPort video.

Each Type-C port controlled by the TPS65988DJ is functionally identical and supports the full range of the USB Type-C and PD standards.

The TPS65988DJ is divided into five main sections:

- USB-PD controller
- cable plug and orientation detection circuitry
- port power switches
- power management circuitry
- digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the C_CC1 pin or the C_CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features and more detailed circuitry, see the *USB-PD Physical Layer* section.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see .

The port power switches provide power to the system port through the VBUS pin and also through the C_CC1 or C_CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, see the *Port Power Switches* section.

The power management circuitry receives and provides power to the TPS65988DJ internal circuitry and to the LDO_3V3 output. For a high-level block diagram of the power management circuitry, a description of its features and more detailed circuitry, see the *Power Management* section.

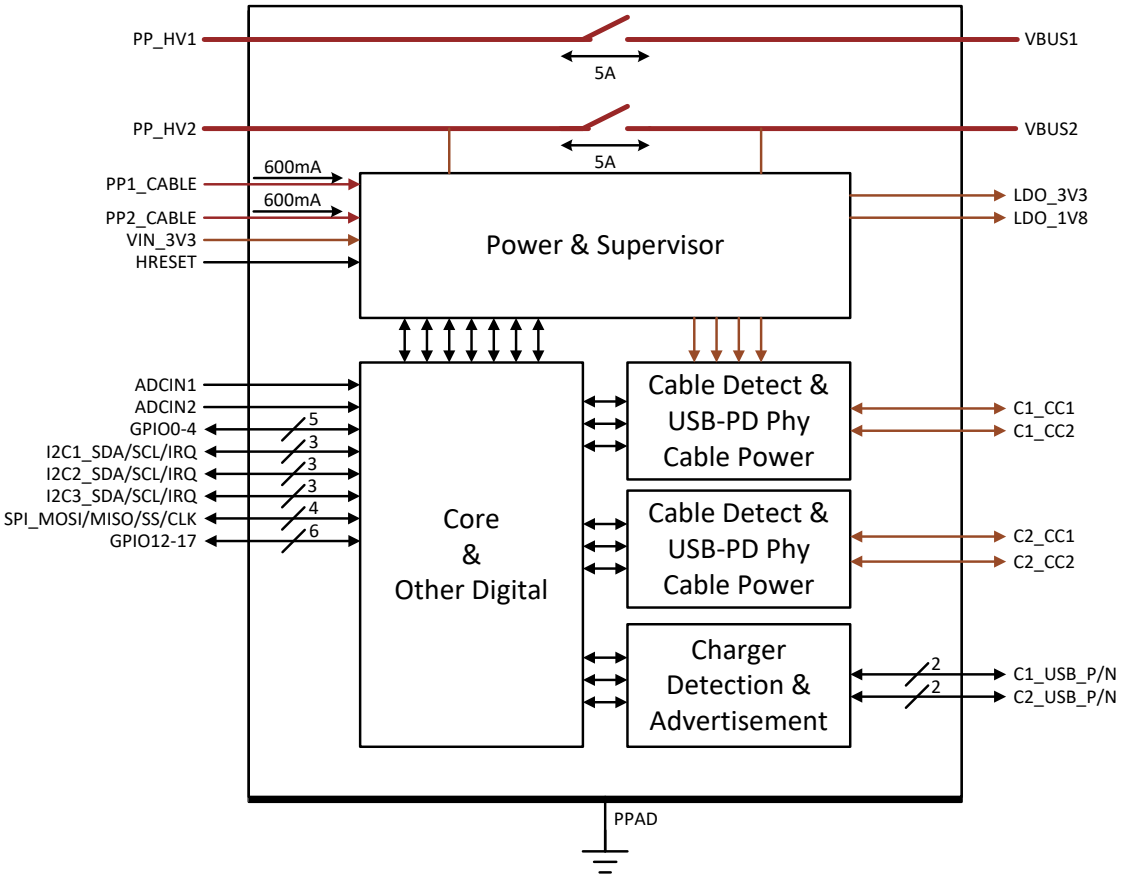
The digital core provides the engine for receiving, processing and sending all USB-PD packets as well as handling control of all other TPS65988DJ functionality. A portion of the digital core contains ROM memory which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM called boot code, is capable of initializing the TPS65988DJ, loading of device configuration information and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features and more detailed circuitry, see the *Digital Core* section.

The TPS65988DJ is an I^2C slave to be controlled by a host processor (see the *I^2C Interfaces* section), and an SPI master to write to and read from an optional external flash memory (see the *SPI Master Interface* section).

The TPS65988DJ also integrates a thermal shutdown mechanism (see the*Thermal Shutdown* section) and runs off of accurate clocks provided by the integrated oscillators (see the *Oscillators* section).

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB-PD Physical Layer

Figure 5 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block. This block is duplicated for the second TPS65988DJ port.

Feature Description (continued)

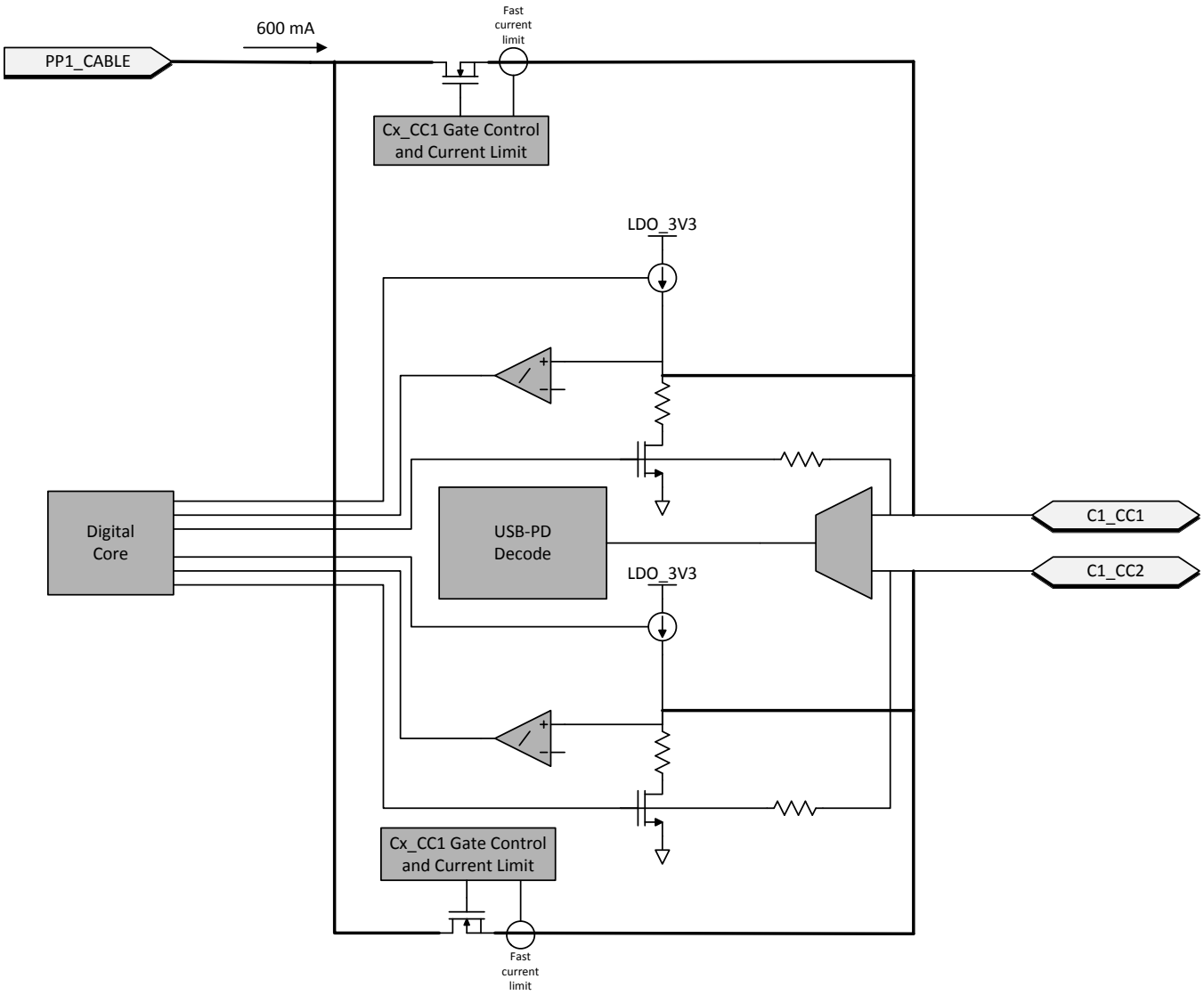


Figure 5. USB-PD Physical Layer, Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (Cx_CC1 or Cx_CC2) that is DC biased due to the DFP (or UFP) cable attach mechanism shown in .

8.3.1.1 USB-PD Encoding and Signaling

Figure 6 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 7 illustrates the high-level block diagram of the baseband USB-PD receiver.

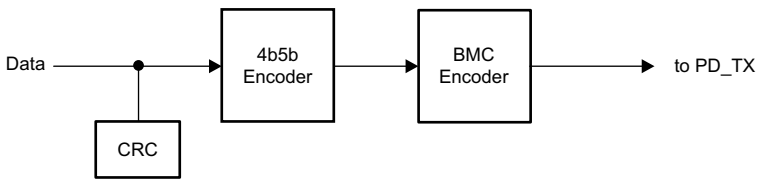


Figure 6. USB-PD Baseband Transmitter Block Diagram

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Feature Description (continued)

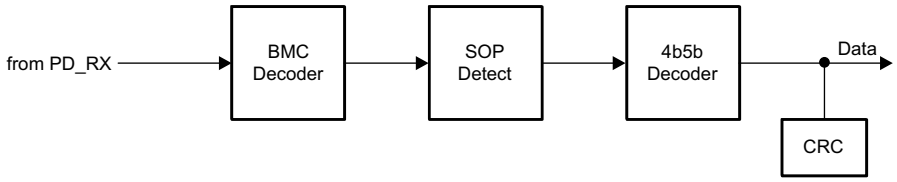


Figure 7. USB-PD Baseband Receiver Block Diagram

The USB-PD baseband signal is driven on the Cx_CCn pins with a tri-state driver. The tri-state driver is slew rate limited to reduce the high frequency components imparted on the cable and to avoid interference with frequencies used for communication.

8.3.1.2 USB-PD Bi-Phase Marked Coding

The USBP-PD physical layer implemented in the TPS65988DJ is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 8 illustrates Biphase Mark Coding.

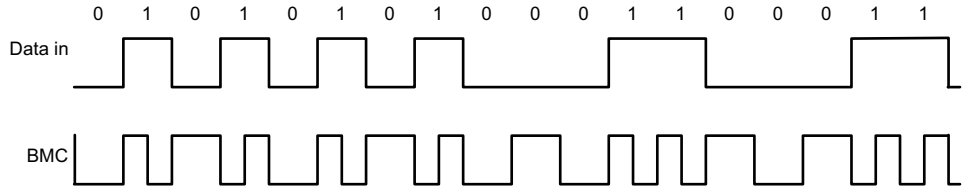


Figure 8. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the Cx_CC1 or Cx_CC2 pins with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

8.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

8.3.1.4 USB-PD BMC Transmitter

The TPS65988DJ transmits and receives USB-PD data over one of the Cx_CCn pins for a given CC pin pair (one pair per USB Type-C port). The Cx_CCn pins are also used to determine the cable orientation (see) and maintain the cable/device attach detection. Thus, a DC bias exists on the Cx_CCn pins. The transmitter driver overdrives the Cx_CCn DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the Cx_CCn pin when not transmitting. Figure 9 shows the USB-PD BMC TX and RX driver block diagram.

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Feature Description (continued)

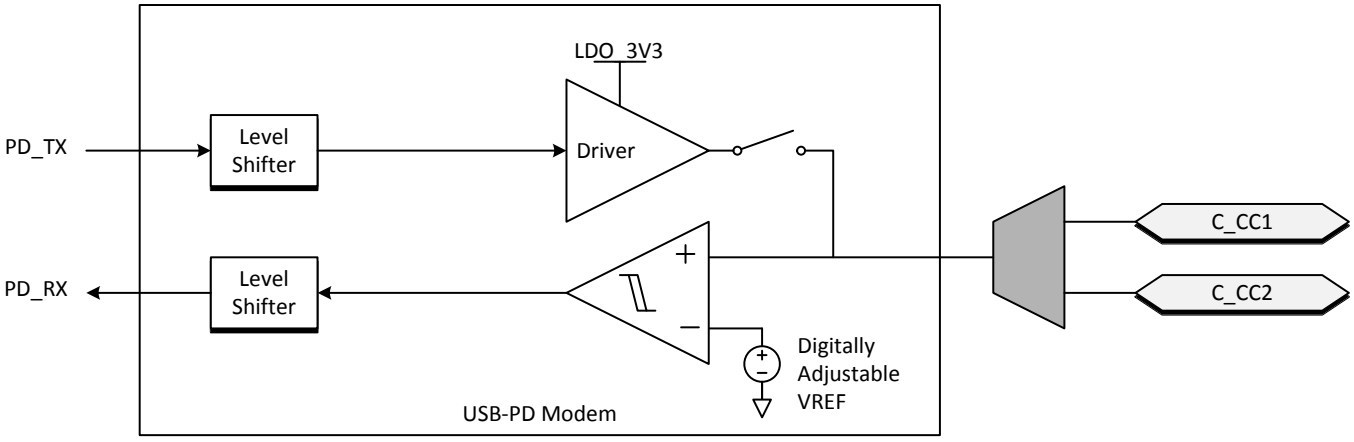


Figure 9. USB-PD BMC TX/Rx Block Diagram

Figure 10 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum threshold for detecting a UFP attach (VD_CCH_USB) and the maximum threshold for detecting a UFP attach to a DFP (VD_CCH_3P0). This means that the DC bias can be below VOH of the transmitter driver or above VOH.

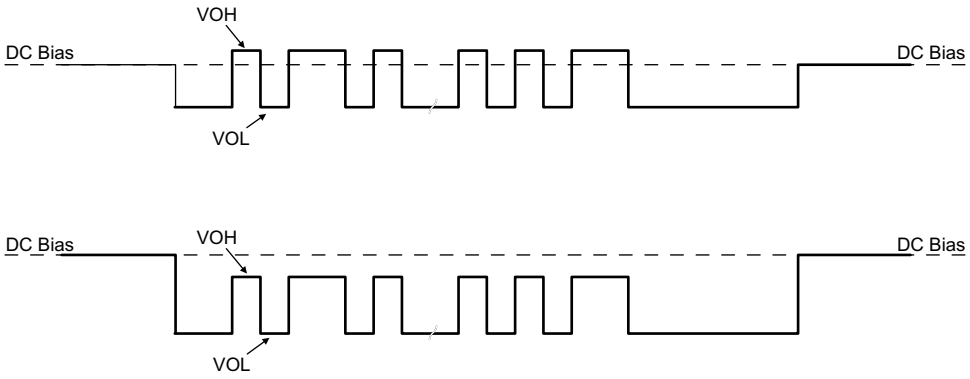


Figure 10. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the Cx_CCn lines. The signal peak, VTXP, is set to meet the TX masks defined in the *USB-PD Specifications*.

When driving the line, the transmitter driver has an output impedance of ZDRIVER. ZDRIVER is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. ZDRIVER impacts the noise ingression in the cable.

Figure 11 shows the simplified circuit determining ZDRIVER. It is specified such that noise at the receiver is bounded.

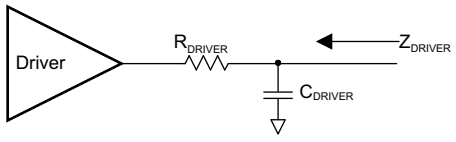


Figure 11. ZDRIVER Circuit

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Feature Description (continued)

8.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS65988DJ receives a signal that falls within the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Figure 12 shows an example of a multi-drop USB-PD connection. This connection has the typical UFP (device) to DFP (host) connection, but also includes cable USB-PD TX/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (ZBMCRX). The USB-PD Specification also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

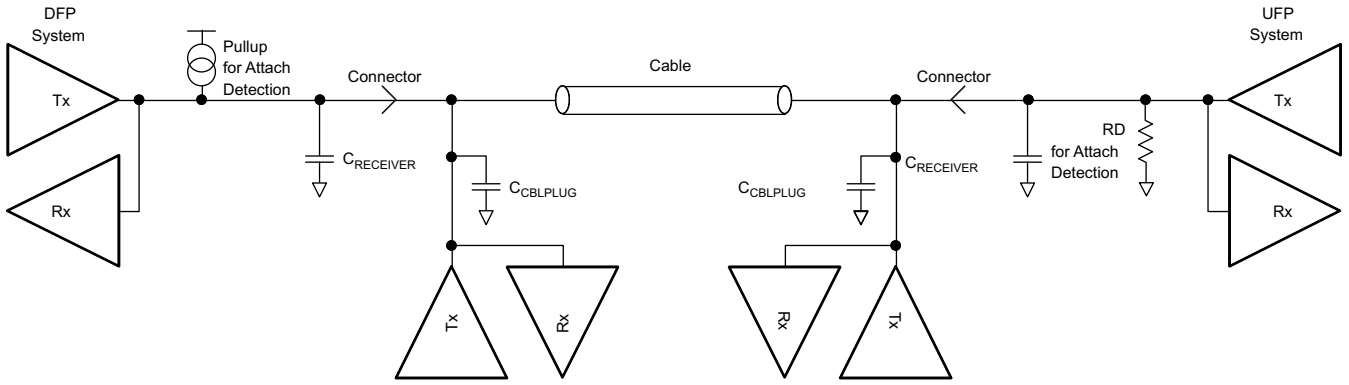


Figure 12. Example USB-PD Multi-Drop Configuration

8.3.2 Power Management

The TPS65988DJ power management block receives power and generates voltages to provide power to the TPS65988DJ internal circuitry. These generated power rails are LDO_3V3 and LDO_1V8. LDO_3V3 may also be used as a low power output for external flash memory. The power supply path is shown in Figure 13.

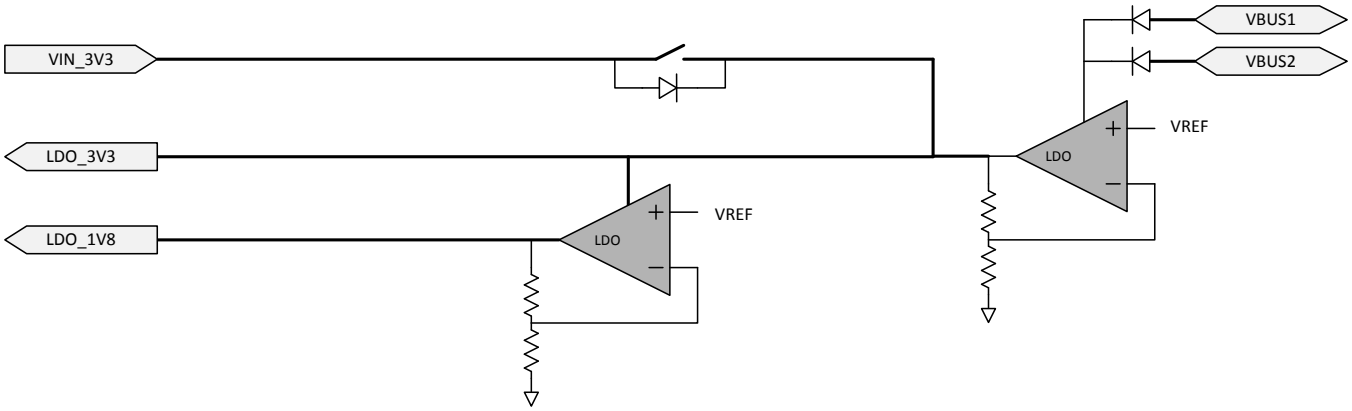


Figure 13. Power Supplies

The TPS65988DJ is powered from either VIN_3V3, VBUS1, or VBUS2. The normal power supply input is VIN3V3. In this mode, current flows from VIN_3V3 to LDO3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V8 to power the 1.8-V core digital circuitry. When VIn_3V3 power is unavailable and power is available on VBUS1 or VBUS2 , the TPS65988DJ is powered from VBUS. In this mode, the voltage on VBUS1 or VBUS 2 is stepped down through an LDO to LDO_3V3.

8.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

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Feature Description (continued)

8.3.2.2 VBUS LDO

The TPS65988DJ contains an internal high-voltage LDO which is capable of converting up to 22 V from VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used during dead battery operation while the VIN_3V3 supply is not present. The VBUS LDO may be powered from either VBUS1 or VBUS2. The path connecting each VBUS to the internal LDO blocks reverse current, preventing power on one VBUS from leaking to the other. When power is present on both VBUS inputs, the internal LDO draws current from both VBUS pins.

8.3.2.3 Supply Switch Over

VIN_3V3 takes precedence over VBUS, meaning that when both supply voltages are present the TPS65988DJ powers from VIN_3V3. See Figure 13 for a diagram showing the power supply path block. There are two cases in which a power supply switch-over occurs. The first is when VBUS is present first and then VIN_3V3 becomes available. In this case, the supply automatically switches over to VIN_3V3 and brown-out prevention is verified by design. The other way a supply switch-over occurs is when both supplies are present and VIN_3V3 is removed and falls below 2.85 V. In this case, a hard reset of the TPS65988DJ is initiated by device firmware, prompting a re-boot.

8.3.3 Port Power Switches

The figure below shows the TPS65988DJ internal power paths. The TPS65988DJ features two internal high-voltage power paths. Each path contains two back to back common drain N-Fets, current monitor, overvoltage monitor, undervoltage monitor, and temperature sensing circuitry. Each path may conduct up to 5 A safely. Additional external paths may be controlled through the TPS65988DJ GPIOs.

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Feature Description (continued)

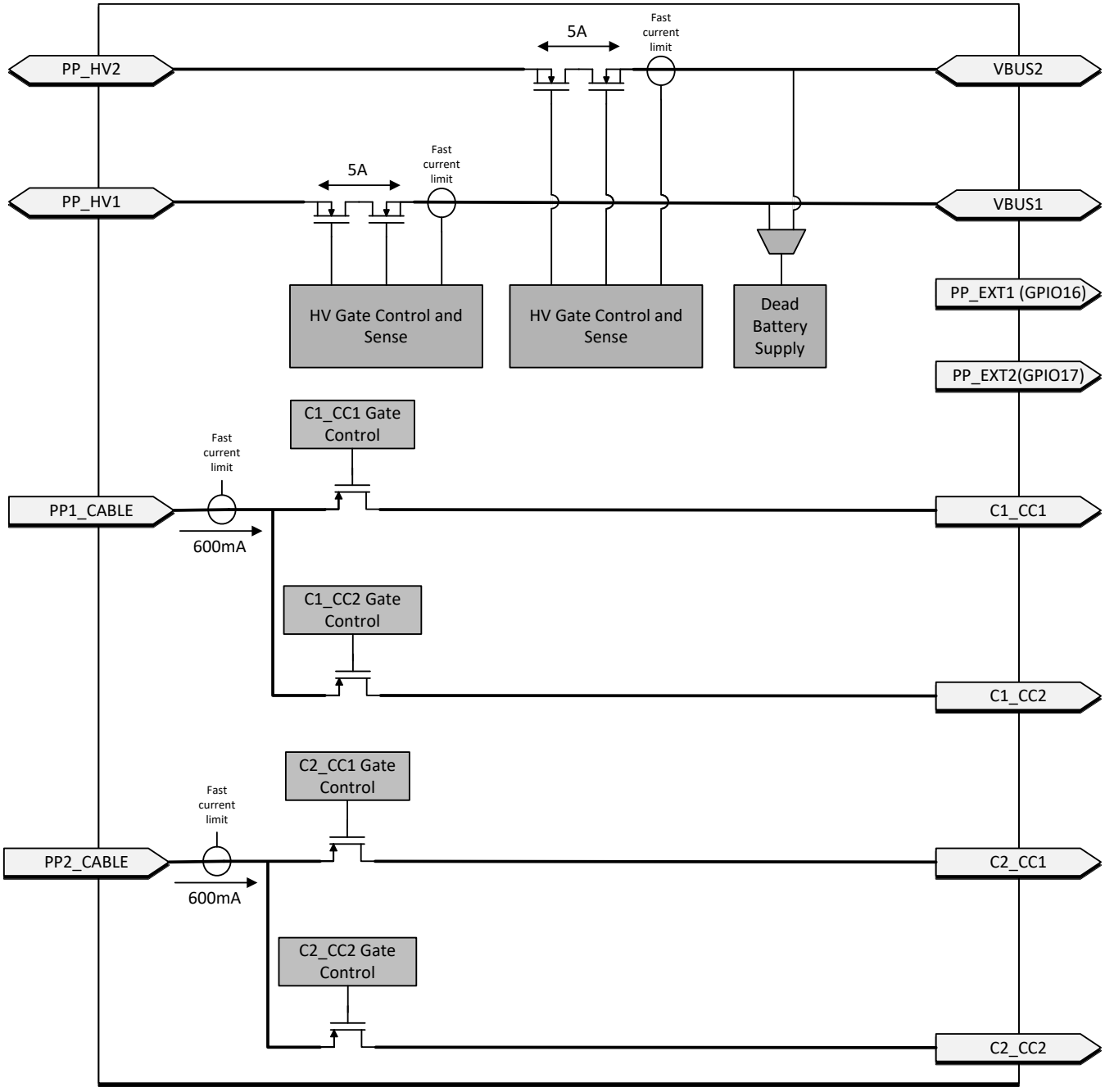


Figure 14. Port Power Switches

8.3.3.1 PP_HV Power Switch

The TPS65988DJ has two integrated bi-directional high-voltage switches that are rated for up to 5 A of current. Each switch may be used as either a sink or source path for supporting USB-PD power up to 20 V at 5 A of current.

Feature Description (continued)

NOTE

The power paths can sustain up to 5 A of continuous current as long as the internal junction temperature of each path remains below 150°C. Care should be taken to follow the layout recommendations described in DRAIN1 and DRAIN2 Pad Pours

8.3.3.1.1 PP_HV Overcurrent Clamp

The internal source PP_HV path has an integrated overcurrent clamp circuit. The current through the internal PP_HV paths are current limited to I_{OCC}. The I_{OCC} value is selected by application firmware and only enabled while acting as a source. When the current through the switch exceeds I_{OCC}, the current clamping circuit activates and the path behaves as a constant current source. If the duration of the overcurrent event exceeds the deglitch time, the switch is latched off.

8.3.3.1.2 PP_HV Overcurrent Protection

The TPS65988DJ continuously monitors the forward voltage drop across the internal power switches. When a forward drop corresponding to a forward current of I_{OCP} is detected the internal power switch is latched off to protect the internal switches as well as upstream power supplies.

8.3.3.1.3 PP_HV OVP and UVP

Both the overvoltage and undervoltage protection levels are configured by application firmware. When the voltage on a port's VBUS pin exceeds the set overvoltage threshold or falls below the set undervoltage threshold the associated PP_HV path is automatically disabled.

8.3.3.1.4 PP_HV Reverse Current Protection

The TPS65988DJ reverse current protection has two modes of operation: Comparator Mode and Ideal Diode Mode. Both modes disable the power switch in cases of reverse current. The comparator protection mode is enabled when the switch is operating as a source, while the ideal diode protection is enabled while operating as a sink.

In the Comparator mode of reverse current protection, the power switch is allowed to behave resistively until the current reaches the amount calculated in Equation 1 and then blocks reverse current from VBUS to PP_HV. Figure 15 shows the diode behavior of the switch with comparator mode enabled.

$$IREVHV = VREVHV/RPPHV \quad (1)$$

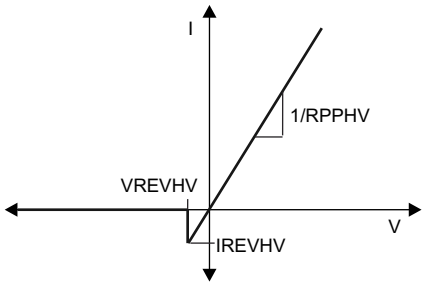


Figure 15. Comparator Mode (Source) Internal HV Switch I-V Curve

In the Ideal Diode mode of reverse current protection, the switch behaves as an ideal diode and blocks reverse current from PP_HV to VBUS. Figure 16 shows the diode behavior of the switch with ideal diode mode enabled.

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Feature Description (continued)

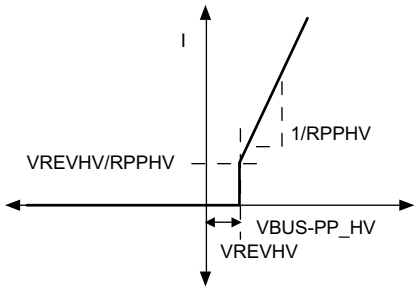


Figure 16. Ideal Diode Mode (Sink) Internal HV Switch I-V Curve

8.3.3.2 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS65988DJ during sudden disconnects due to inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to ground as shown in Figure 17.

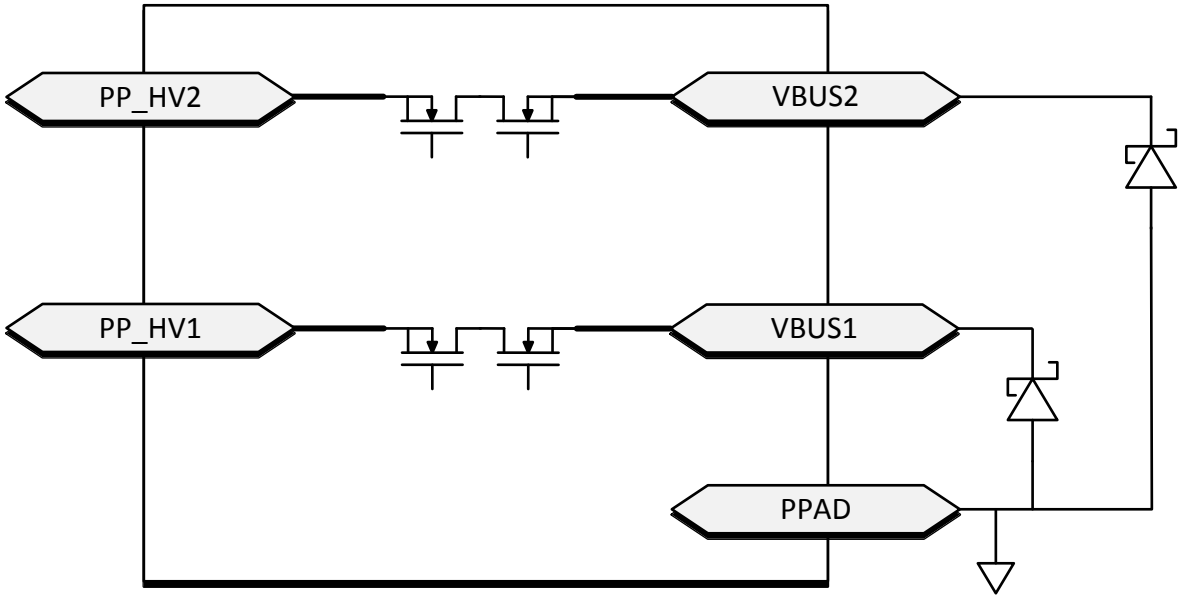


Figure 17. Schottky for Current Surge Protection

8.3.3.3 PP_EXT Power Path Control

GPIO16 and GPIO17 of the TPS65988DJ are intended for control of additional external power paths. These GPIO are active high when configured for external path control and disables in response to an OVP or UVP event. Overcurrent protection and thermal shutdown are not available for external power paths controlled by GPIO16 and GPIO17.

NOTE

GPIO16 and GPIO17 must be pulled to ground through an external pull-down resistor when used as external path control signals.

8.3.3.4 PP_CABLE Power Switch

The TPS65988DJ has two integrated 5-V unidirectional power muxes that are rated for up to 600 mA of current. Each mux may supply power to either of the port CC pins for use as VCONN power.

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Feature Description (continued)

8.3.3.4.1 PP_CABLE Overcurrent Protection

When enabled and providing VCONN power the TPS65988DJ PP_CABLE power switches have a 600-mA current limit. When the current through the PP_CABLE switch exceeds 600 mA, the current limiting circuit activates and the switch behaves as a constant current source. The switches do not have reverse current blocking when the switch is enabled and current is flowing to either Cx_CC1 or Cx_CC2.

8.3.3.4.2 PP_CABLE Input Good Monitor

The TPS65988DJ monitors the voltage at the PP_CABLE pins prior to enabling the power switch. If the voltage at PP_CABLE exceeds the input good threshold the switch is allowed to close, otherwise the switch remains open. Once the switch has been enabled, PP_CABLE is allowed to fall below the input good threshold.

8.3.3.5 VBUS transition to VSAFE5V

The TPS65988DJ has an integrated active pull-down on VBUS for transitioning from high voltage to VSAFE5V. When the high voltage switch is disabled and VBUS > VSAFE5V, an amplifier turns on a current source and pulls down on VBUS. The amplifier implements active slew rate control by adjusting the pull-down current to prevent the slew rate from exceeding specification. When VBUS falls to VSAFE5V, the pull-down is turned off.

8.3.3.6 VBUS Transition to VSAFE0V

When VBUS transitions to near 0 V (VSAFE0V), the pull-down circuit in is turned on until VBUS reaches VSAFE0V. This transition occurs within time TSAFE0V.

8.3.4 Cable Plug and Orientation Detection

Figure 18 shows the plug and orientation detection block at each Cx_CCn pin (C1_CC1, C1_CC2, C2_CC1, C2_CC2). Each pin has identical detection circuitry.

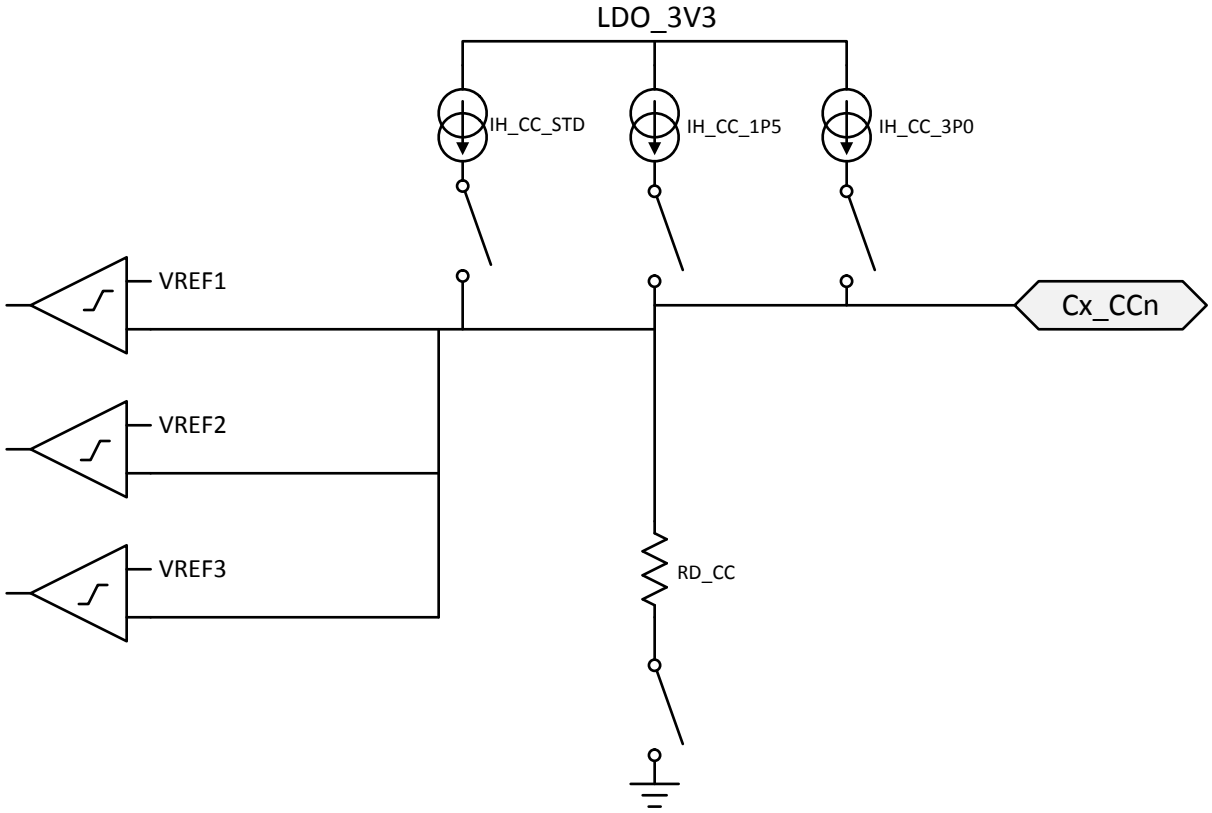


Figure 18. Plug and Orientation Detection Block

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Feature Description (continued)

8.3.4.1 Configured as a DFP

When one of the TPS65988DJ ports is configured as a DFP, the device detects when a cable or a UFP is attached using the Cx_CC1 and Cx_CC2 pins. When in a disconnected state, the TPS65988DJ monitors the voltages on these pins to determine what, if anything, is connected. See USB Type-C Specification for more information.

Table 1 shows the Cable Detect States for a DFP.

Table 1. Cable Detect States for a DFP

C_CC1	C_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both C_CC pins for attach. Power is not applied to VBUS or VCONN until a UFP connect is detected.
Rd	Open	UFP attached	Monitor C_CC1 for detach. Power is applied to VBUS but not to VCONN (C_CC2).
Open	Rd	UFP attached	Monitor C_CC2 for detach. Power is applied to VBUS but not to VCONN (C_CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor C_CC2 for a UFP attach and C_CC1 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Open	Ra	Powered Cable-No UFP attached	Monitor C_CC1 for a UFP attach and C_CC2 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN (C_CC1) then monitor C_CC2 for a UFP detach. C_CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (C_CC2) then monitor C_CC1 for a UFP detach. C_CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either C_CC pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either C_CC pin for detach.

When a TPS65988DJ port is configured as a DFP, a current IH_CC is driven out each C_CCn pin and each pin is monitored for different states. When a UFP is attached to the pin a pull-down resistance of Rd to GND exists. The current IH_CC is then forced across the resistance Rd generating a voltage at the C_CCn pin.

When configured as a DFP advertising Default USB current sourcing capability, the TPS65988DJ applies IH_CC_USB to each C_CCn pin. When a UFP with a pull-down resistance Rd is attached, the voltage on the C_CCn pin pulls below VH_CCD_USB. The TPS65988DJ can be configured to advertise default (500 mA or 900 mA), 1.5-A and 3-A sourcing capabilities when acting as a DFP.

When the C_CCn pin is connected to an active cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the C_CCn pin will pull below VH_CCA_USB/1P5/3P0 and the system recognizes the active cable.

The VH_CCD_USB/1P5/3P0 thresholds are monitored to detect a disconnection from each of these cases respectively. When a connection has been recognized and the voltage on the C_CCn pin rises above the VH_CCD_USB/1P5/3P0 threshold, the system registers a disconnection.

8.3.4.2 Configured as a UFP

When a TPS65988DJ port is configured as a UFP, the TPS65988DJ presents a pull-down resistance RD_CC on each C_CCn pin and waits for a DFP to attach and pull-up the voltage on the pin. The DFP pulls-up the C_CCn pin by applying either a resistance or a current. The UFP detects an attachment by the presence of VBUS. The UFP determines the advertised current from the DFP by the pull-up applied to the C_CCn pin.

8.3.4.3 Configured as a DRP

When a TPS65988DJ port is configured as a DRP, the TPS65988DJ alternates the port's C_CCn pins between the pull-down resistance, Rd, and pull-up current source, Rp.

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8.3.4.4 Fast Role Swap Signaling

The TPS65988DJ cable plug block contains additional circuitry that may be used to support the Fast Role Swap (FRS) behavior defined in the USB Power Delivery Specification. The circuitry provided for this functionality is detailed in Figure 19.

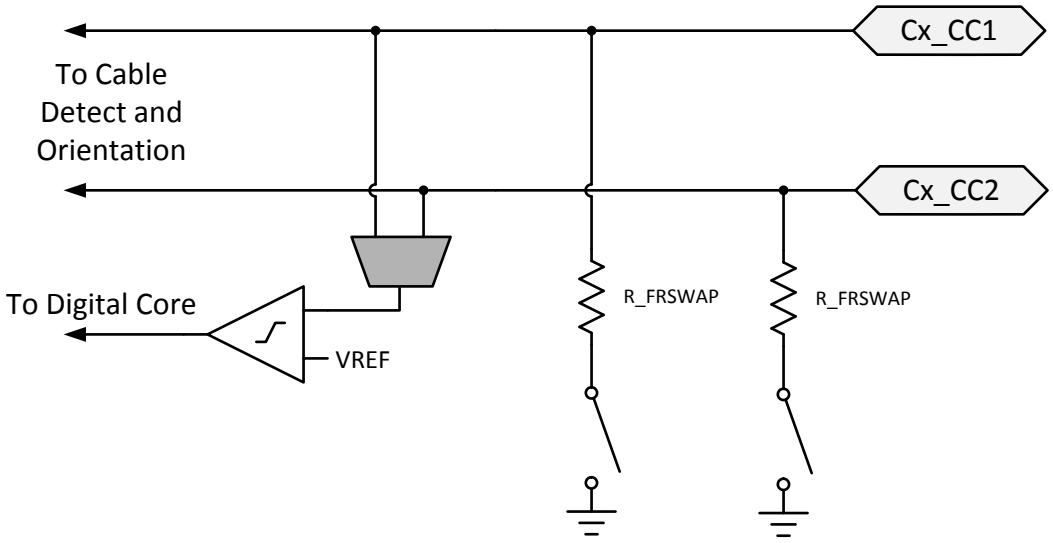


Figure 19. Fast Role Swap Detection and Signaling

When a TPS65988DJ port is operating as a sink with FRS enabled, the TPS65988DJ monitors the CC pin voltage. If the CC voltage falls below VTH_FRS a fast role swap situation is detected and signaled to the digital core. When this signal is detected the TPS65988DJ ceases operating as a sink and begin operating as a source.

When a TPS65988DJ port is operating as a source with FRS enabled, the TPS65988DJ digital core can signal to the connected port partner that a fast role swap is required by enabling the R_FRSWAP pull down on the connected CC pin. When this signal is sent the TPS65988DJ ceases operating as the source and begin operating as a sink.

8.3.5 Dead Battery Operation

8.3.5.1 Dead Battery Advertisement

The TPS65988DJ supports booting from no-battery or dead-battery conditions by receiving power from VBUS. Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source provides a voltage on VBUS. The TPS65988DJ hardware is configured to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd once the device no longer requires power from VBUS. Figure 20 shows the configuration of the C_CCn pins, and elaborates on the basic cable plug and orientation detection block shown in Figure 18. A resistance R_RPD is connected to the gate of the pull-down FET on each C_CCn pin. During normal operation when configured as a sink, RD is RD_CC; however, while dead-battery or no-battery conditions exist, the resistance is un-trimmed and is RD_DB. When RD_DB is presented during dead-battery or no-battery, application code switches to RD_CC.

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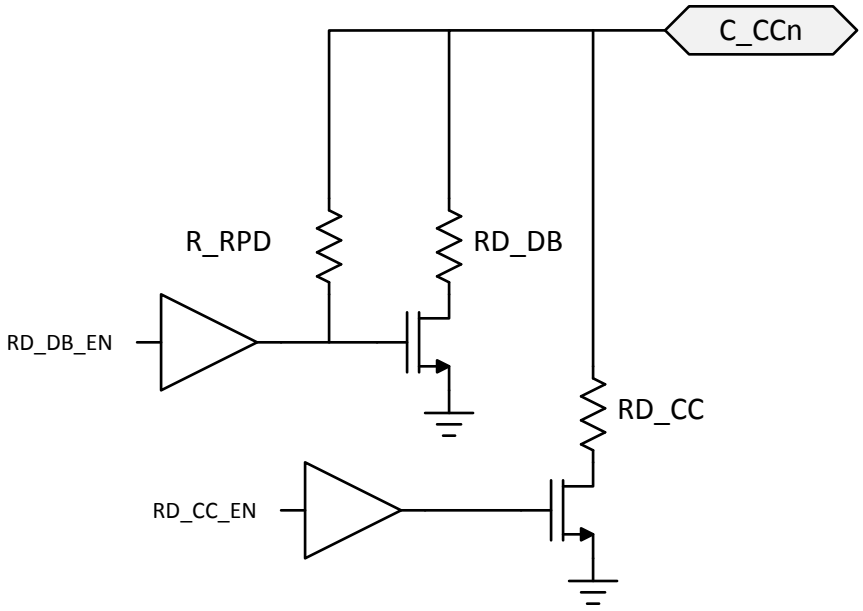


Figure 20. Dead Battery Pull-Down Resistor

In this case, the gate driver for the pull-down FET is Hi-Z at its output. When an external connection pulls up on C_CCn (the case when connected to a DFP advertising with a pull-up resistance Rp or pull-up current), the connection through R_RPD pulls up on the FET gate turning on the pull-down through RD_DB. In this condition, the C_CCn pin acts as a clamp VTH_DB in series with the resistance RD_DB.

8.3.5.2 BUSPOWER (ADCIN1)

The BUSPOWER input to the internal ADC controls the behavior of the TPS65988DJ in response to VBUS being supplied during a dead battery condition. The pin must be externally tied to the LDO_3V3 output via a resistive divider. At power-up the ADC converts the BUSPOWER voltage and the digital core uses this value to determine start-up behavior. It is recommended to tie ADCin1 to LDO_3V3 through a resistor divider as shown in Figure 21. For more information about how to use the ADCIN1 pin to configure the TPS65988DJ, see the Boot section.

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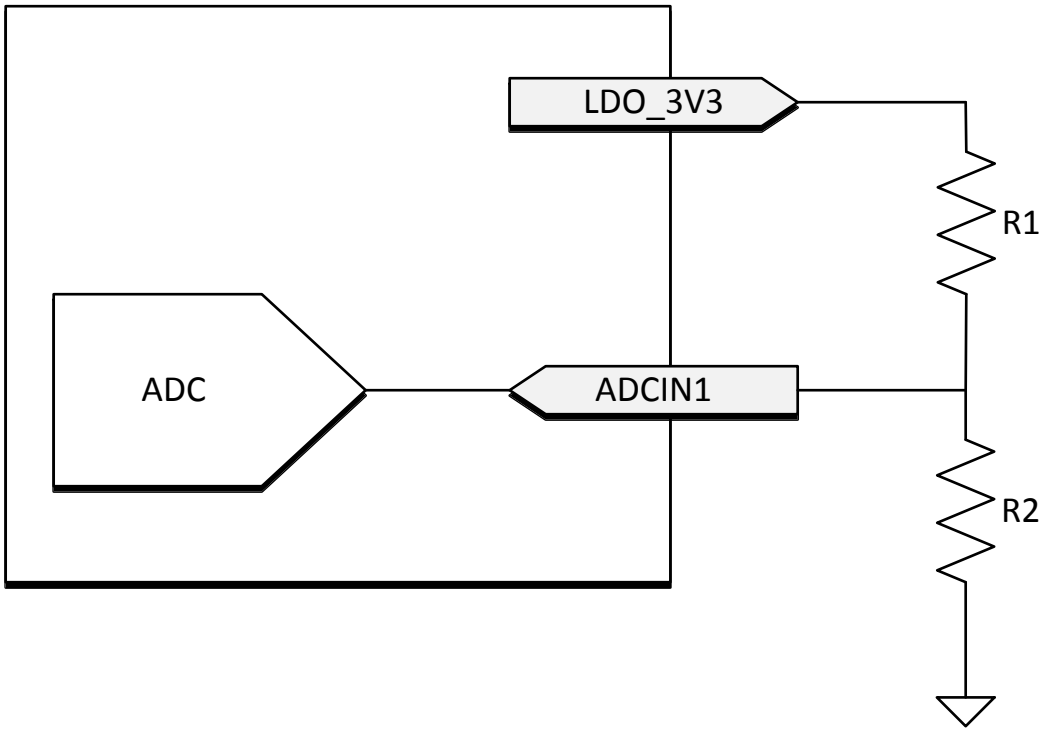


Figure 21. ADCIN1 Resistor Divider

NOTE

Devices implementing the BP_WaitFor3V3_External configuration must use GPIO16 for port 1 external path control and GPIO17 for port 2 external path control.

8.3.6 Battery Charger Detection and Advertisement

The battery charger (BC1.2) block integrates circuitry to detect when the connected entity on the USB D+/D– pins is a BC1.2 compliant charger, as well as advertise BC1.2 charging capabilities to connected devices. To enable the required detection and advertisement mechanisms, the block integrates various voltage sources, currents, and resistances. shows the connection of these elements to the TPS65988DJ Cx_USB_P and Cx_USB_N pins.

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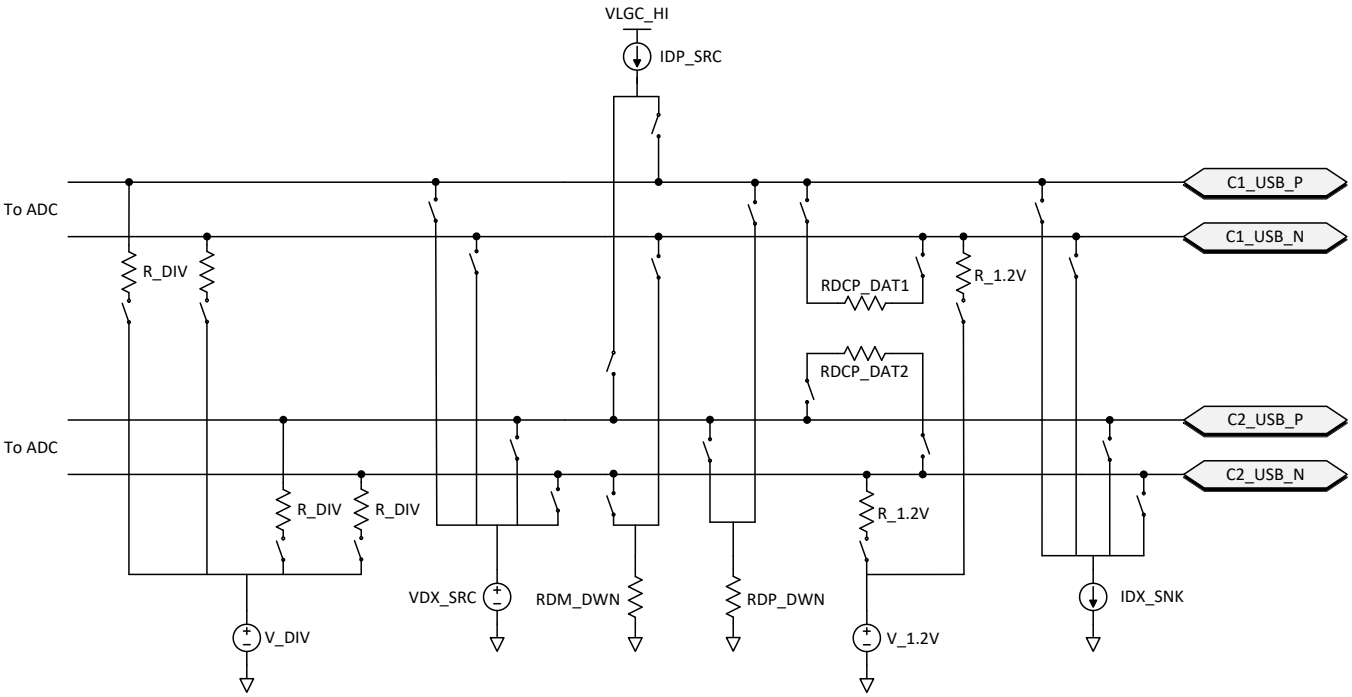


Figure 22. Battery Charger Detection and Advertisement

NOTE

The pull-up and pull-down resistors required by the USB2 standard for a USB host or device are not provided by the TPS65988DJ and must be provided externally to the device in final applications.

8.3.6.1 BC1.2 Data Contact Detect

The Data Contact Detect follows the definition in the USB BC1.2 specification. The detection scheme sources a current IDP_SRC into the D+ pin of the USB connection. The current is sourced into the C_USB_P D+ pin. A resistance RDM_DWN is connected between the D- pin and GND. The current source IDP_SRC and the pull-down resistance RDM_DWN, is activated during data contact detection.

8.3.6.2 BC1.2 Primary and Secondary Detection

The Primary and Secondary Detection follow the USB BC1.2 specification. This detection scheme looks for a resistance between D+ and D– lines by forcing a known voltage on the first line, forcing a current sink on the second line and then reading the voltage on the second line using the ADC integrated in the TPS65988DJ. The voltage source VDX_SRC and the current source IDX_SNK, are activated during primary and secondary detection.

8.3.6.3 Charging Downstream Port Advertisement

The Charging Downstream Port (CDP) advertisement follows the USB BC1.2 specification. The advertisement scheme monitors the D+ line using the ADC. When a voltage of 0.6 V is seen on the D+ line, TPS65988DJ forces a voltage of 0.6 V on the D- line until the D+ goes low. The voltage source VDX_SRC and the current source IDX_SNK, are activated during CDP advertisement. CDP advertisement takes place with the USB Host 15-kΩ pull-down resistors on the D+ and D- lines from the USB Host Transceiver, because after CDP negotiation takes place on the D+/D- lines, USB2.0 data transmission begins.

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8.3.6.4 Dedicated Charging Port Advertisement

The Dedicated Charging Port (DCP) advertisement follows the USB BC1.2 specification (Shorted Mode per BC1.2) and the YD/T 1591-2009 specification. The advertisement scheme shorts the D+ and D– lines through the RDCP_DAT resistor.

8.3.6.5 2.7-V Divider3 Mode Advertisement

The 2.7-V Divider3 Mode is a proprietary advertisement scheme used to charge popular devices in the market. This advertisement places V_DIV on D+ with an R_DIV output impedance and V_DIV on D- with an R_DIV output impedance. With this advertisement scheme present on D+ and D-, specific popular devices are allowed to pull more than 1.5 A of current from VBUS. If enabling 2.7-V Divider3 Mode advertisement on a port, it is recommended that VBUS be able to supply at least 2.4 A of current.

8.3.6.6 1.2-V Mode Advertisement

The 1.2-V Mode is a proprietary advertisement scheme used to charge popular devices in the market. This advertisement places V_1.2 V on D- with an R_1.2 V output impedance and shorts D+ and D- together through the RDCP_DAT resistor. With this advertisement scheme present on D+ and D-, specific popular devices are allowed to pull more than 1.5 A of current from VBUS. If enabling 1.2-V Mode advertisement on a port, it is recommended that VBUS be able to supply at least 2 A of current.

8.3.6.7 DCP Auto Mode Advertisement

The DCP Auto Mode Advertisement scheme is a special scheme that automatically advertises the correct charging scheme depending on the device attached to the USB port. If a device that detects Dedicated Charging Port Advertisement is connected, the DCP Advertising scheme will automatically be placed on D+/D-. If a device that detects 2.7-V Divider3 Mode Advertisement is connected, the 2.7-V Divider3 Mode Advertising scheme will automatically be placed on D+/D-. Likewise, if a device that detects 1.2-V Mode Advertisement is connected, the 1.2-V Mode Advertising scheme will automatically be placed on D+/D-. The TPS65988DJ DCP Auto Mode Advertisement circuit is able to place the correct advertisement scheme on D+/D- without needing to discharge VBUS.

8.3.7 ADC

The TPS65988DJ integrated ADC is accessible to internal firmware only. The ADC reads are not available for external use.

8.3.8 DisplayPort HPD

To enable HPD signaling through PD messaging, a single pin is used as the HPD input and output for each port. When events occur on these pins during a DisplayPort connection though the Type-C connector (configured by firmware), hardware timers trigger and interrupt the digital core to indicate needed PD messaging. When one of the TPS65988DJ's ports is operating as a DP source, its corresponding HPD pin operates as an output (HPD TX), and when a port is operating as a DP sink, its corresponding HPD pin operates as an input (HPD RX). When DisplayPort is not enabled via firmware both HPD1 and HPD2 operate as generic GPIOs (GPIO3 and GPIO4).

8.3.9 Digital Interfaces

The TPS65988DJ contains several different digital interfaces which may be used for communicating with other devices. The available interfaces include three I^2C ports (I^2C1 is a Master/Slave, I^2C2 is a Slave, and I^2C3 is a Master), one SPI master, and 12 additional GPIOs.

8.3.9.1 General GPIO

Figure 23 shows the GPIO I/O buffer for all GPIOn pins. GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input. The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but

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with GPIO_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO_3V3 and LDO_1V8 to the input buffer. When interfacing with non 3.3-V I/O devices the output buffer may be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

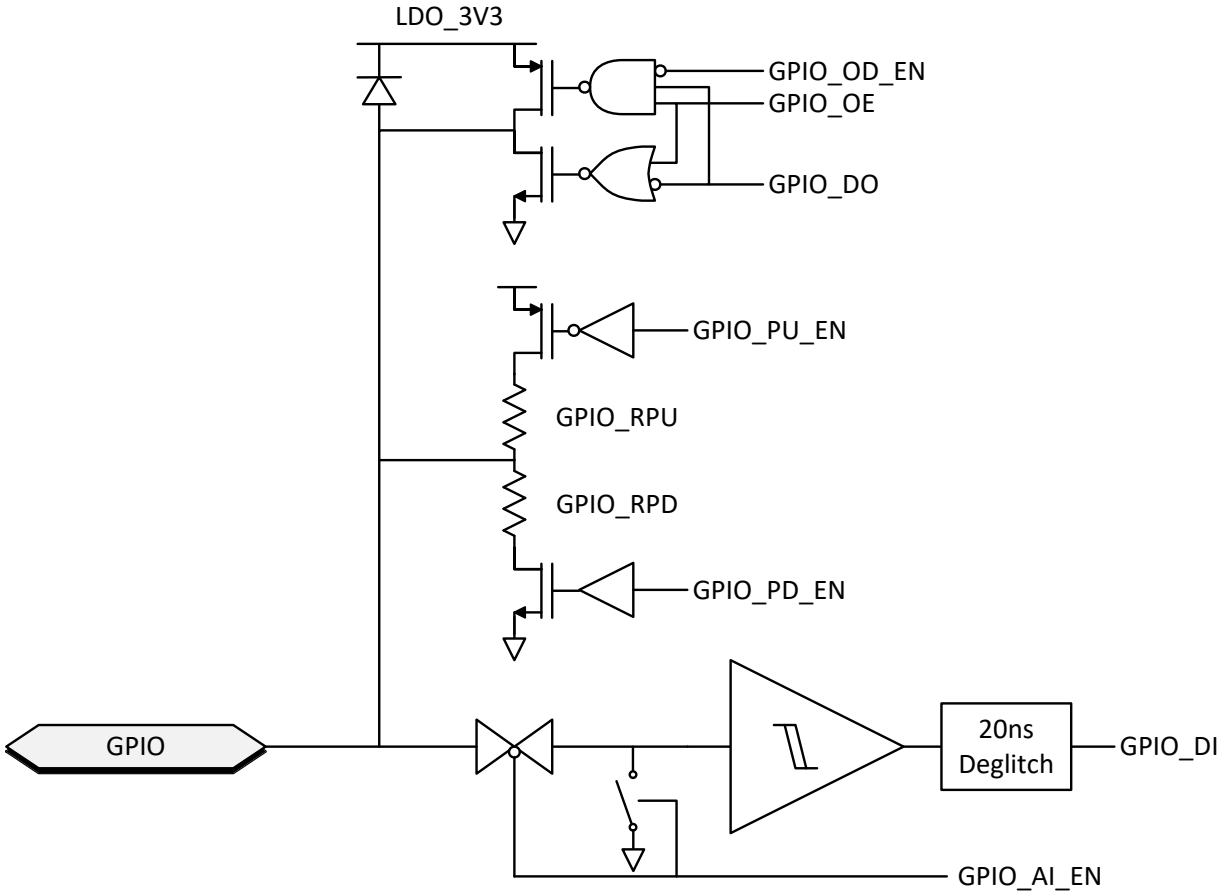


Figure 23. General GPIO Buffer

8.3.9.2 I2C

The TPS65988DJ features three I^2C interfaces. The I^2C1 interface is configurable to operate as a master or slave. The I^2C2 interface may only operate as a slave. The I^2C3 interface may only operate as a master. The I^2C I/O driver is shown in Figure 24. This I/O consists of an open-drain output and in input comparator with de-glitching. The I^2C input thresholds are set by LDO_1V8 and by default.

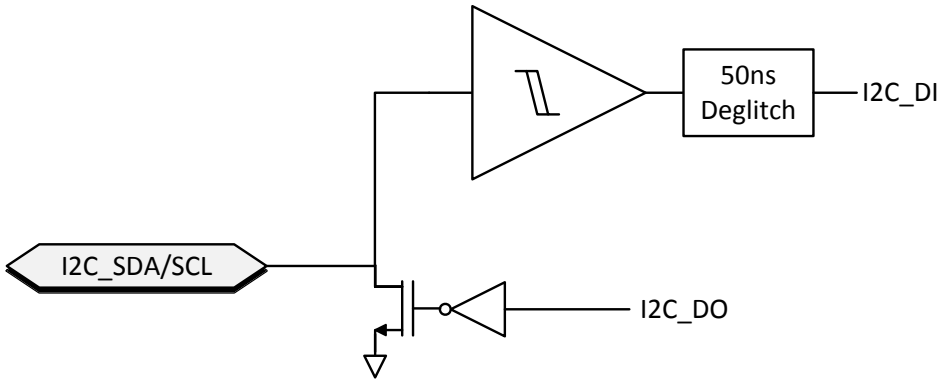


Figure 24. I^2C Buffer

8.3.9.3 SPI

The TPS65988DJ has a single SPI master interface for use with external memory devices. Figure 25 shows the I/O buffers for the SPI interface.

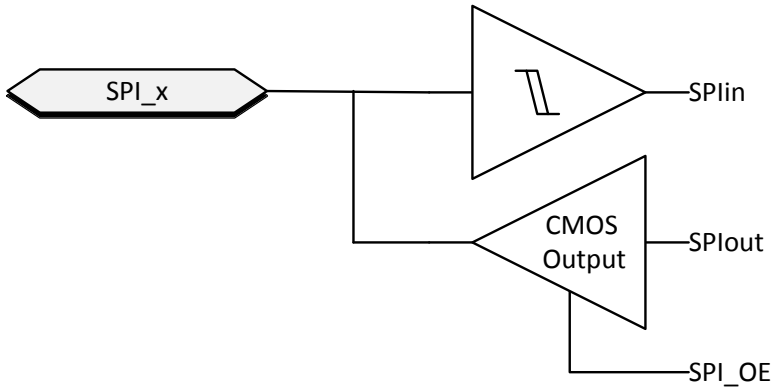


Figure 25. SPI buffer

8.3.10 Digital Core

The figure below shows a simplified block diagram of the digital core.

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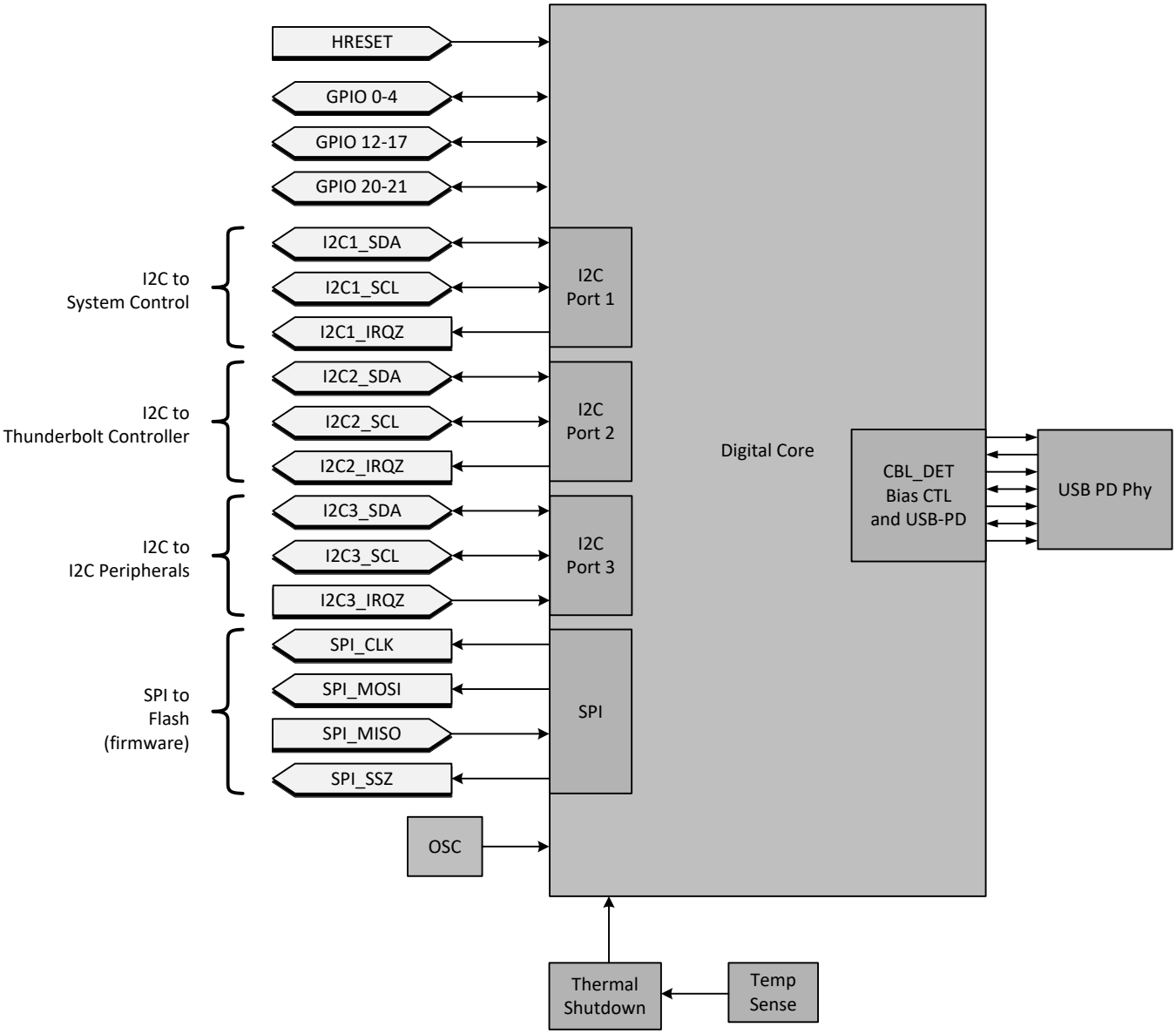


Figure 26. Digital Core Block Diagram

8.3.11 I²C Interfaces

The TPS65988DJ has three I²C interface ports. I²C Port 1 is comprised of the I2C1_SDA, I2C1_SCL, and I2C1_IRQ1 pins. I²C Port 2 is comprised of the I2C2_SDA, I2C2_SCL, and I2C2_IRQ pins. These interfaces provide general status information about the TPS65988DJ, as well as the ability to control the TPS65988DJ behavior, as well as providing information about connections detected at the USB-C receptacle and supporting communications to/from a connected device and/or cable supporting BMC USB-PD. I²C Port 3 is comprised of the I2C3_SDA, I2C3_SCL, and I2C3_IRQ1 pins. This interface is used as a general I²C master to control external I²C devices such as a super-speed mux or re-timer.

The first port can be a master or a slave, but the default behavior is to be a slave. The second port operates as a slave only. Port 1 and Port 2 are interchangeable as slaves. Both Port1 and Port2 operate in the same way and has the same access in and out of the core. An interrupt mask is set for each that determines what events are interrupted on that given port. Port 3 operates as a master only.

8.3.11.1 I²C Interface Description

The TPS65988DJ support Standard and Fast mode I²C interface. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input and output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Figure 27 shows the start and stop conditions of the transfer. Figure 28 shows the SDA and SCL signals for transferring a bit. Figure 29 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

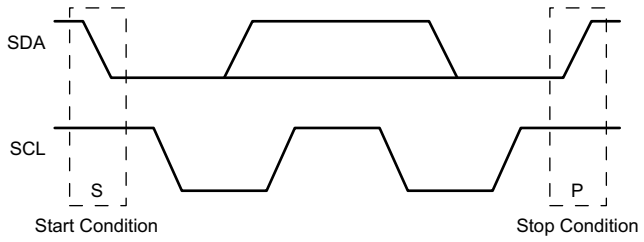


Figure 27. I²C Definition of Start and Stop Conditions

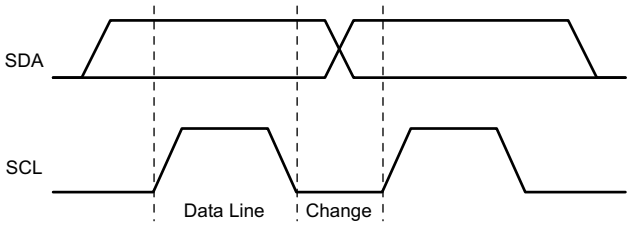


Figure 28. I²C Bit Transfer

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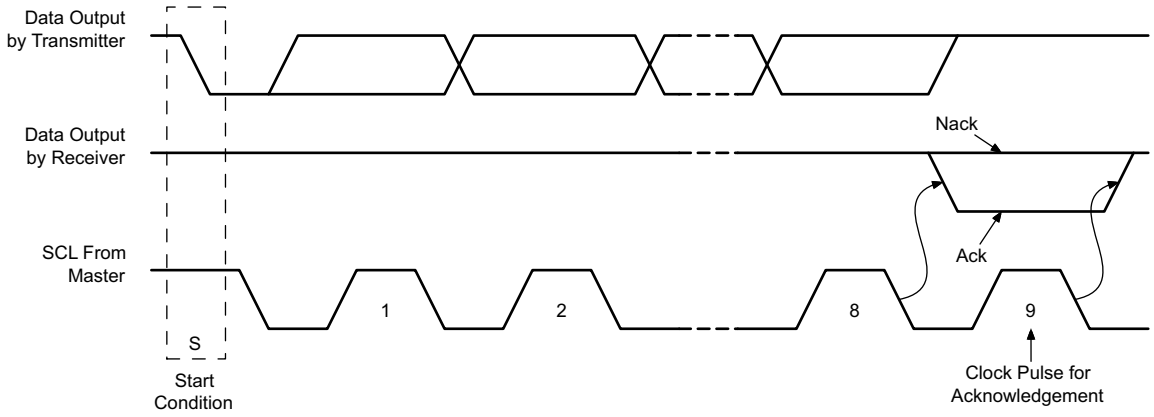


Figure 29. I²C Acknowledgment

8.3.11.2 I²C Clock Stretching

The TPS65988DJ features clock stretching for the I²C protocol. The TPS65988DJ slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 μs for standard 100 kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

8.3.11.3 I²C Address Setting

Each of the TPS65988DJ's two I²C slave interfaces responds to two unique I²C addresses. The first address allows communication with Port 1 of the TPS65988DJ and the second address allows communication with Port 2 of the TPS65988DJ.

The boot flow sets the hardware configurable unique I²C addresses of the TPS65988DJ before the ports are enabled to respond to I²C transactions. For the I2C1 interface, the unique I²C addresses are determined by the analog level set by the analog ADCIN2 pin (three bits) as shown in Table 2 and Table 3.

Table 2. I²C Default Unique Address I2C1 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C1[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

Table 3. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

For the I2C2 interface, the unique I²C address is a fixed value as shown in Table 4 and Table 5.

Table 4. I²C Default Unique Address I2C2 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

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Table 5. I²C Default Unique Address I2C2 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

NOTE

The TPS65988DJ I2C address values are set and controlled by device firmware. Certain firmware configurations may override the presented address settings.

8.3.11.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS65988DJ. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. Figure 30 and Figure 31 show the write and read protocol for the I²C slave interface, and a key is included in Figure 32 to explain the terminology used. The TPS65988DJ Host interface uses a different unique address to identify each of the two USB Type-C ports controlled by the TPS65988DJ. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

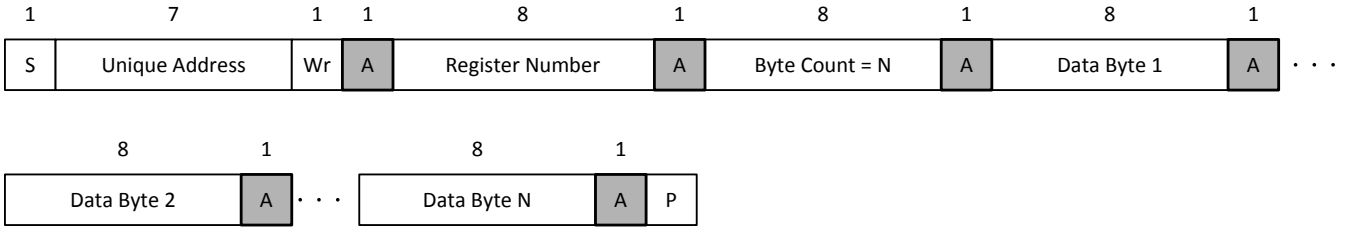


Figure 30. I²C Unique Address Write Register Protocol

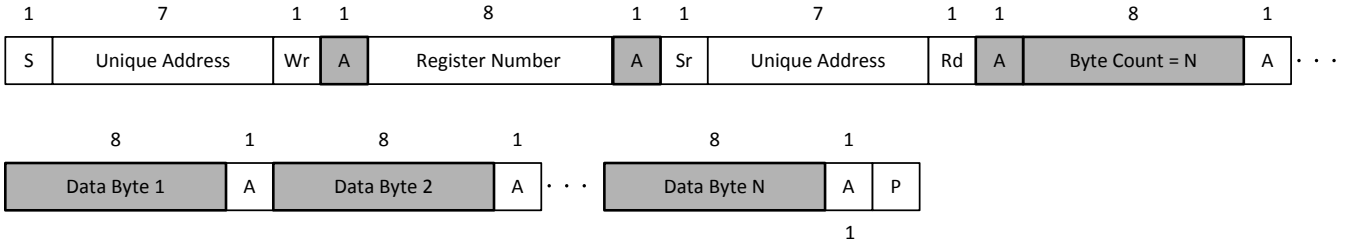


Figure 31. I²C Unique Address Read Register Protocol

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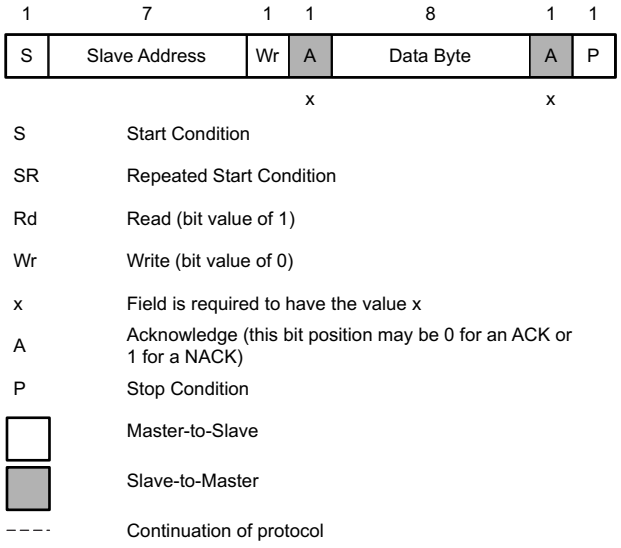


Figure 32. I²C Read/Write Protocol Key

8.3.11.5 I²C Pin Address Setting (ADCIN2)

To enable the setting of multiple I²C addresses using a single TPS65988DJ pin, a resistor divider is placed externally on the ADCIN2 pin. The internal ADC then decodes the address from this divider value. Figure 33 shows the decoding.

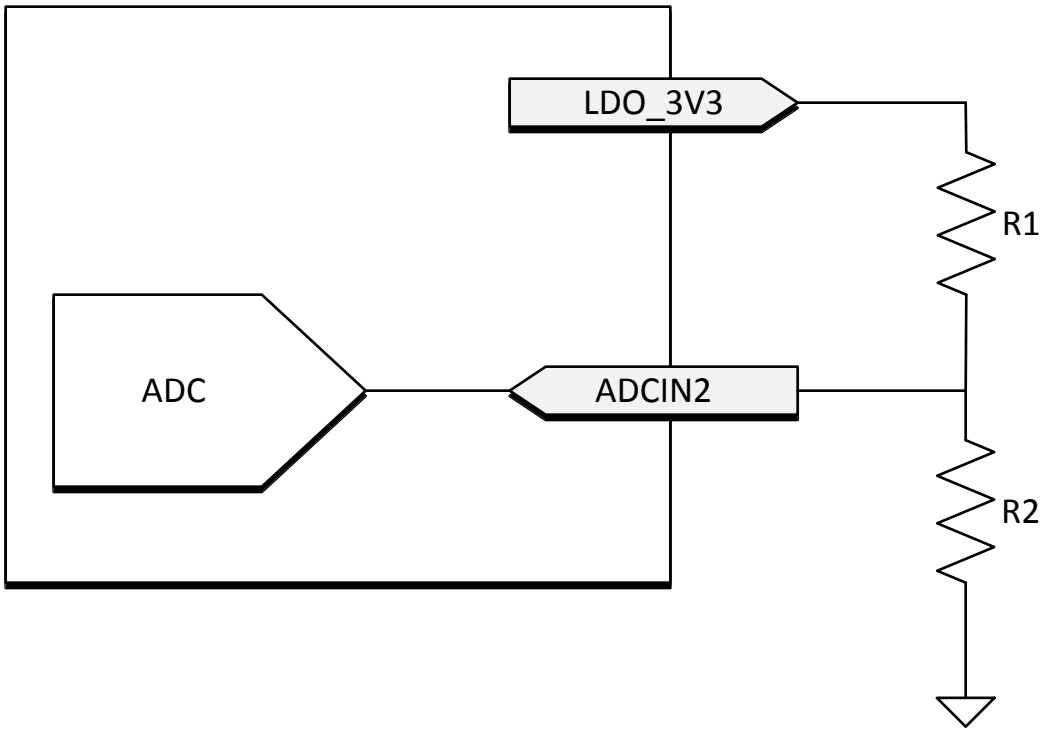


Figure 33. I²C Address Divider

Table 6 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 6. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
Short ADCIN2 to GND		000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
Short ADCIN2 to LDO_3V3		011b	111b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

8.3.12 SPI Master Interface

The TPS65988DJ loads any ROM patch and-or configuration from flash memory during the boot sequence. The TPS65988DJ is designed to power the flash from LDO_3V3 in order to support dead-battery or no-battery conditions, and therefore pull-up resistors used for the flash memory must be tied to LDO_3V3. The flash memory IC must support 12 MHz SPI clock frequency. The size of the flash must be at least 64 kB. The SPI master of the TPS65988DJ supports SPI Mode 0. For Mode 0, data delay is defined s0 that data is output on the same cycle as chip select ($\overline{SPI_SS}$ pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI_MISO and SPI_MOSI pins) is shifted out on the falling edge of the clock (SPI_CLK pin) and data is sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 KB. The W25X05CL or similar is recommended.

8.3.13 Thermal Shutdown

The TPS65988DJ features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of TSD_MAIN. The temperature shutdown has a hysteresis of TSDH_MAIN and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal power path and disables the power path in response to an overtemperature event. Once the temperature falls below TSDH_PWR the path can be configured to resume operation or remain disabled until re-enabled by firmware.

8.3.14 Oscillators

The TPS65988DJ has two independent oscillators for generating internal clock domains. A 24-MHz oscillator generates clocks for the core during normal operation. A 100-kHz oscillator generates clocks for various timers and clocking the core during low power states.

8.4 Device Functional Modes

8.4.1 Boot

At initial power on the device goes through a boot routine. This routine is responsible for initializing device register values and loading device patch and configuration bundles. The device's functional behavior after boot can be configured through the use of pin straps on the SPI_MISO and ADCIN1 pins as shown in Table 7.

Table 7. Boot Mode Pin Strapping

SPI_MISO	ADCIN1 DIV = R2/(R1+R2)(1)		Dead Battery Mode	Device Configuration
	DIV MIN	DIV MAX		
1	0.00	0.18	BP_NoResponse	Safe Configuration
1	0.20	0.28	BP_WaitFor3V3_Internal	Safe Configuration
1	0.30	0.38	BP_ECWait_Internal	Infinite Wait
1	0.40	0.48	BP_WaitFor3V3_External	Safe Configuration

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

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Device Functional Modes (continued)

Table 7. Boot Mode Pin Strapping (continued)

SPI_MISO	ADCIN1 DIV = R2/(R1+R2)(1)		Dead Battery Mode	Device Configuration
	DIV MIN	DIV MAX		
1	0.50	0.58	BP_ECWait_External	Infinite Wait
1	0.60	1.00	BP_NoWait	Safe Configuration
0	0.10	0.18	BP_NoResponse	Configuration 1
0	0.20	0.28	BP_NoResponse	Configuration 2
0	0.30	0.38	BP_ECWait_Internal	Infinite Wait
0	0.40	0.48	BP_NoWait	Configuration 3
0	0.50	0.58	BP_ECWait_External	Infinite Wait
0	0.60	0.68	BP_NoResponse	Configuration 4
0	0.70	0.78	BP_NoWait	Reserved
0	0.80	0.88	BP_NoResponse	Reserved
0	0.90	1.00	BP_NoWait	Configuration 5

The pin strapping configures two different parameters, Dead battery mode and device configuration. The dead battery mode selects device behavior when powered from VBUS. The dead battery mode behaviors are detailed in Table 8.

Table 8. Dead Battery Configurations

CONFIGURATION	DESCRIPTION
BP_NoResponse	No power switch is enabled and the device does not start-up until VIN_3V3 is present
BP_WaitFor3V3_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.
BP_WaitFor3V3_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.
BP_ECWait_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_ECWait_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_NoWait	The device continues to start-up and attempts to load configurations while receiving power from VBUS. Once configuration is loaded the appropriate power switch is closed based on the loaded configuration.

NOTE

Devices implementing the BP_WaitFor3V3_External configuration must use GPIO16 for port 1 external path control and GPIO17 for port 2 external path control.

When powering up from VIN_3V3 or VBUS the device will attempt to load configuration information from the SPI or I2C digital interfaces. The device configuration settings select the device behavior should configuration information not be available during the device boot process. Table 9 shows the device behavior for each device configuration setting.

Table 9. Device Default Configurations

Configuration	Description
Safe	Ports disabled, if powered from VBUS operates a legacy sink
Infinite Wait	Device infinitely waits in boot state for configuration information

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Table 9. Device Default Configurations (continued)

Configuration	Description
Configuration 1	DFP only (Internal Switch) 5 V at 3-A Source capability USB Type-C Only (No PD)
Configuration 2	DFP only (Internal Switch) 45-W Source (5/9/15/20-V Output) TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 3	UFP only (Internal Switch) 5-20 V at 0.9 - 3.0-A Sink capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 4	DFP only (Internal Switch) 60-W Source (5/9/15/20-V Output) TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 5	UFP only (External Switch)) 5-20 V at 0.9-3.0-A Sink capability 5 V at 3.0-A Source capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled

8.4.2 Power States

The TPS65988DJ may operate in one of three different power states: Active, Idle, or Sleep. The functionality available in each state is summarized in Table 10.

Table 10. Power States

	ACTIVE	IDLE	SLEEP
Type-C State			
Type-C Port 1 State	Connected or Unconnected	Connected or Unconnected	Unconnected
LDO_3V3(1)	Valid	Valid	Valid
LDO_1V8	Valid	Valid	Valid
Oscillator Status			
Digital Core Clock Frequency	12 MHz	4 MHz - 6 MHz	100 kHz
100-kHz Oscillator Status	Enabled	Enabled	Enabled
24-MHz Oscillator Status	Enabled	Enabled	Disabled
Available Features			
Type-C Detection	Yes	Yes	Yes
PD Communication	Yes	No	No
I2C Communication	Yes	Yes	No
SPI Communication	Yes	No	No
Wake Events			
Wake on Attach/Detach	N/A	Yes	Yes
Wake on PD Communication	N/A	Yes(2)	No
Wake on I2C Communication	N/A	Yes	Yes

(1) LDO_3V3 may be generated from either VIN_3V3 or VBUS. If LDO_3V3 is generated from VBUS, TPS65988DJ ports only operate as sinks.
(2) Wake up from Idle to Active upon a PD message is supported however the first PD message received is lost.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65988DJ firmware implements a host interface over I^2C to allow for the configuration and control of all device options. Initial device configuration is configured through a configuration bundle loaded onto the device during boot. The bundle may be loaded through I^2C or SPI. The TPS65988DJ configuration bundle and host interface allow the device to be customized for each specific application. The configuration bundle can be generated through the Application Customization Tool.

9.2 Typical Applications

9.2.1 Type-C VBUS Design Considerations

USB Type-C and PD allows for voltages up to 20 V with currents up to 5 A. This introduces power levels that could damage components touching or hanging off of VBUS. Under normal conditions, all high power PD contracts should start at 5 V and then transition to a higher voltage. However, there are some devices that are not compliant to the USB Type-C and Power Delivery standards, and could have 20 V on VBUS. This could cause a 20-V hot plug that can ring above 30 V. Adequate design considerations are recommended below for these non-compliant devices.

9.2.1.1 Design Requirements

Table 11 shows VBUS conditions that can be introduced to a USB Type-C and PD Sink. The system should be able to handle these conditions to ensure that the system is protected from non-compliant and/or damaged USB PD sources. A USB Sink should be able to protect from the following conditions being applied to its VBUS. The *Detailed Design Procedure* section explains how to protect from these conditions.

Table 11. VBUS Conditions

CONDITION	VOLTAGE APPLIED
Abnormal VBUS Hot Plug	4 V - 21.5 V
VBUS Transient Spikes	4 V - 43 V

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 External Sink Power Path Options

The TPS65988DJ provides two GPIO controls that are hardware controlled to respond to over/undervoltage conditions to enable/disable the sink power paths. PEXT1 (GPIO16) and PEXT2 (GPIO17) are used for Port 1 and Port 2 respectively. The GPIO control can be used to control a discrete power path or load switch. The external sink path can be controlled through the embedded controller (EC) or the configuration of the TPS65988DJ. The EC approach allows the embedded controller to only close the sink path when the system is ready to start receiving power from VBUS. The configuration allows the PD controller to enable and disable the external power path and can be configured to only enable one path with the highest power PD contract.

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9.2.1.2.1.1 Load Switch Power Path

When a load switch is used for the external sink path there are a few parameters to consider. Choosing a load switch that is capable of withstanding 20 V on VBUS could be considered as a minimum requirement as some faulty or “out of specification” chargers can have 20 V on VBUS without PD communication. The load switch must be able to handle the current supported in the sink capabilities of the system. A system that can sink up to 5 A and is connected to a source that is capable of 200% I_{oc} may see up to 10-A current for a duration of time. The load switch used must be able to handle these current spikes when a system supports high Power Delivery currents. Reverse current protection is very important when there are two sink paths used in the system. The two load switches must prevent a low impedance path from VBUS1 to VBUS2 when they are enabled and disabled.

9.2.1.2.1.2 Discrete Power Path

The recommended discrete power path includes reverse current protection to disable the power path when both sink paths are enabled at different PD contracts. In Figure 34 a comparator is used to force disable the external power path when the common source voltage is higher than the system voltage. The comparator circuit has hysteresis added to prevent any oscillations when the system voltage is very close to the common source voltage. The NMOS driven by the comparator will pull the PEXTx to GND when the common source voltage is higher than the system power and the 1k in series will limit the current drawn from the PEXTx GPIO. The comparator is powered from LDO_3V3 on the TPS65988DJ which mean that even in dead battery operation the comparator circuit will remain active regardless of the state of PEXTx. For lower power consumption from VBUS the voltage dividers for the comparator inputs can use higher resistance values.

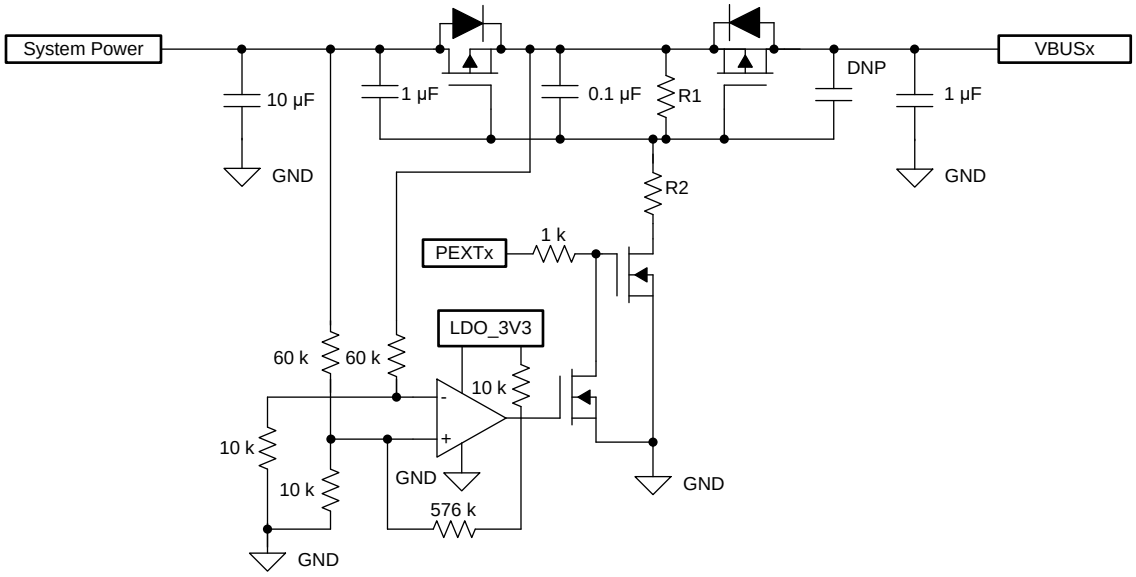


Figure 34. Recommended Sink Power Path

The simplest discrete power path does not have reverse current protection and relies on either the configuration to only enable the power path with the highest power PD contract or on the EC to enable and disable the power path. This simple power path has some limitations as it will always be fully on or fully off and both paths cannot be enabled at the same time. The design is shown in Figure 35.

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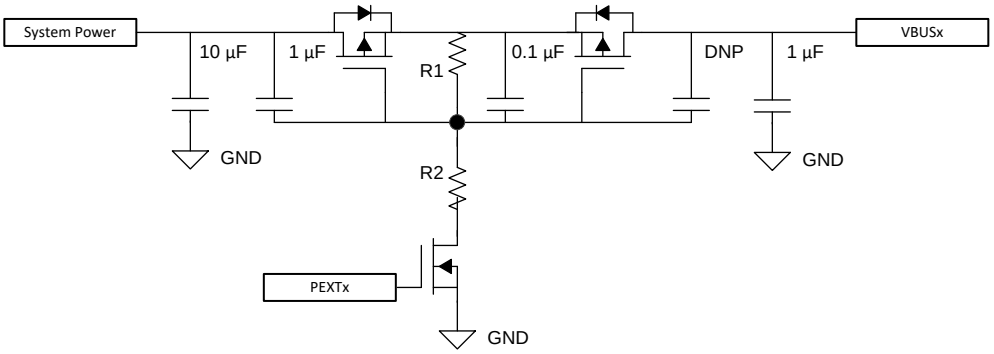


Figure 35. Simple Sink Power Path

For both discrete implementations the R1 and R2 divider should be selected to reach the PMOS threshold (Vgs) at 5 V and 20 V to insure the common source PMOS are completely on. When the sink path is enabled the R1 and R2 resistance will draw current from VBUS. For systems that need to meet low power requirements it is recommended to use higher resistance values for R1 and R2 but this will show how fast the external sink path turns off and on. A R1 = 100 k and R2 = 10 k is a good medium that will draw around 3.6 mW from VBUS at 20 V and will create enough VGS for most PMOS.

9.2.1.2.2 Type-C Connector VBUS Capacitors

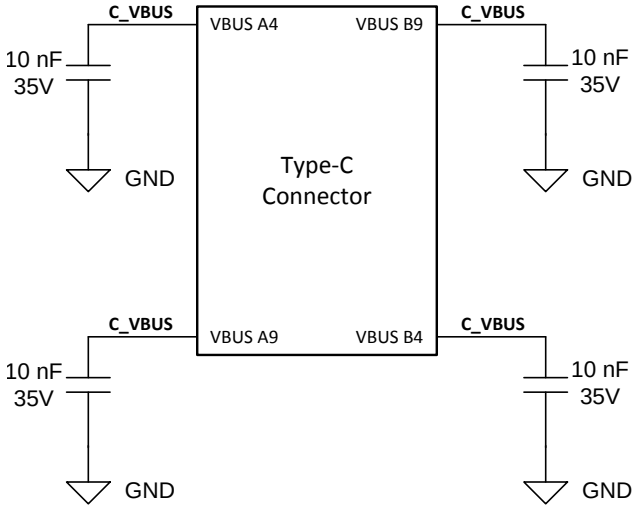


Figure 36. Type-C Connector VBUS Capacitors

The first level of protection starts at the Type-C connector and the VBUS pin capacitors. These capacitors help filter out high frequency noise but can also help absorb short voltage transients. Each VBUS pin should have a 10-nF capacitor rated at or above 25 V and placed as close to the pin as possible. The GND pin on the capacitors should have very short path to GND on the connector. The derating factor of ceramic capacitors should be taken into account as they can lose more than 50% of their effective capacitance when biased. Adding the VBUS capacitors can help reduce voltage spikes by 2 V to 3 V.

9.2.1.2.3 VBUS Schottky and TVS Diodes

Schottky diodes are used on VBUS to help absorb large GND currents when a Type-C cable is removed while drawing high current. The inductance in the cable will continue to draw current on VBUS until the energy stored is dissipated. Higher currents could cause the body diodes on IC devices connected to VBUS to conduct. When the current is high enough it could damage the body diodes of IC devices. Ideally a VBUS Schottky diode should have a lower forward voltage so it can turn on before any other body diodes on other IC devices. Schottky diodes on VBUS also help during hard shorts to GND which can occur with a faulty Type-C cable or damaged Type-C PD device. VBUS could ring below GND which could damage devices hanging off of VBUS. The Schottky diode

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will start to conduct once VBUS goes below the forward voltage. When the TPS65988DJ is the only device connected to VBUS place the Schottky Diode close to the VBUS pin of the TPS65988DJ. The two figures below show a short condition with and without a Schottky diode on VBUS. In without the Schottky diode, VBUS rings 2 V below GND and oscillates after settling to 0 V. In with the Schottky diode, VBUS drops 750 mV below GND (Schottky diode Vf) and the oscillations are minimized.

TVS Diodes help suppress and clamp transient voltages. Most TVS diodes can fully clamp around 10 ns and can keep the VBUS at their clamping voltage for a period of time. Looking at the clamping voltage of TVS diodes after they settle during a transient will help decide which TVS diode to use. The peak power rating of a TVS diode must be able to handle the worst case conditions in the system. A TVS diode can also act as a “pseudo schottky diode” as they will also start to conduct when VBUS goes below GND.

9.2.1.2.4 VBUS Snubber Circuit

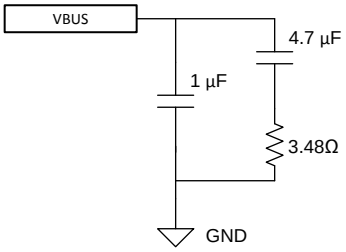


Figure 37. VBUS Snubber

Another method of clamping the USB Type-C VBUS is to use a VBUS RC Snubber. An RC Snubber is a great solution because in general it is much smaller than a TVS diode, and typically more cost effective as well. An RC Snubber works by modifying the characteristic of the total RLC response in the USB Type-C cable hot-plug from being under-damped to critically-damped or over-damped. So rather than clamping the overvoltage directly, it actually changes the hot-plug response from under-damped to critically-damped, so the voltage on VBUS does not ring at all; so the voltage is limited, but without requiring a clamping element like a TVS diode.

However, the USB Type-C and Power Delivery specifications limit the range of capacitance that can be used on VBUS for the RC snubber. VBUS capacitance must have a minimum 1 µF and a maximum of 10 µF. The RC snubber values chosen support up to 4-m USB Type-C cable (maximum length allowed in the USB Type-C specification) being hot plugged, is to use 4.7-µF capacitor in series with a 3.48-Ω resistor. In parallel with the RC Snubber a 1-µF capacitor is used, which always ensures the minimum USB Type-C VBUS capacitance specification is met. This circuit can be seen in .

9.2.1.3 Application Curves

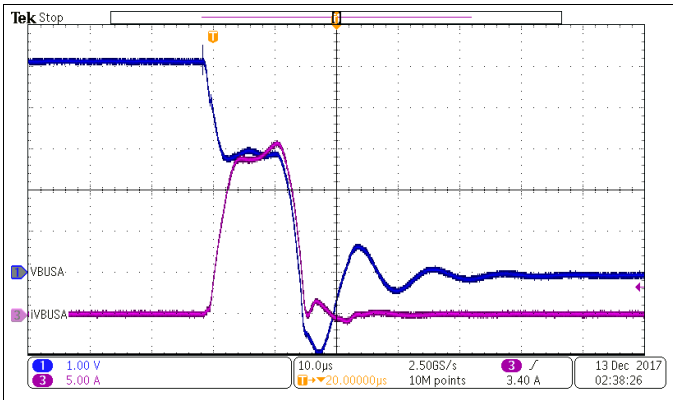


Figure 38. VBUS Short without Schottky Diode

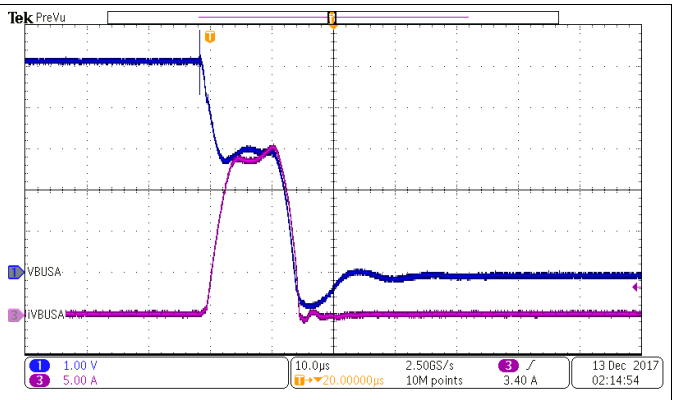


Figure 39. VBUS Short with Schottky Diode

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9.2.2 Dual Port Thunderbolt Notebook with AR Supporting USB PD Charging

The figure below shows Dual Port Thunderbolt Notebook application. The TPS65988DJ is capable of managing two full featured Type-C and PD ports supporting USB, DisplayPort, Thunderbolt and PD charging. When the TPS65988DJ detects a connection on a Type-C port it will generate an interrupt to the Thunderbolt controller to generate the appropriate data output. The TPS65988DJ's two internal power paths provide VBUS which is taken from the System 5 V for Port and will control the external sink path to charge the system through USB PD. The System 5 V will also power PP_CABLE1/2 on the TPS65988DJ to supply VCONN to Type-C e-marked cables and Type-C accessories. An embedded controller EC is used to communicate to the TPS65988DJ for additional control and to relay information back to the operating system. An embedded controller can control additional features such as entering and exiting sleep modes, changing source and sink capabilities depending on the state of the battery, UCSI support, control alternate modes, and so forth.

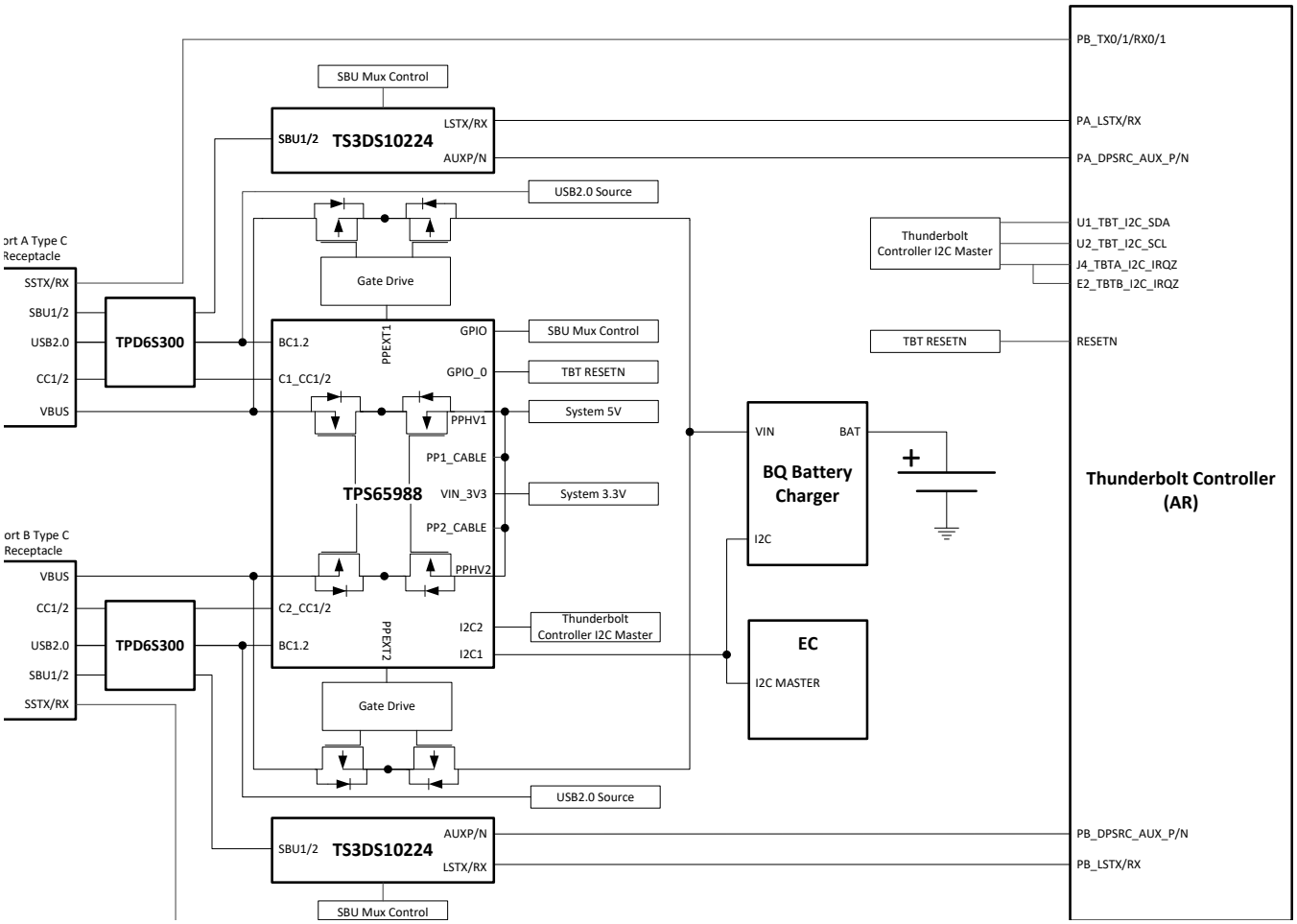


Figure 40. TBT Notebook with PD Charging

9.2.2.1 Design Requirements

Table 12 summarizes the Power Design parameters for a Dual Port Thunderbolt Notebook.

Table 12. Power Design Requirements

Power Design Parameters	Value	Current Path
PPHV1/2 Input Voltage, Current	5 V, 6 A (3 A per Port)	VBUS Source
PP_CABLE1/2 Input Voltage, Current	5 V, 1 A (500 mA per port)	VCONN Source
PEXT1/2 Voltage, Current	5 V – 20 V, 3 A (5 A Max)	VBUS Sink
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65988DJ Circuitry

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9.2.2.2 USB Power Delivery Source Capabilities

Most Type-C dongles (video and data) draw less than 900 mA and supplying 1.5 A on each Type-C port is sufficient for a notebook that supports USB and DisplayPort. The table below shows the PDO for each port.

Table 13. Source Capabilities

PDO	PDO Type	Voltage	Current
PDO1	Fixed	5 V	1.5 A

9.2.2.3 USB Power Delivery Sink Capabilities

Most notebooks support buck and boost charging which means they can charge the battery from 5 V to 20 V. USB PD sources must also support and follow the Source Power Rules defined by the UBS Power Delivery specification. It is recommended for notebooks to support all the voltages in the Source Power Rules to ensure compatibility with most PD chargers and adapters.

Table 14. Sink Capabilities

PDO	PDO Type	Voltage	Current
PDO1	Fixed	5 V	3 A
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A (5 A Max)

9.2.2.4 Supported Data Modes

Thunderbolt Controllers are capable generate USB3, DisplayPort and Thunderbolt Data. The Thunderbolt controller is also capable of muxing the appropriate super speed signal to the Type-C connector. Thunderbolt systems do not need a super speed mux for the Type-C connector. Table 15 summarizes the data capabilities of each Type-C port supporting Thunderbolt.

Table 15. Supported Data Modes

Protocol	Data	Data Role
USB Data	USB3.1 Gen2	Host (DFP)
DisplayPort	DP1.2	Host, DFP_D (Pin Assignemnt C, D, and E)
Thunderbolt	PCIe/DP	Host/Device

9.2.2.5 RESETN

The TPS65988DJ and the Thunderbolt controller share the same flash and they must be able to access it at different times. The TPS65988DJ will access the flash first to load its configuration and then the Thunderbolt controller will read the flash for its firmware. The TPS65988DJ will hold the Thunderbolt controller in reset until it has read its configuration from the flash. GPIO_0 is reserved to act as the reset signal for the Thunderbolt controller. The RESET_N (Thunderbolt Controller Master Reset) signal must also be gated by the 3.3-V supply to the Thunderbolt controller (VCC3P3_SX). When the RESET_N signal is de-asserted before the supply has come up it may put the Thunderbolt controller in a latched state. The RESET_N signal must be de-asserted at least 100 µs after the Thunderbolt Controller supply has come up. For dead battery operation the GPIO_0 signal should be “ANDed” with the 3.3-V supply to avoid de-asserting the RESETN when the Thunderbolt controller is not powered. The figure below shows the RESET_N control with GPIO_0 and the 3.3-V supply. Alternatively, the EC could configure GPIO_0 to de-assert RESETN when the system has successfully booted.

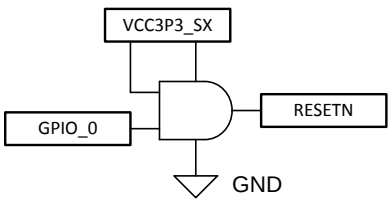


Figure 41. RESETN Circuit

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9.2.2.6 I2C Design Requirements

The I2C connection from the TPS65988DJ and the Thunderbolt control allows the Thunderbolt controller to read the current data status from the TPS65988DJ when there is connection on the Type-C port. The Thunderbolt controller has two interrupts assigned for two Type-C ports and when one of these interrupts is detected, the Thunderbolt controller will read the I2C address corresponding to the Type-C port. For Port A the I2C address is 0×38 and Port B the address 0×3F. The I2C2 on the TPS65988DJ is always connected to the Thunderbolt controller and the I2C channel will respond to both 0x38 and 0x3F I2C addresses. The two interrupt lines from the Thunderbolt controller are both shorted and connected to the I2C2 interrupt on the TPS65988DJ. This will interrupt the Thunderbolt controller to query both port addresses and will determine which port has a data connection.

9.2.2.7 TS3DS10224 SBU Mux for AUX and LSTX/RX

The SBU signals must be muxed from the Type-C connector to the Thunderbolt controller. The AUX for DisplayPort and LSTX/RX for Thunderbolt are connected to the TS3DS10224 and then muxed to the SBU pins. The SBU mux is controlled through GPIOs from the TPS65988DJ. Table 16 shows the TPS65988DJ GPIO events and the control signals from the TS3DS10224.

Table 16. GPIO Events for SBU Mux

TPS65988DJ GPIO EVENT	TS3DS10224 CONTROL
Port 0 Cable Orientation Event	SAO, SBO
Port 0 DP Mode Selection Event	ENA
Port 0 TBT Event	ENB
N/A	SAI tied to VCC
N/A	SBI tied to GND

Table 17 shows the connections for the AUX, LSTXRX, and SBU pins for the TS3DS10224.

Table 17. TS3DS10224 Pin Connections

TS3DS10224 PIN	SIGNAL
INA+	SBU1
INA-	SBU2
OUTB0+	LSTX
OUTB0-	LSRX
OUTB1+	LSRX
OUTB1-	LSTX
OUTA0+	AUX_P
OUTA0-	AUX_N
OUTA1+	AUX_N
OUTA1-	AUX_P

9.2.2.8 Thunderbolt Flash Options

In most Thunderbolt systems the TPS65988DJ will share the flash with the Thunderbolt controller. The flash contains the Thunderbolt Controller firmware and the configuration data for the TPS65988DJ. Table 18 shows the supported SPI flash options for Thunderbolt systems.

Table 18. Flash Supported for Thunderbolt Systems

MANUFACTURER	PART NUMBER	SIZE
Winbond	W25Q80JVNIQ	8 Mb
Spansion	S25FL208K	8 Mb
AMIC	A25L080	8 Mb
Macronix	MX25L8006EM1I	8 Mb
Micron	M25PE80-VMN6TP	8 Mb

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Table 18. Flash Supported for Thunderbolt Systems (continued)

MANUFACTURER	PART NUMBER	SIZE
Micron	M25PX80-VMN6TP	8 Mb

9.2.3 Dual Port USB and Displayport Notebook Supporting PD Charging

Certain SoCs can support USB, DisplayPort and the muxing required for Type-C. The systems that use this architecture may need a re-driver to ensure signal integrity to from the SoC to the Type-C connectors. Generally the SoC is controlled through I2C and must be connected to the I2C1 Master on the TPS65988DJ. A re-driver can be controlled through GPIO or I2C. The Embedded controller is connected to the I2C2 Slave on the TPS65988DJ. Figure 42 shows the SoC controlled though I2C and the Re-Driver controlled through GPIO. Figure 43 shows the SoC and Re-Driver controlled though I2C. The TPS65988DJ's two internal power paths provide VBUS which is taken from the System 5 V for Port and will control the external sink path to charge the system through USB PD. The System 5 V will also power PP_CABLE1/2 on the TPS65988DJ to supply VCONN to Type-C e-marked cables and Type-C accessories. An embedded controller EC is used to communicate to the TPS65988DJ for additional control and to relay information back to the operating system. An embedded controller can control additional features such as entering and exiting sleep modes, changing source and sink capabilities depending on the state of the battery, UCSI support, control alternate modes, and so forth.

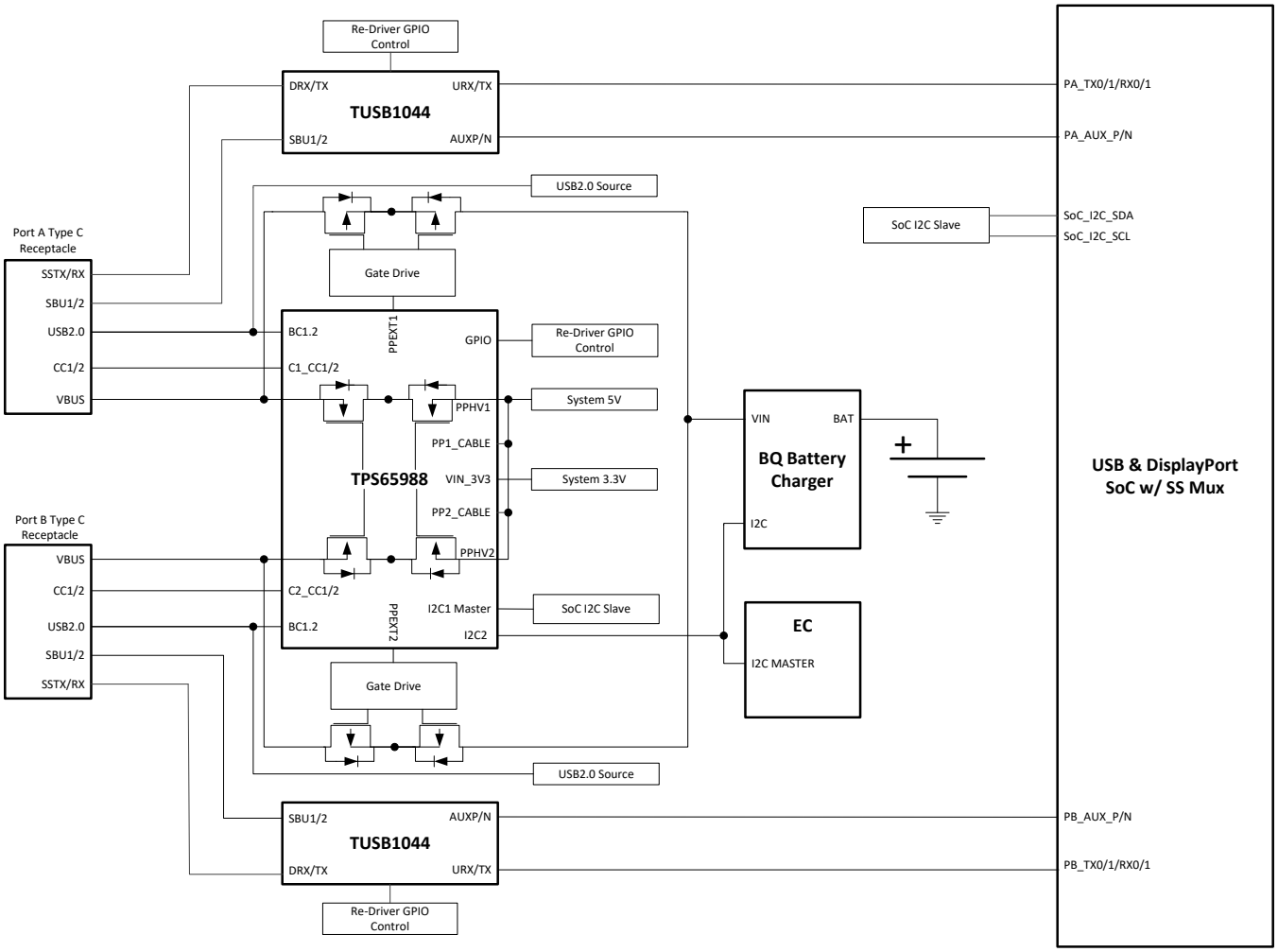


Figure 42. TPS65988DJ and SoC I2C with Re-Driver GPIO

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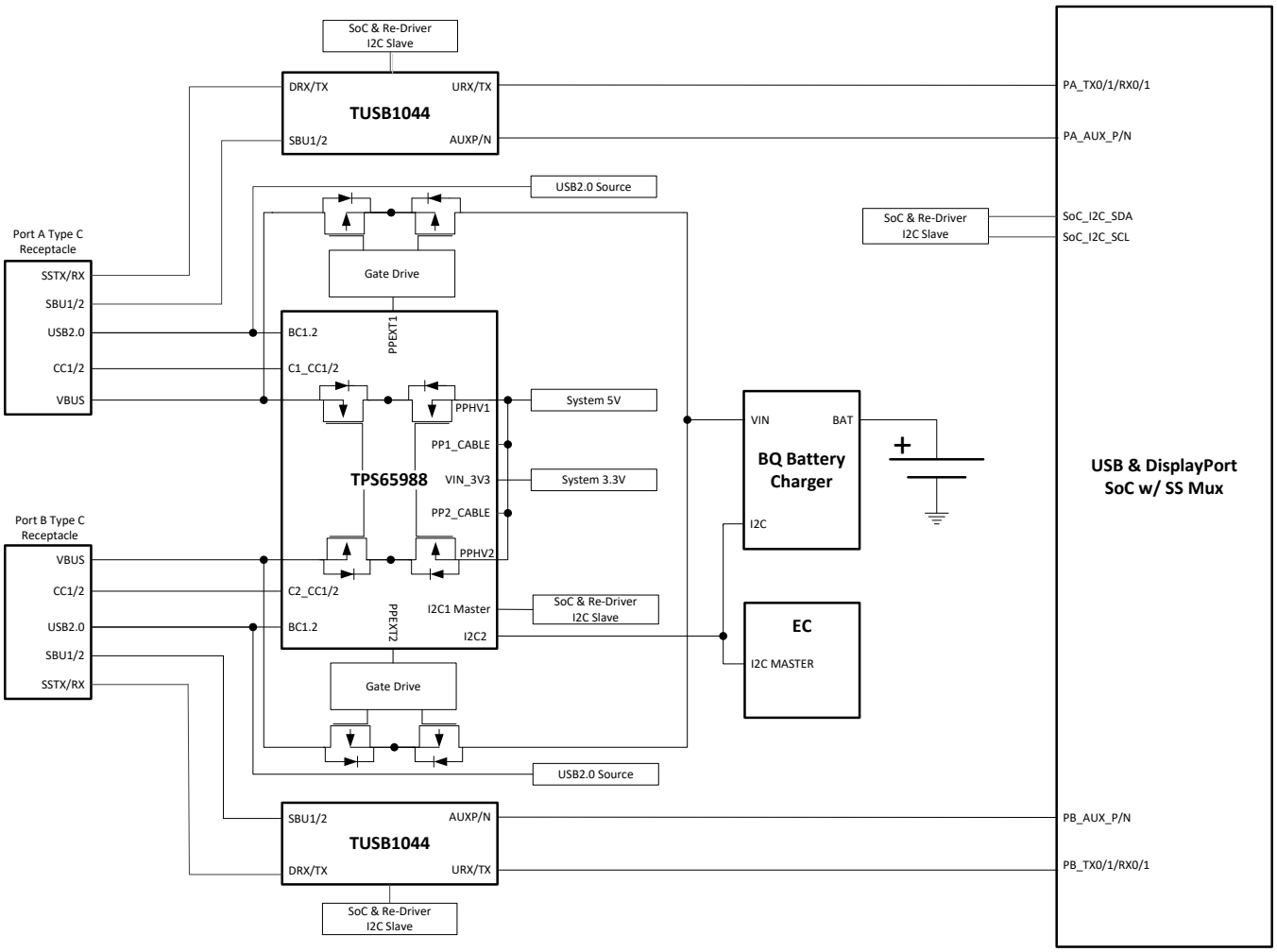


Figure 43. TPS65988DJ, SoC and Redriver I2C

9.2.3.1 Design Requirements

Table 19 summarizes the Power Design parameters for a Dual Port Thunderbolt Notebook.

Table 19. Power Design Requirements

Power Design Parameters	Value	Current Path
PPHV1/2 Input Voltage, Current	5 V, 3 A (1.5 A per Port)	VBUS Source
PP_CABLE1/2 Input Voltage, Current	5 V, 1 A (500 mA per port)	VCONN Source
PEXT1/2 Voltage, Current	5 V – 20 V, 3 A (5 A Max)	VBUS Sink
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65988DJ Circuitry

9.2.3.2 USB Power Delivery Source Capabilities

Most Type-C dongles (video and data) draw less than 900 mA and supplying 1.5 A on each Type-C port is sufficient for a notebook that supports USB and DisplayPort. The table below shows the PDO for each port.

Table 20. Source Capabilities

PDO	PDO Type	Voltage	Current
PDO1	Fixed	5 V	1.5 A

9.2.3.3 USB Power Delivery Sink Capabilities

Most notebooks support buck and boost charging which means they can charge the battery from 5 V to 20 V. USB PD sources must also support and follow the Source Power Rules defined by the UBS Power Delivery specification. It is recommended for notebooks to support all the voltages in the Source Power Rules to ensure compatibility with most PD chargers and adapters.

Table 21. Sink Capabilities

PDO	PDO Type	Voltage	Current
PDO1	Fixed	5 V	3 A
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A (5-A Max)

9.2.3.4 Supported Data Modes

These SoC's are capable to generate USB3, DisplayPort and the appropriate muxing for the super speed signals to the Type-C connector. Table 22 summarizes the data capabilities of each Type-C port.

Table 22. Supported Data Modes

Protocol	Data	Data Role
USB Data	USB3.1 Gen2	Host (DFP)
DisplayPort	DP1.2	Host, DFP_D (Pin Assignemnt C, D, and E)

9.2.3.5 TUSB1044 Re-Driver GPIO Control

The TUSB1044 requires GPIO control to determine whether if there is USB or DisplayPort data connection. The table below summarizes the TPS65988DJ GPIO events and the control pins for the TUSB1044. Note that the pin strapping on the TUSB1044 will set the GPIO control mode and the required equalizer settings.

Table 23. GPIO Events for Super Speed Mux

TPS65988DJ GPIO EVENT	TUSB1044 CONTROL
Port X Cable Orientation Event	FLIP
Port X USB3 Event	CTL0
Port X DP Mode Selection Event	CTL1

9.2.4 USB Type-C and PD Monitor/Dock

Monitors supporting UBS Type-C and PD can take advantage of the various DisplayPort Alternate mode configurations to allow four lane DisplayPort or two lane DisplayPort with USB3.1. Figure 44 shows a monitor that has one Type-C connection that would go to a USB-Type-C PD notebook and another that is connected to another monitor to allow for daisy chaining.

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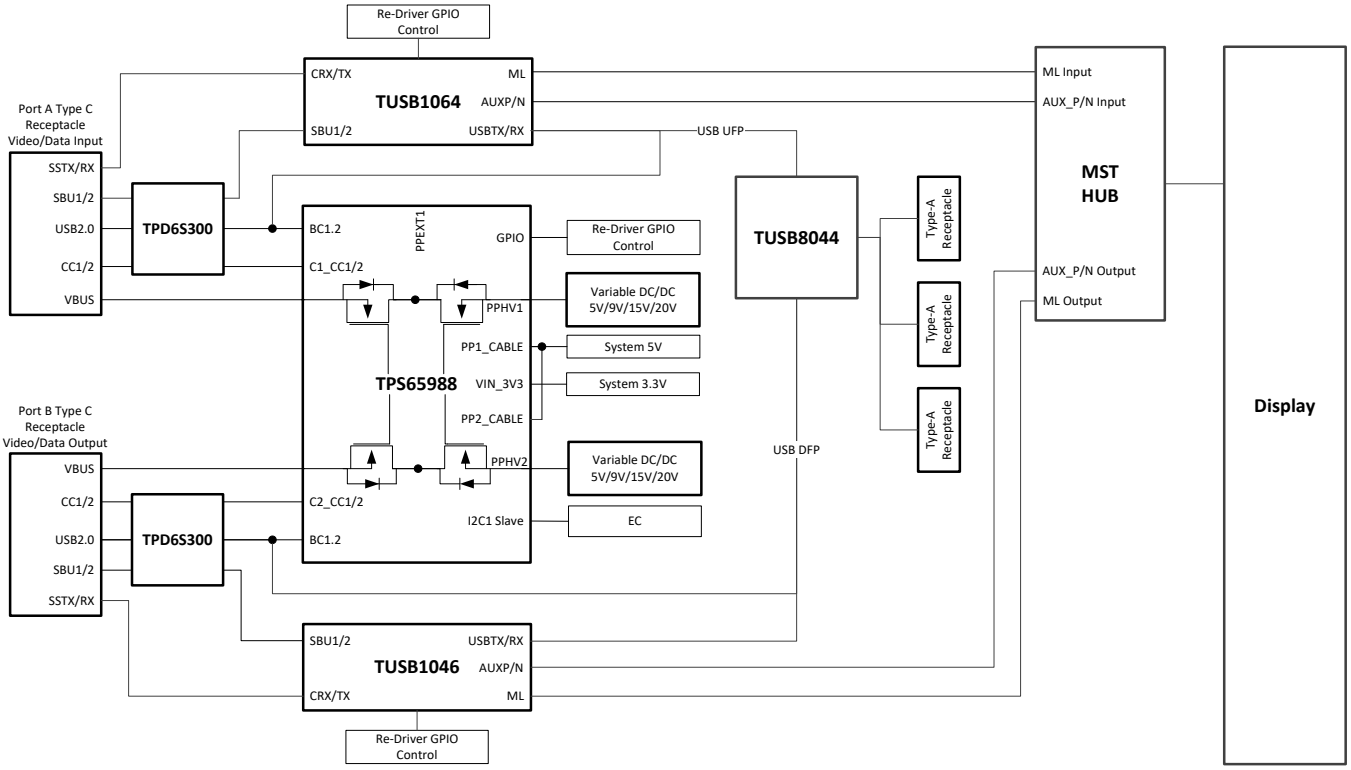


Figure 44. USB and DisplayPort Dock Block Diagram

9.2.4.1 Design Requirements

The table below summarizes the Power Design parameters for a Dual Port Monitor and Dock. For each VBUS source they must be able to provide 60 W at 5-V, 9-V, 15-V and 20-V independently. This will require a variable regulator for each VBUS source.

Table 24. Power Design Parameters

POWER DESIGN PARAMETERS	VALUE	CURRENT PATH
PPHV1/2 Input Voltage, Current	5 V, 9 V, 15 V, 20 V, 6 A (3 A per Port)	VBUS Source
PP_CABLE1/2 Input Voltage, Current	5 V, 500 mA	VCONN Source
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65988DJ Circuitry

9.2.4.2 Detailed Design Procedure

9.2.4.2.1 USB Power Delivery Source Capabilities

To support 60 W, each of the ports must support the PDOs below to meet USB Power Delivery Requirements. .

Table 25. Source PDOs

SOURCE PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A

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9.2.4.2.2 USB and DisplayPort Supported Data Modes

The Type-C port connected to the notebook (USB/DisplayPort source) is a UFP in terms of data. Table 26 summarizes the data capabilities of the Type-C port connected to the notebook.

Table 26. Port 1 Data Capabilities

PROTOCOL	DATA	DATA ROLE
USB Data	USB3.1 Gen1	Device (UFP)
DisplayPort	DP1.2	Device UFP_D (Pin Assignment C and D)

The Type-C port used for daisy chaining will be a DFP in terms of data. Table 27 summarizes the data capabilities of the Type-C port used for daisy chaining.

Table 27. Port 2 Data Capabilities

PROTOCOL	DATA	DATA ROLE
USB Data	USB3.1 Gen1	Host (DFP)
DisplayPort	DP1.2	Host DFP_D (Pin Assignment C, D, and E)

9.2.4.2.3 TUSB1064 Super Speed Mux GPIO Control

The TUSB1064 requires GPIO control in GPIO control mode to determine whether if there is USB or DisplayPort data connection. Table 28 summarizes the TPS65988DJ GPIO Events and the control pins for the TUSB1064. Note that the pin strapping on the TUSB1064 will set the GPIO control mode and the required equalizer settings. For more details refer to the *TUSB1064 data sheet*.

Table 28. GPIO Events for Super Speed Mux

TPS65988DJ GPIO EVENT	TUSB1064 CONTROL
Port 0 Cable Orientation Event	FLIP
Port 0 USB3 Event	CTL0
Port 0 DP Mode Selection Event	CTL1

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10 Power Supply Recommendations

10.1 3.3-V Power

10.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply to the TPS65988DJ device. The VIN_3V3 switch (see Figure 13) is a unidirectional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when 3.3 V is available. See Table 29 for the recommended external capacitance on the VIN_3V3 pin.

10.1.2 VBUS 3.3-V LDO

The 3.3-V LDO from VBUS steps down voltage from VBUS to LDO_3V3 which allows the TPS65988DJ device to be powered from VBUS when VIN_3V3 is unavailable. This LDO steps down any recommended voltage on the VBUS pin. When VBUS is 20 V, as is allowable by USB PD, the internal circuitry of the TPS65988DJ device operates without triggering thermal shutdown; however, a significant external load on the LDO_3V3 pin can increase the temperature enough to trigger a thermal shutdown. The VBUS 3.3-V LDO blocks reverse current from LDO_3V3 back to VBUS allowing VBUS to be unpowered when LDO_3V3 is driven from another source. See Table 29 for the recommended external capacitance on the VBUS and LDO_3V3 pins.

10.2 1.8-V Power

The internal circuitry is powered from 1.8 V. The 1.8-V LDO steps the voltage down from LDO_3V3 to 1.8 V. The 1.8-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, memory and other digital circuits. The 1.8-V LDO also provides power to all internal low-voltage analog circuits. See Table 29 for the recommended external capacitance on the LDO_1V8 pin.

10.3 Recommended Supply Load Capacitance

Table 29 lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

Table 29. Recommended Supply Load Capacitance

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABSOLUTE)	TYP (PLACED)	MAX (ABSOLUTE)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 µF	10 µF	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 µF	10 µF	25 µF
CLDO_1V8	Capacitance on LDO_1V8	4 V	2.2 µF	4.7 µF	12 µF
CVBUS1	Capacitance on VBUS1	25 V	0.5 µF	1 µF	12 µF
CVBUS2	Capacitance on VBUS2	25 V	0.5 µF	1 µF	12 µF
CPP_HV_SRC	Capacitance on PP_HV when configured as a 5-V source	10 V	2.5 µF	4.7 µF	
CPP_HV_SNK	Capacitance on PP_HV when configured as a 20-V sink	25 V	1 µF	47 µF	120 µF
CPP_CABLE	Capacitance on PP_CABLE. When shorted to PP_HV congifured as a 5-V source, the CPP_HV_SRC capacitance may be shared.	10 V	2.5 µF	4.7 µF	

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11 Layout

11.1 Layout Guidelines

A dual port full featured USB Type-C and PD system can be easily implemented in a 20 mm × 40 mm (800 mm^2) area with the TPS65988DJ. This area includes two Type-C receptacles, two low Rdson external power paths, Type-C protection for CC and SBU pins, and the TPS65988DJ. The layout techniques in this guide can be applied to other USB Type-C systems.

11.2 Layout Example

The schematic below shows the design used for this layout example. All TPS65988 I/O are routed in this example, not all designs will use all of the I/O on the device. For differential routing for USB3.1, USB2.0, DisplayPort, and Thunderbolt follow their requirements defined by their respective specifications.

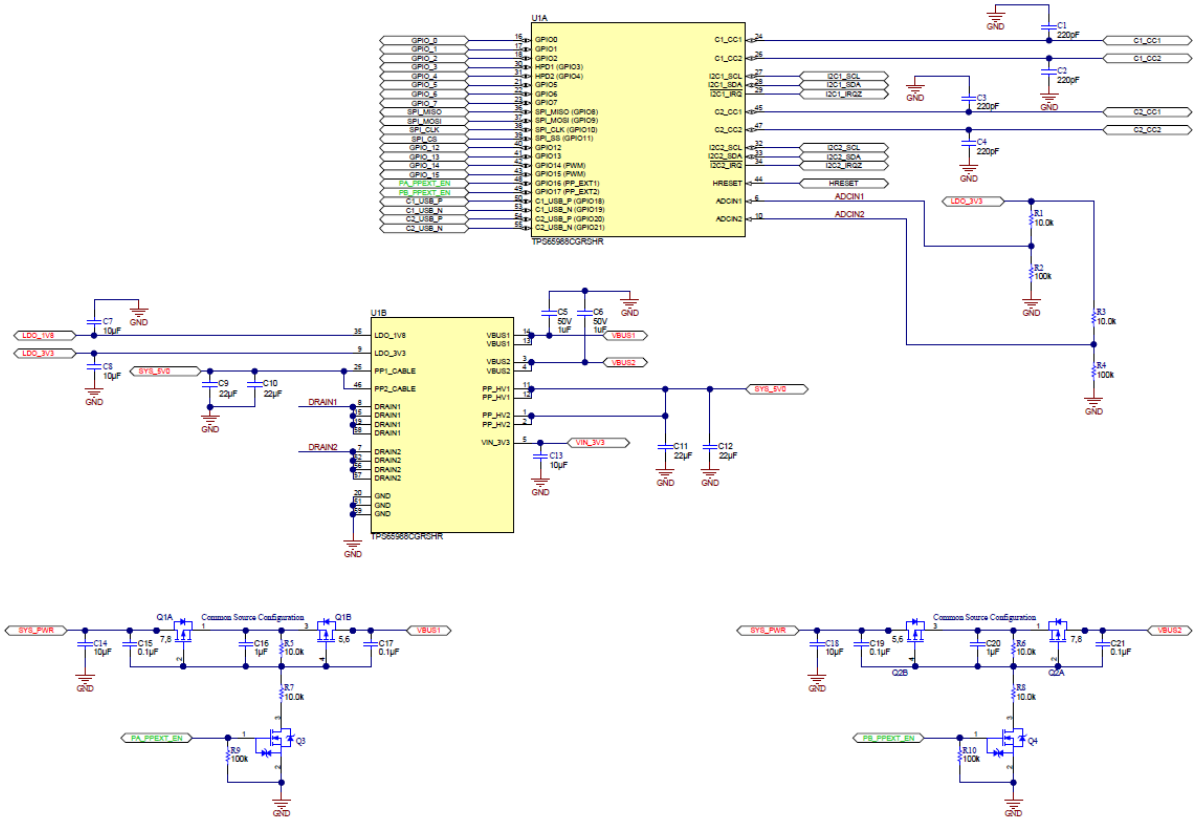


Figure 45. Layout Example Device Schematic

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Layout Example (continued)

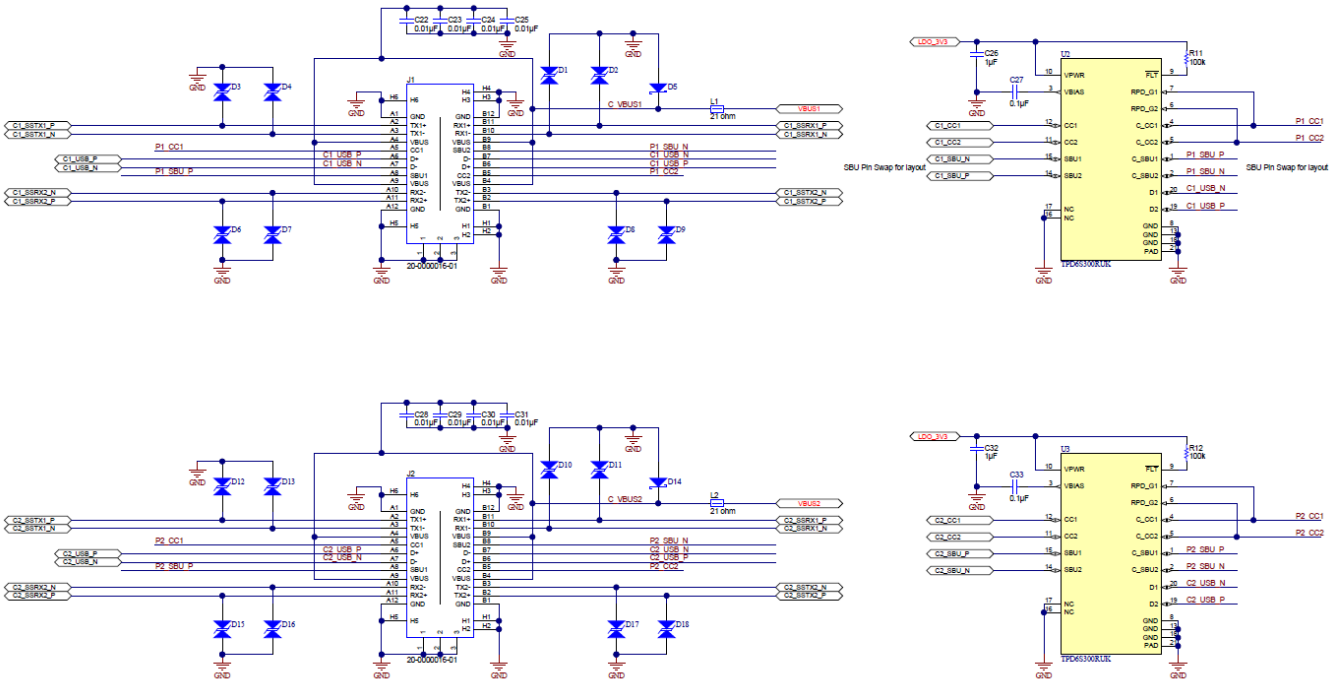


Figure 46. Example Connector Schematic

11.3 Stack-up and Design Rules

An 8-layer stack-up is used and this particular stack is common with most processor chipset guides. In some systems a 10-layer stack-up is used, the same principles can be carried over from the 8-layer to a 10-layer stack-up. Figure 47 shows the details of each of the layers. The two outer layers have a thickness of 1.0 oz copper and the inner layers are 0.5 oz copper.

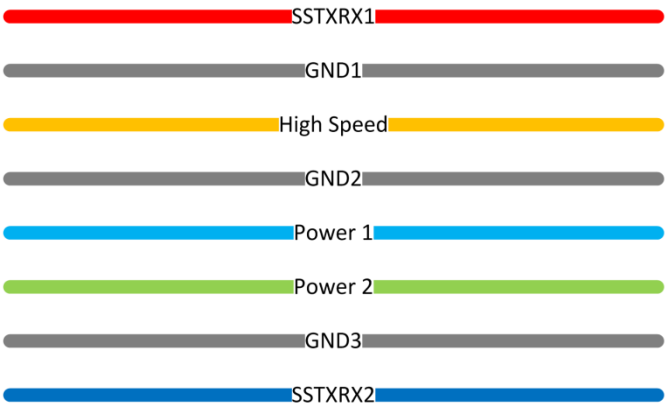


Figure 47. 8 Layer Board Stack Up

Table 30 shows the recommended routing for each of these layers. For power routing the Power 1/2 planes can be stacked to allow for high currents.

Stack-up and Design Rules (continued)

Table 30. Recommend Routing for Layers

Layer	Routing
SSTXRX1	Differential: 85Z, 90Z, 100Z, Single Ended: 50Z, Power, and GPIO
High Speed	Differential: 85Z, 90Z, 100Z, Single Ended: 50Z, and GPIO
Power 1	Power and GPIO
Power 2	Power and GPIO
SSTXRX2	Differential: 85Z, 90Z, 100Z, Single Ended: 50Z, Power, and GPIO

The vias used in this layout example are 8mil/16mil. There are no blind and buried vias used in this layout example and for any via on pad used it is recommended to use epoxy filled vias. The figure below shows the via sizing.



Figure 48. Recommended Minimum Via Sizing

11.4 Main Component Placement

This layout example will place the two Type-C connectors close to each other as they would be a notebook. The Type-C connectors are placed 1000 mils from center to center. This will allow for enough space for the end-user to plug in two USB Type-C devices with ease. The external power paths can be placed in between the ports to make the connection to the system supply easier. The TPS65988DJ is placed above the external power path. This will make for a better connection to VBUS for the TPS65988DJ and the external power path. The High Level Placement figure below shows the solution size and placement of these main components. It is recommended to follow the layout guide in a step by step process.

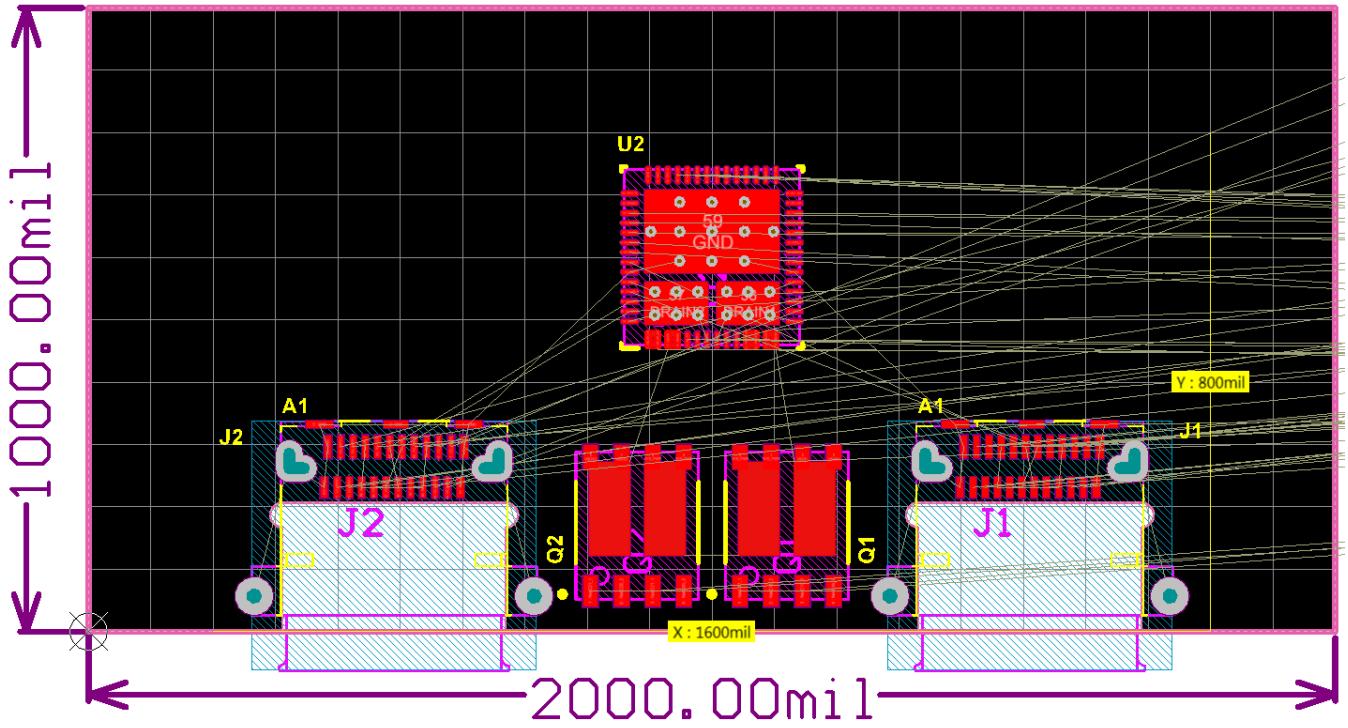


Figure 49. High Level Placement

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11.5 Super Speed Type-C Connectors

In this layout example a dual row SMT mid mount Type-C connector is used. Start by placing vias for all the signals on the Type-C connector that need to be routed on another layer. Once the vias have been placed, route out the super speed lines and place their ESD protection close to the Type-C connector. The figures below show the via placement, top routing, and bottom routing for the super speed signals on the Type-C connector. The same should be implemented for both Type-C connectors.

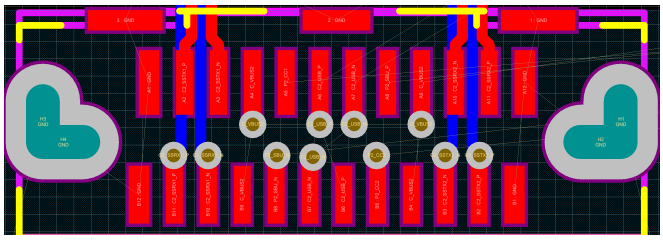


Figure 50. Type-C Connector Via Placement

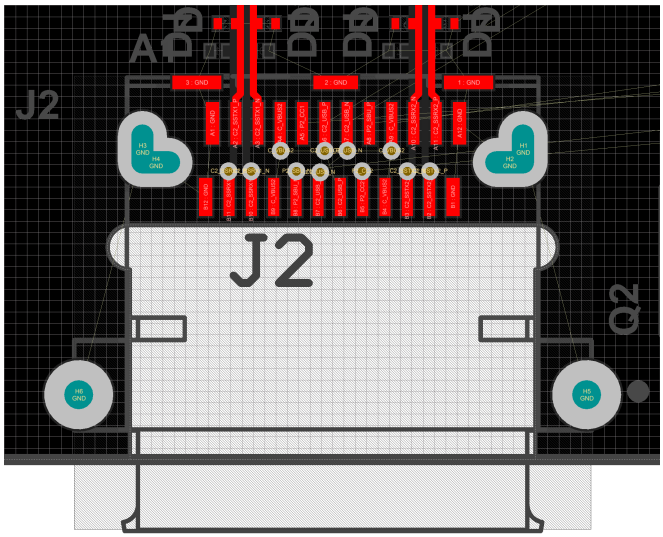


Figure 51. Type-C Connector SSTXRX Top Layer

Super Speed Type-C Connectors (continued)

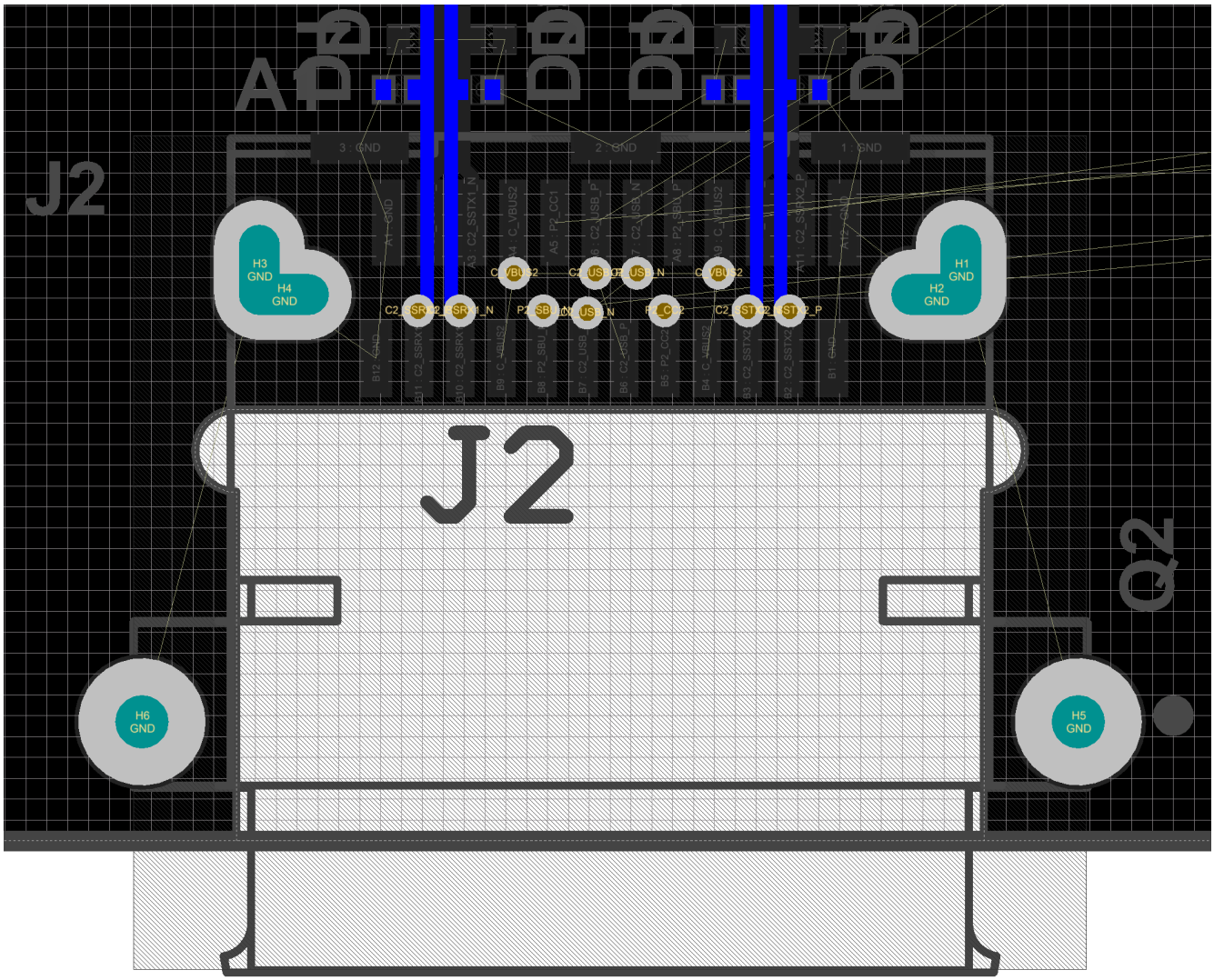


Figure 52. Type-C Connector SSTXRX Bottom Layer

11.6 Capacitor Placement

All of the capacitors for the TPS65988DJ must be placed close to their respective pin. For the PP_HV1/2, VBUS1/2, VIN_3V3 and LDO_3V3 it is recommended to place their capacitors on the opposite side of the TPS65988DJ with the GND terminal facing away from the TPS65988DJ. This method will have all of the GND terminals together in order to have a solid plane that can be stitched to GND. The DRAIN1/2 pad will also have more room for their bottom side pour. PP_CABLE1/2 and LDO_1V8 are placed on the opposite side but their GND terminals are facing toward the TPS65988DJ to share the common GND pour from the TPS65988DJ GND pad. VBUS1/2 and PP_HV1/2 should have at least four vias to connect the TPS65988DJ pin, capacitors and pours. For VIN_3V3, LDO_3V3, LDO_1V8 and PP_CABLE1/2 they can be connected with a single via to their capacitors and pours.

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Capacitor Placement (continued)

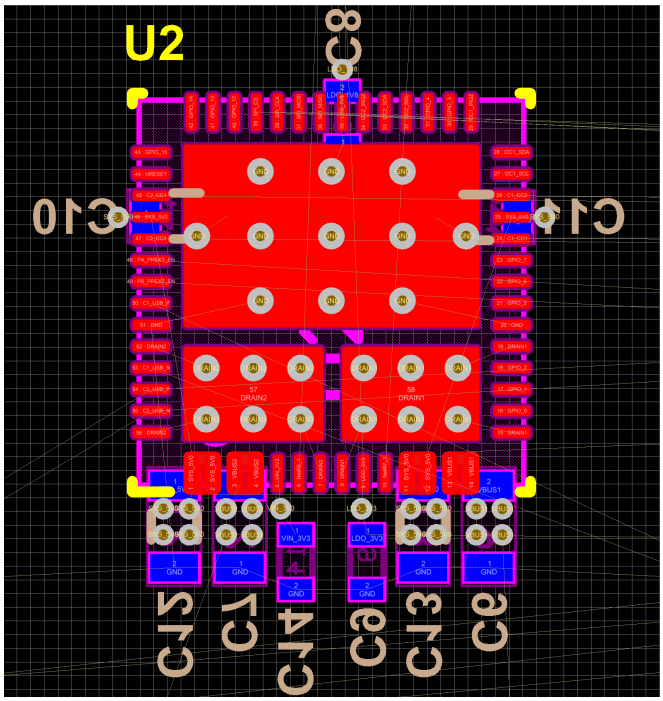


Figure 53. System Capacitors Placement Top/Bottom Layer

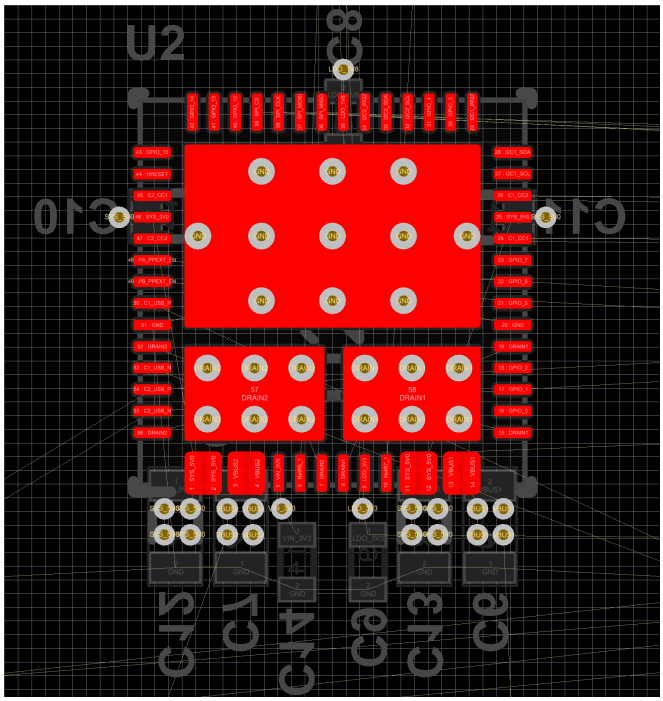


Figure 54. System Capacitors Placement Top Layer

Capacitor Placement (continued)

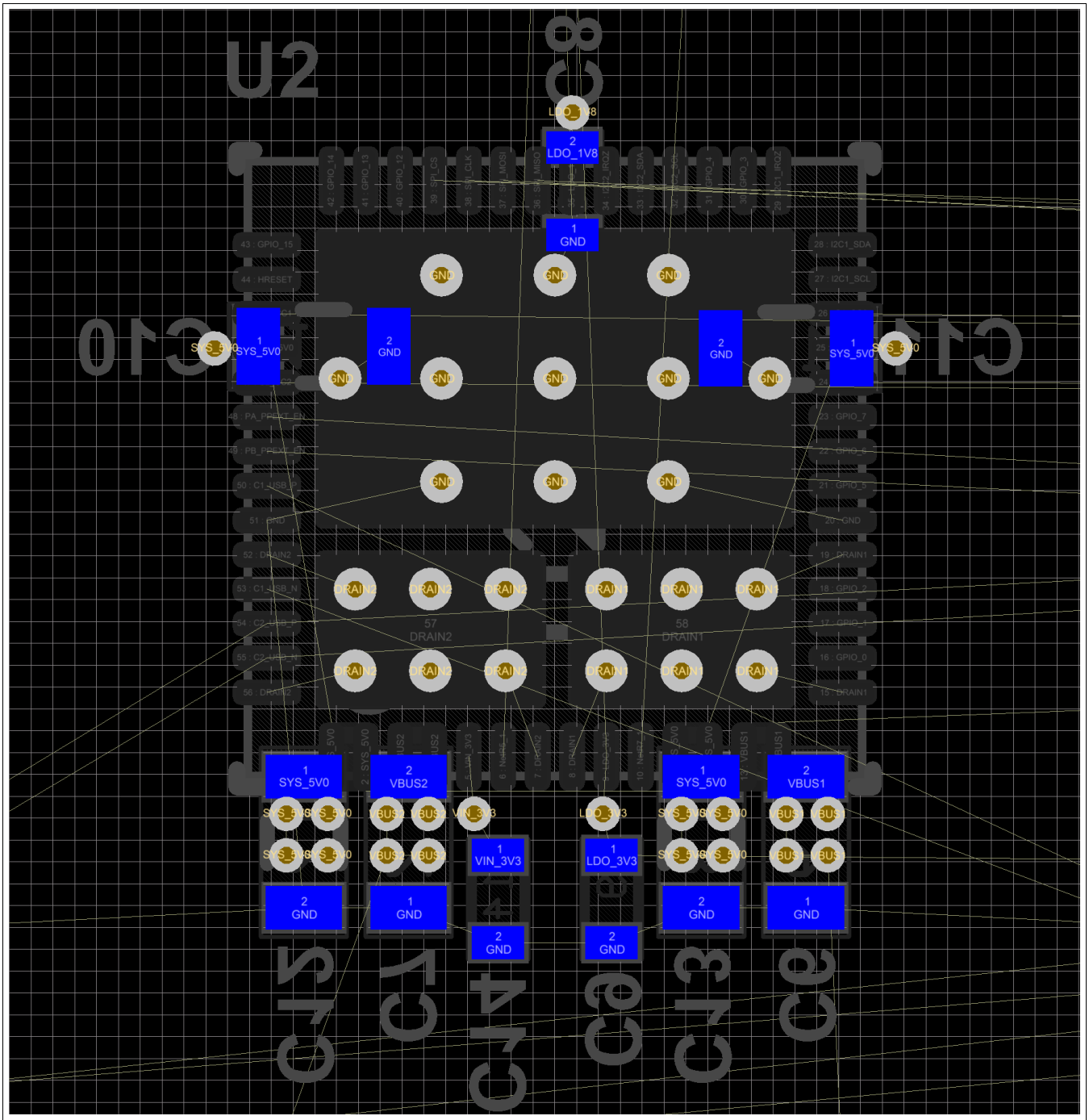


Figure 55. System Capacitors Placement Bottom Layer

11.7 CC1/2 Capacitors & ADCIN1/2 Resistors

The CC1/2 capacitors should be placed on the same layer as the TPS65988DJ and should be placed relatively close to the pins. The ADCIN1/2 resistors have more flexibility where they are placed. In this layout example they are placed close to the LDO_3V3. The figure below shows the placement.

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CC1/2 Capacitors & ADCIN1/2 Resistors (continued)

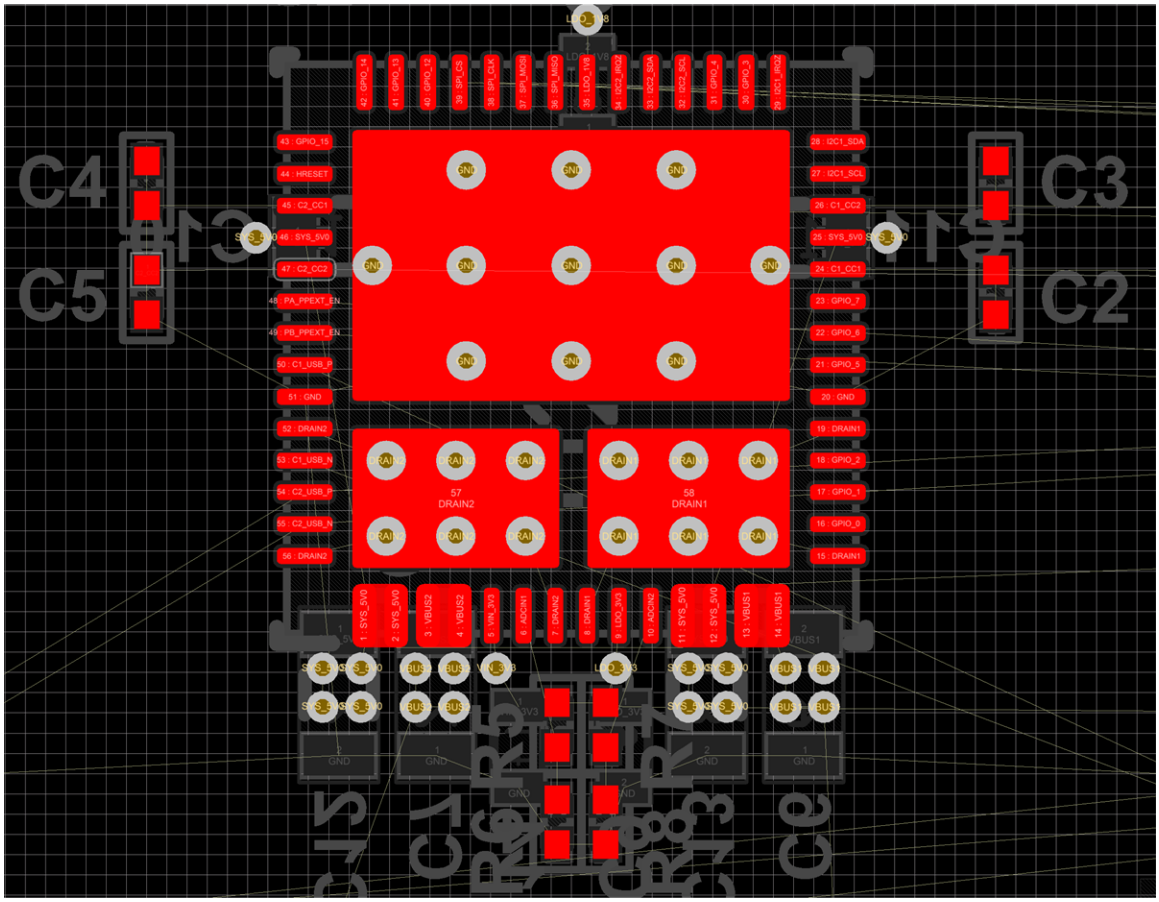


Figure 56. CC and ADCIN1/2 Component Placements

11.8 CC and SBU Protection Placement

The protection device should be placed close to the Type-C connector. In this layout example they are placed in between the Type-C connectors and the TPS65988DJ.

CC and SBU Protection Placement (continued)

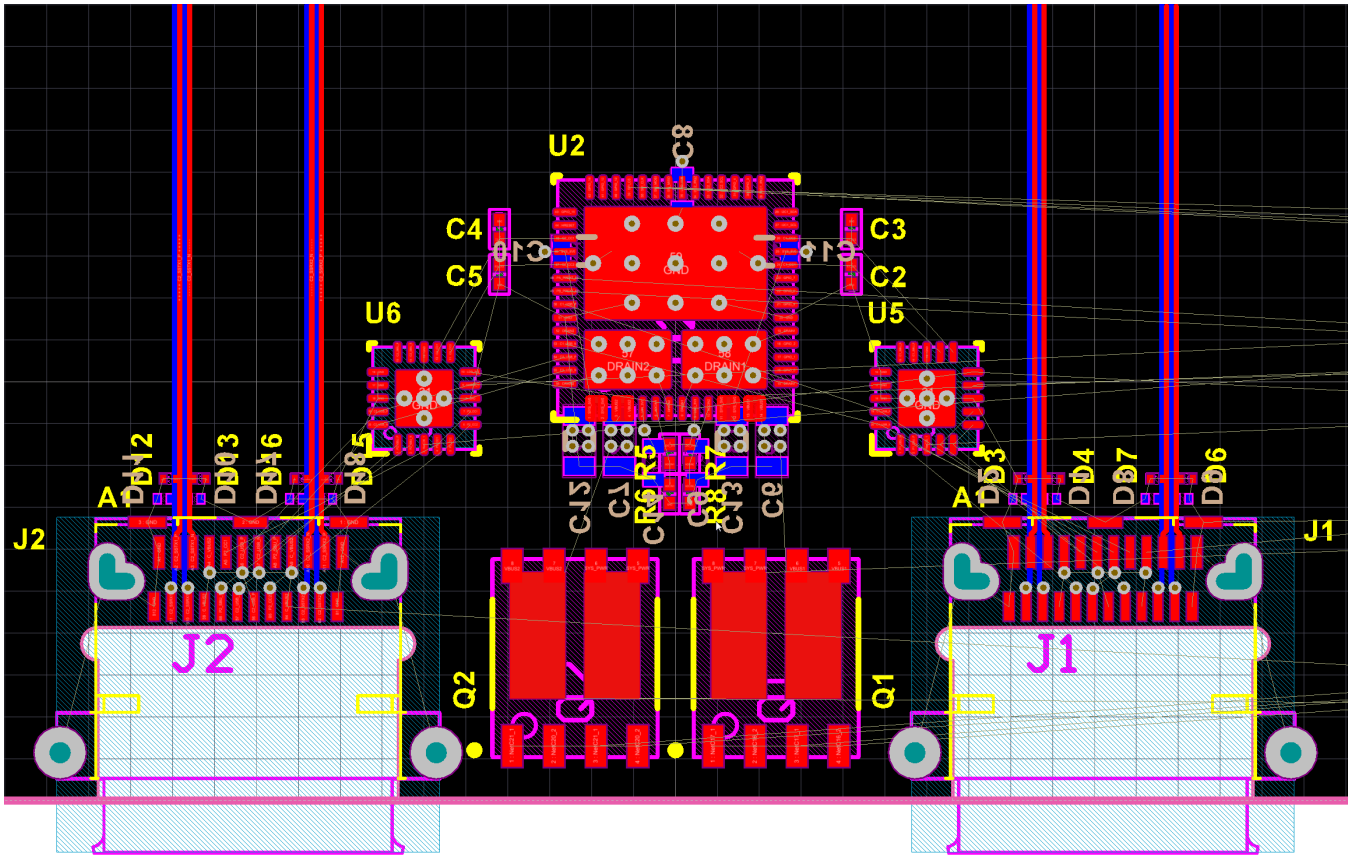


Figure 57. Protection Placement

11.9 CC Routing

Routing the CC lines with an 8 mil trace will guarantee the needed current for supporting powered Type C cables through VCONN. For more information on VCONN refer to the Type C specification. For capacitor GND pin use a 16 mil trace when possible. GPIO signals can be fanned out on the top layer with a 4 mil trace. Table 31 summarizes the minimum trace widths for these signals.

Table 31. Recommended Minimum Widths

Route	Minimum Width (mils)
CC1, CC2, PP_CABLE1, PP_CABLE2	8
VIN_3V3, LDO_3V3, LDO_1V8	6
Component GND	10
GPIO	4

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Figure 58 shows the CC routing from the connector to the protection device and to the TPS65988DJ.

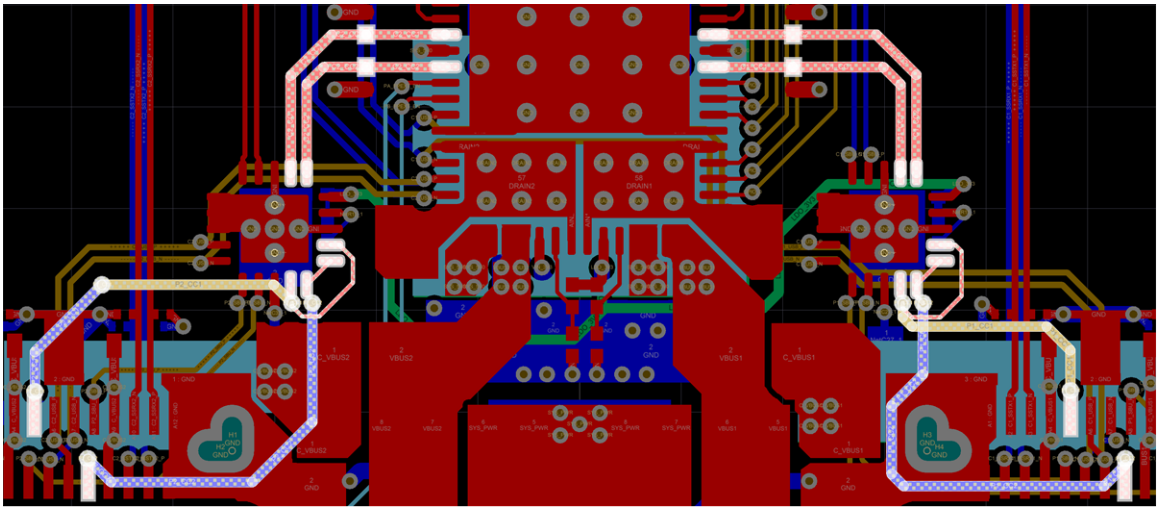


Figure 58. Complete CC Routing

11.10 DRAIN1 and DRAIN2 Pad Pours

The drain pads are used for dissipating heat from the two power paths. DRAIN1 and DRAIN2 should NEVER be connected to each other or to GND. They should be left floating with their own nets assigned. The top layer should have all of the DRAIN1 pins tied to the DRAIN1 pan and the DRAIN2 pins tied to the DRAIN2 pad. When high currents are expected in the system it is recommended to place “fins” on the DRAIN1 and DRAIN2 pads. The effective heat dissipation distance is roughly 3 mm from the pad so it does not have to extend to a large area. Figure 59 shows the top layer routing for DRAIN1 and DRAIN2.

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DRAIN1 and DRAIN2 Pad Pours (continued)

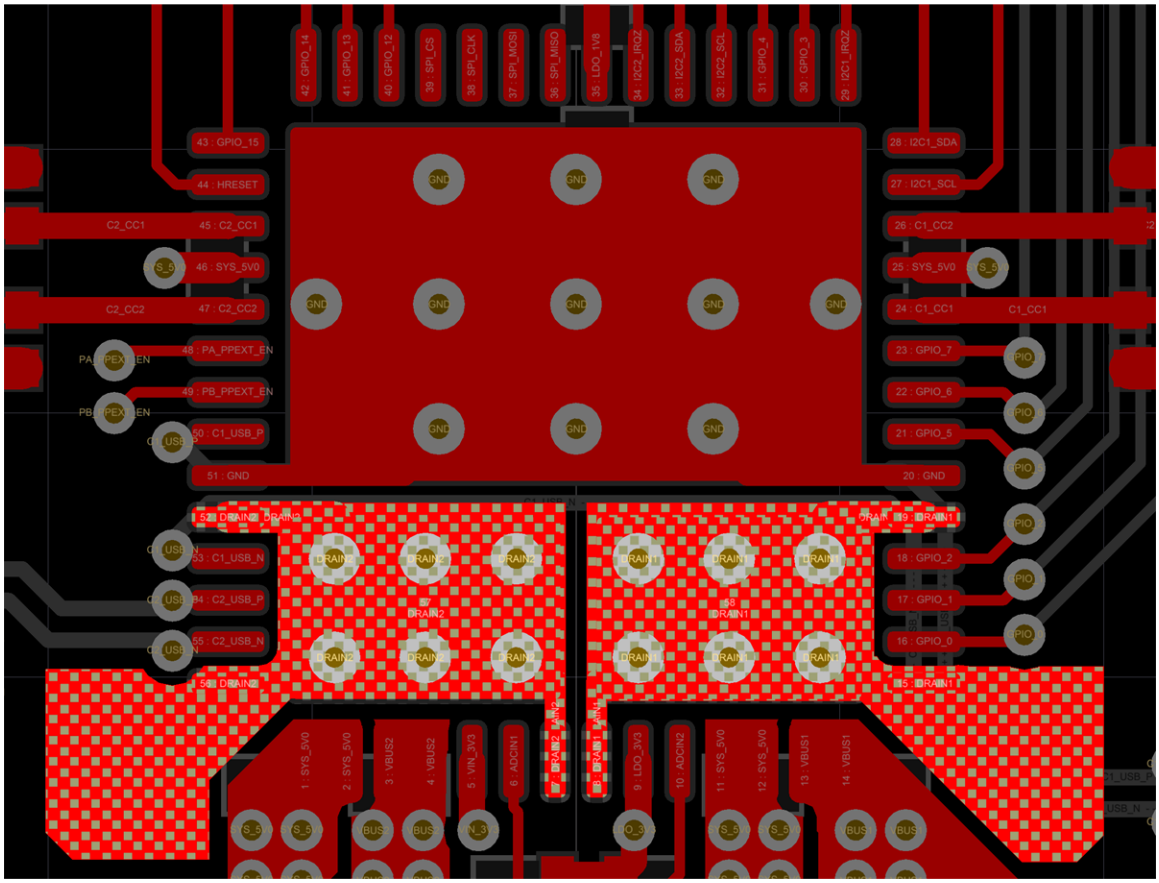


Figure 59. DRAIN1 and DRAIN2 Top Layer

On the bottom layer DRAIN1 and DRAIN2 pour are also required and it is recommended to have a larger pour than the DRAIN1 and DRAIN2 pads. The bottom layer will provide most of the heat dissipation and space should be reserved for the pours. Figure 60 shows the bottom layer routing for the DRAIN1 and DRAIN2 pads.

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DRAIN1 and DRAIN2 Pad Pours (continued)

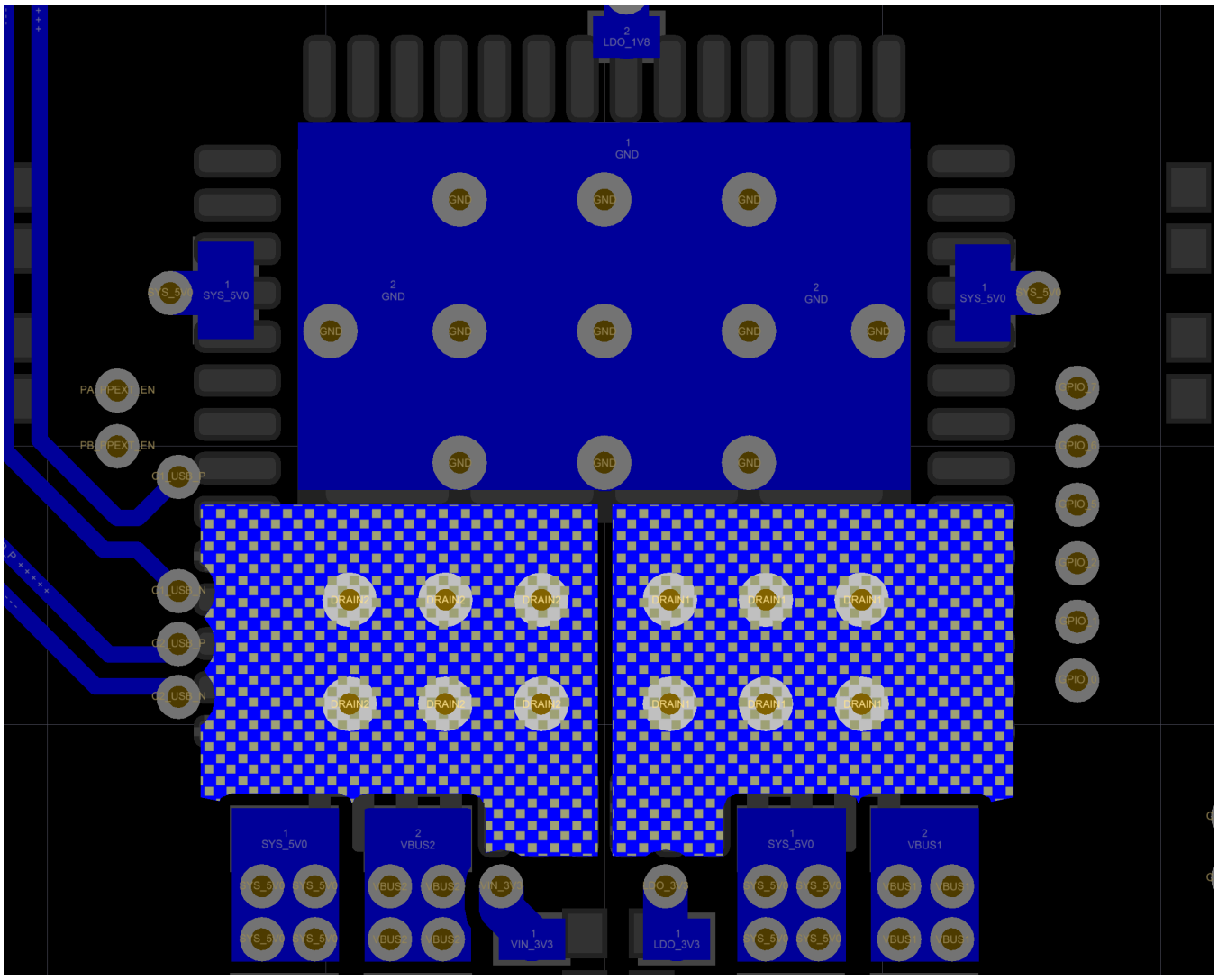


Figure 60. Figure 13. DRAIN1 and DRAIN2 Bottom Layer

11.11 USB2 Routing for ESD Protection and BC1.2

When routing the USB2 signals to the TPS65988DJ BC1.2 detection pins and the ESD protection to the TPS6S300 protection device, it is recommended to reduce the amount of excess trace to all of the pins. This will cause antennae and degrade signal integrity. The USB top/bottom signals are shorted together in this example and the same approach can be used if an external USB mux is used. There are several approaches that can be used to get optimal routing; “tap” the USB2 signals with vias that connect the TPS65988DJ pins, via up to the layer where the pins are located and continue to route on that layer, or a combination of both.

In this layout example, the D+/D- lines are routed to an internal layer from the connector. They are then via’d up to the pins on the devices. The figure below show the complete USB2 routing on SSTX1RX1, High Speed, and SSTX2RX2 layers.

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USB2 Routing for ESD Protection and BC1.2 (continued)

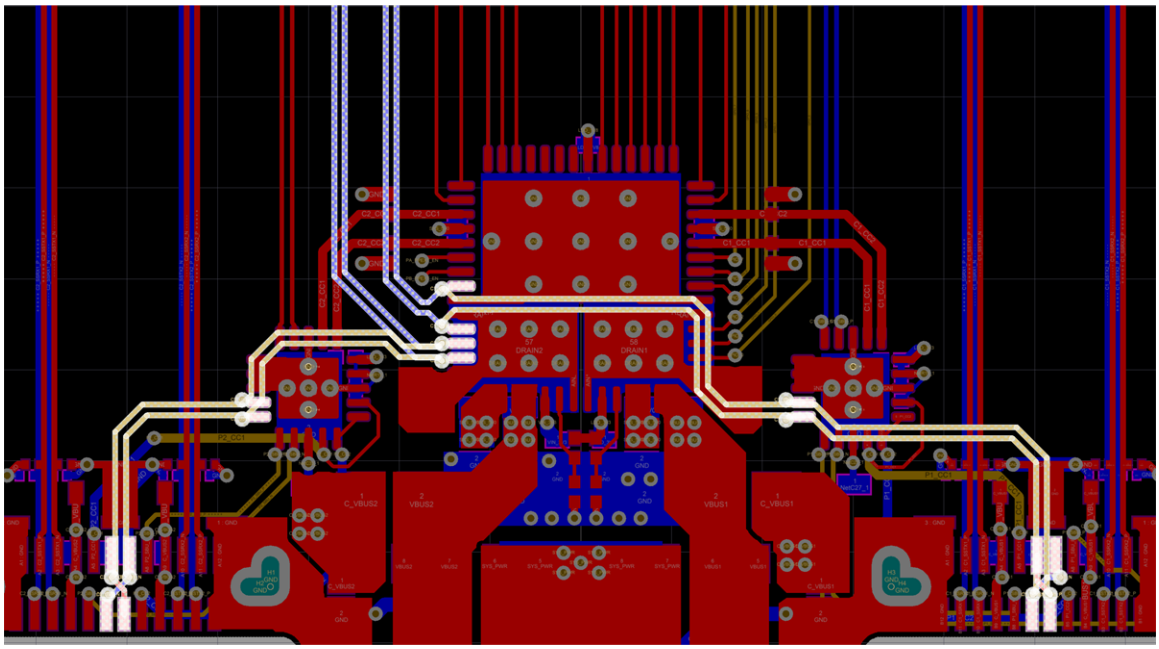


Figure 61. Complete USB2 Routing

11.12 VBUS Routing

When higher current are required in the system and there are space constraints it is recommended to stack power planes to help carry the higher currents. These are mostly used at the Type-C connector where most of the room will be reserved for SSTX/RX, USB2, SBU and CC signals. Table 32 summarizes the recommended widths for various VBUS currents.

Table 32. Recommended Trace Width for VBUS Currents

VBUS Current	Trace Width (0.5 oz Copper)	Trace Width (1 oz Copper)
1.5 A	50 mil	30 mil
3 A	100 mil	60 mil
5 A	240 mil	120 mil

The figures below show the SSTXRX1, Power1, Power2 and SSTXRX2 layers and the VBUS routing for the two ports.

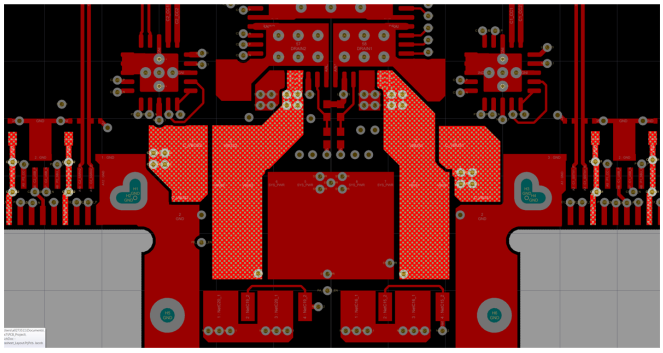


Figure 62. VBUS Routing Top Layer

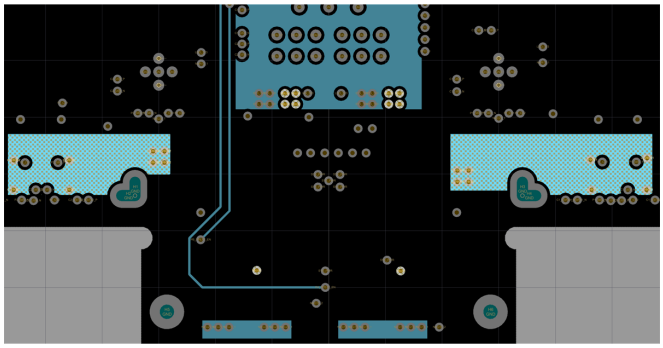


Figure 63. VBUS Routing Power 1

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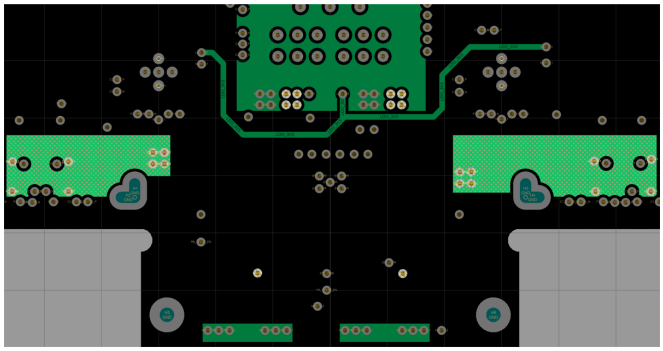


Figure 64. VBUS Routing Power 2

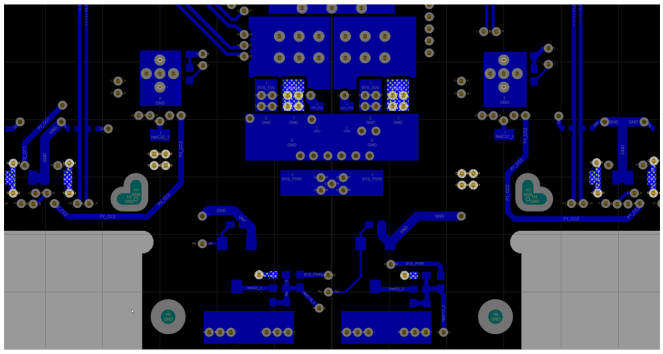


Figure 65. VBUS Routing Bottom Layer

11.13 Completed Layout

A dual port Type-C and PD system can easily be placed and routed in an area smaller than 1×2 inches allowing for Super Speed signals to be routed easily to the system. The figures below show the complete layout for all of the layers and 3D views of the PCB area.

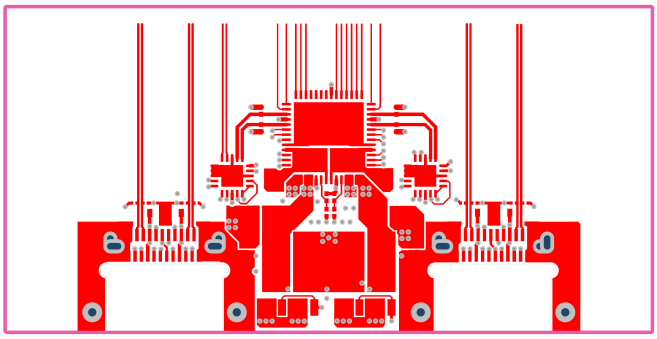


Figure 66. SSTXRX1 Layer

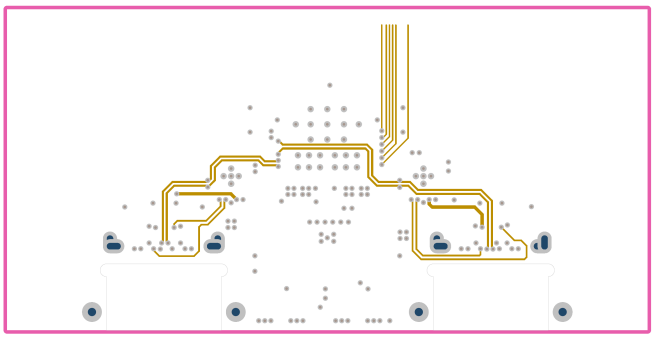


Figure 67. High Speed Layer

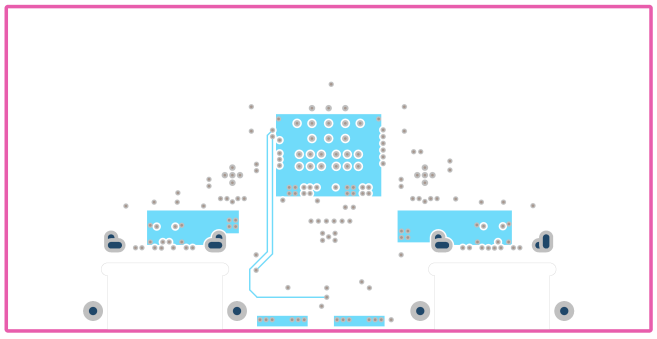


Figure 68. Power 1 Layer

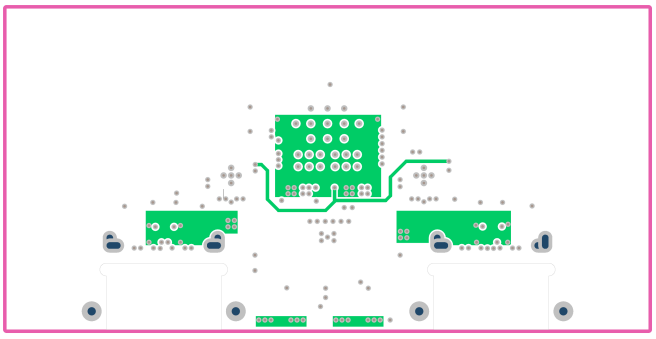


Figure 69. Power 2 Layer

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Completed Layout (continued)

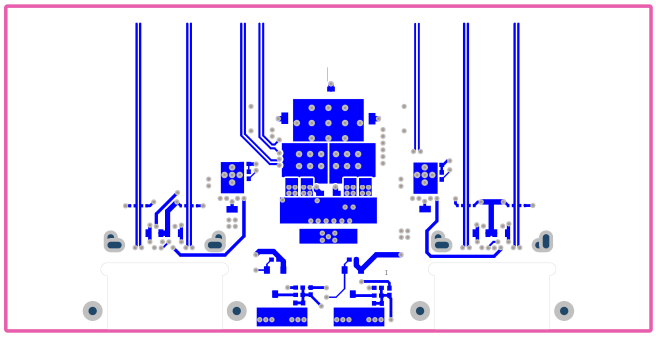


Figure 70. SSTXRX2 Layer

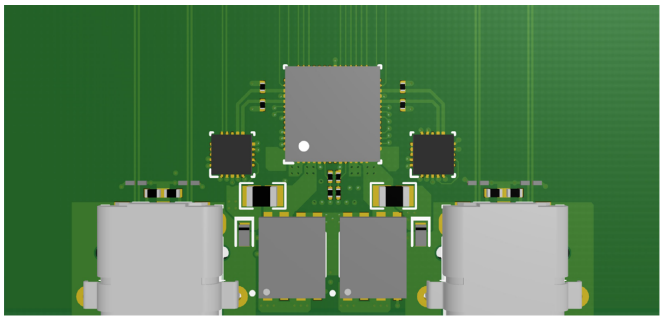


Figure 71. Top 3D View

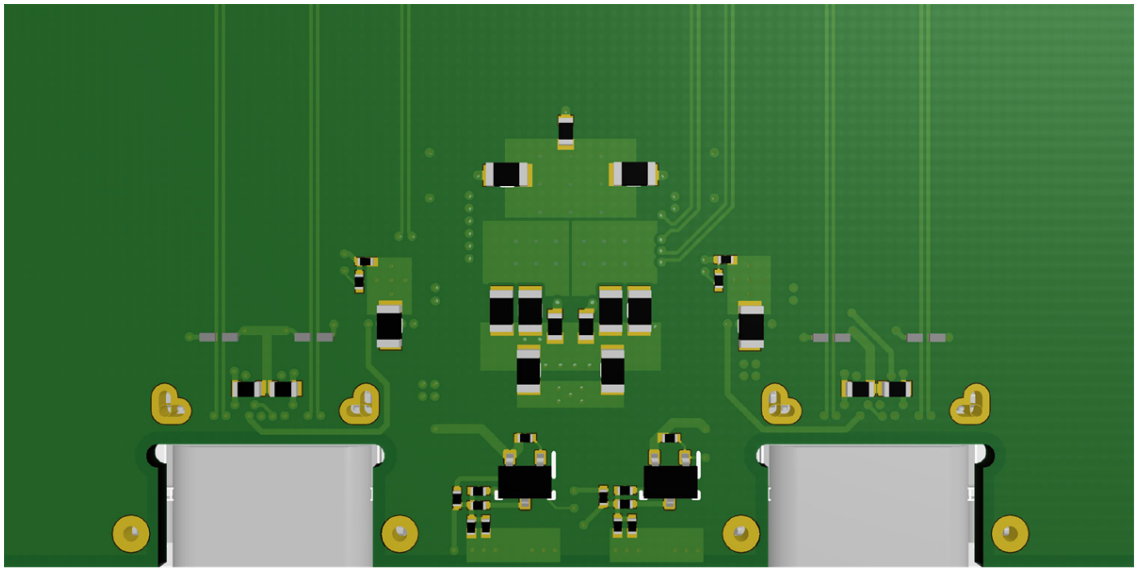


Figure 72. Bottom 3D View

11.14 Power Dissipation

The total power dissipation inside the TPS65988DJ should not cause the temperature of the power paths to exceed the maximum junction temperature of 150ºC or the controller to exceed the maximum junction temperature to exceed 125ºC.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

- *TUSB1064 USB TYPE-C™ DP Alt Mode 10 Gbps Sink-Side Linear Redriver Crosspoint Switch* data sheet

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65988DJRSHR	ACTIVE	VQFN	RSH	56	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-10 to 75	TPS65988 DJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

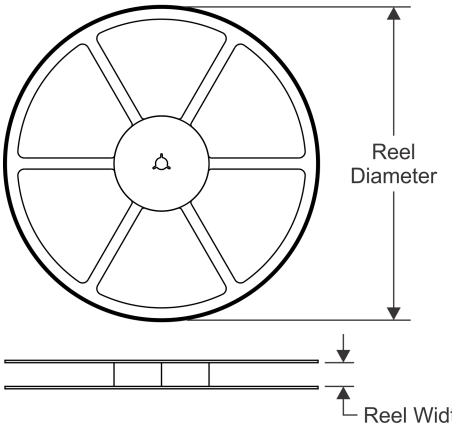
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

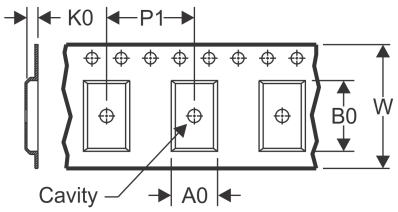
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

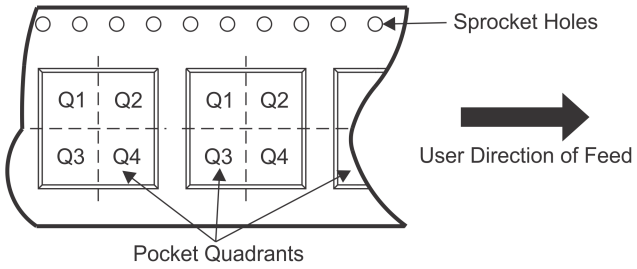


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

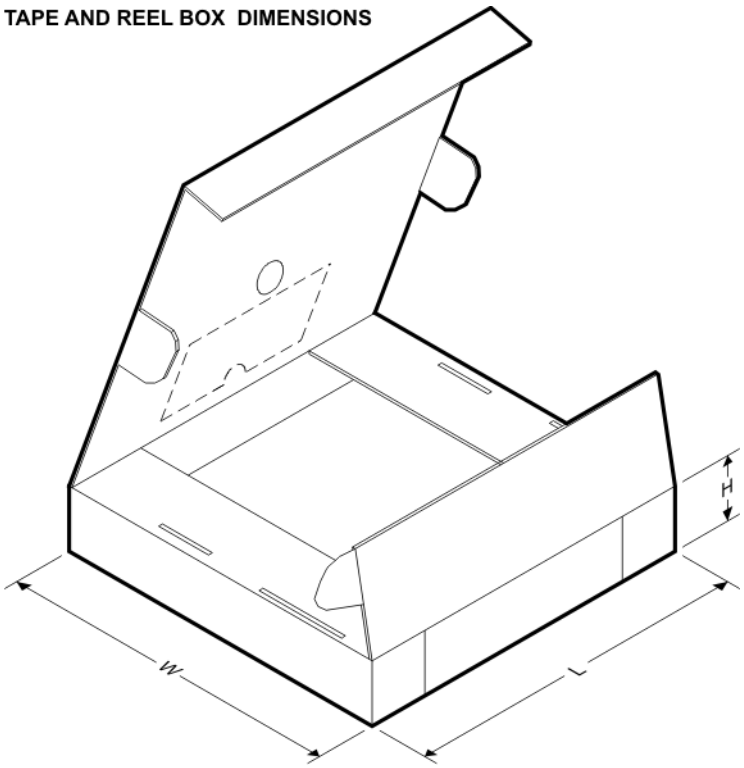
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65988DJRSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

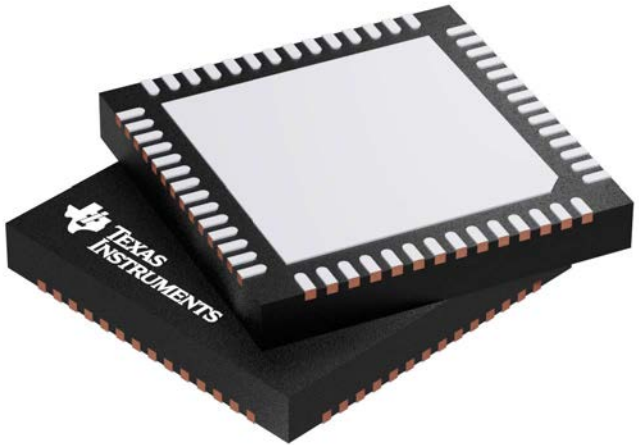
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65988DJRSHR	VQFN	RSH	56	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

RSH 56

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

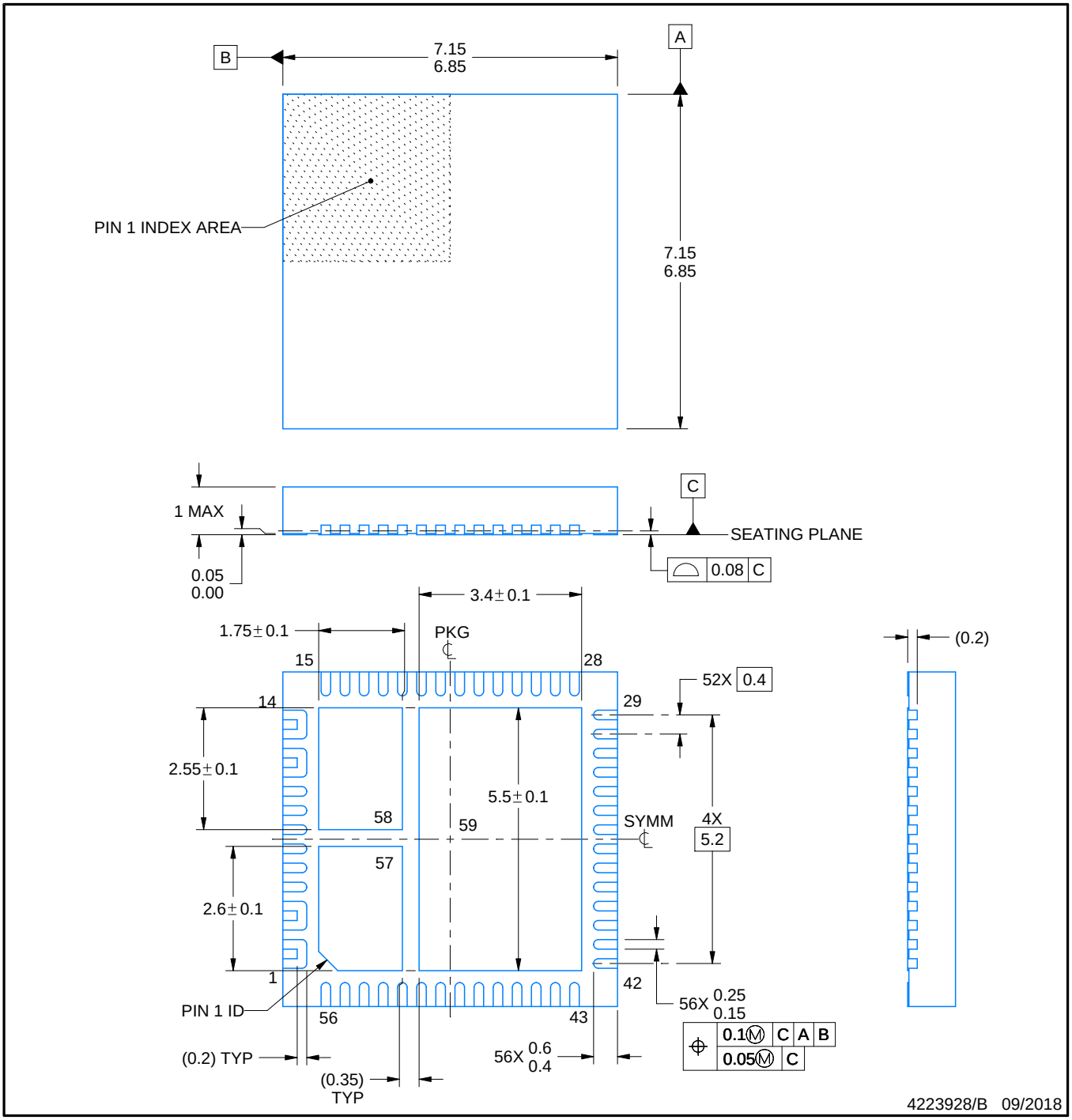
4207513/D

PACKAGE OUTLINE

RSH0056E

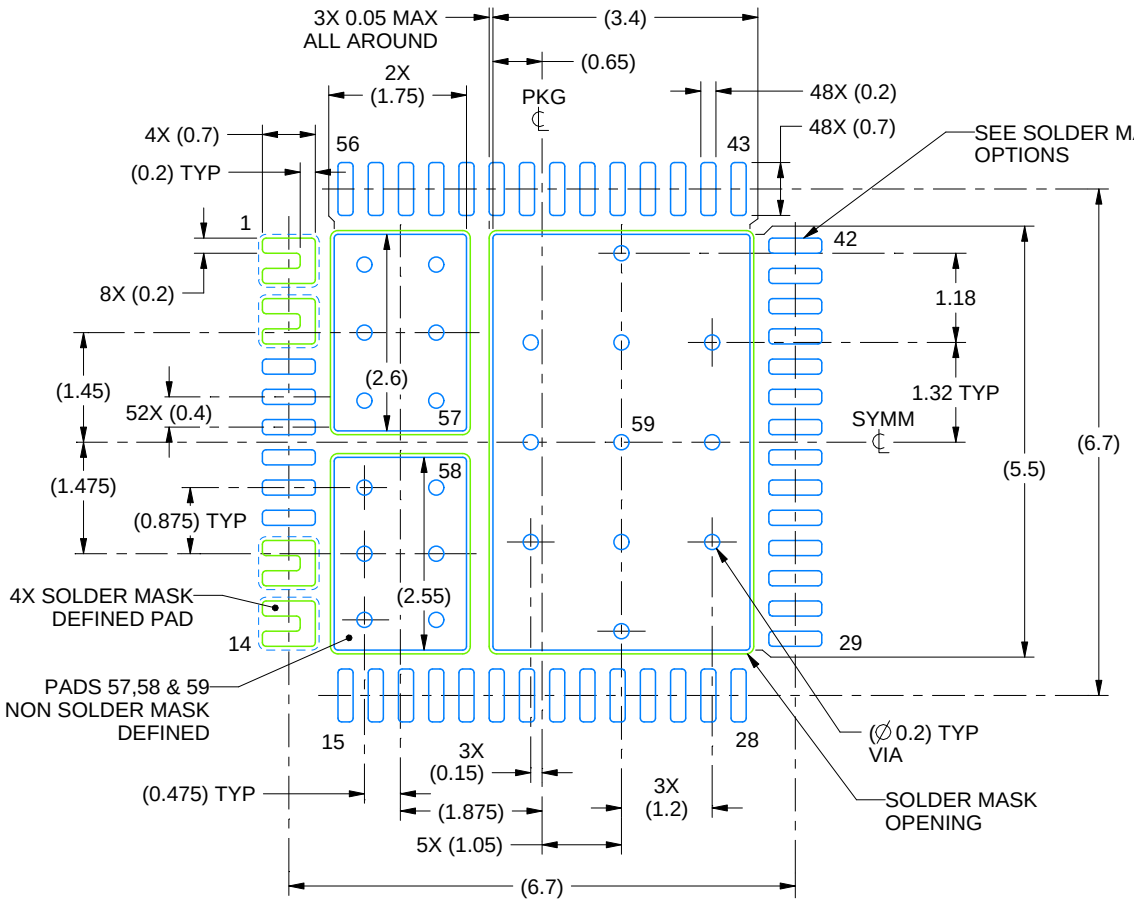
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

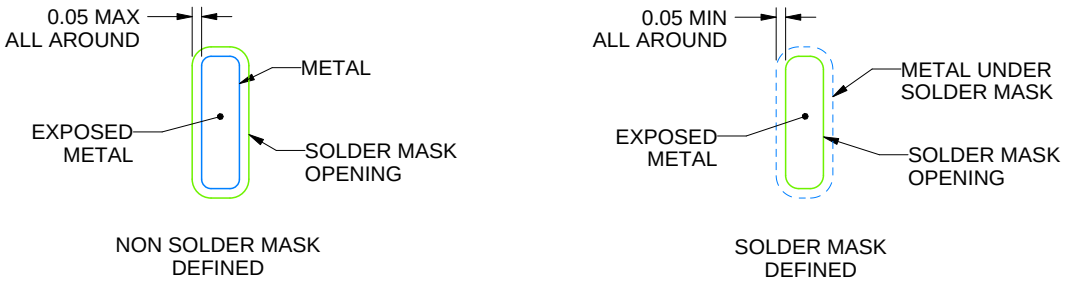


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

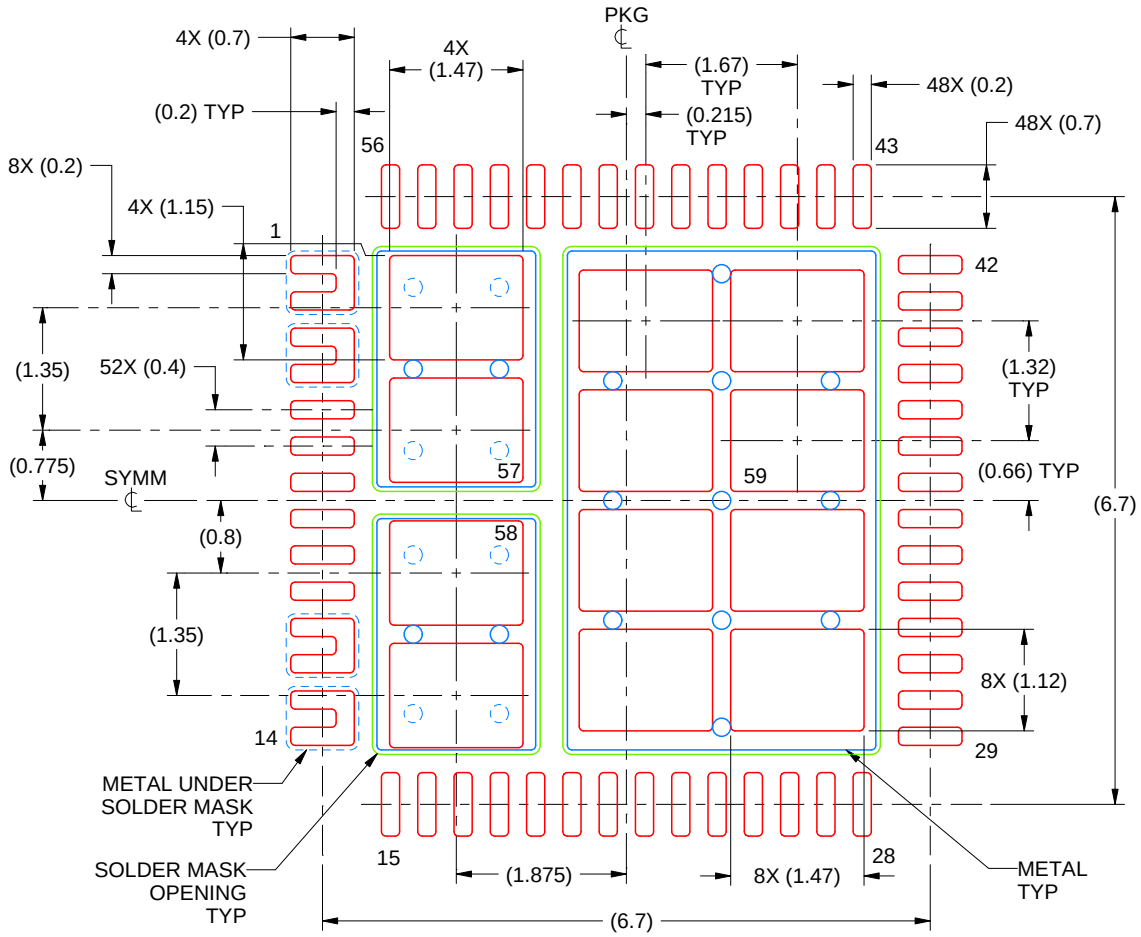


SOLDER MASK OPTIONS
NOT TO SCALE

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL

EXPOSED PAD PRINTED SOLDER COVERAGE BY AREA
PAD 57 & 58: 75%
PAD 59: 70%
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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