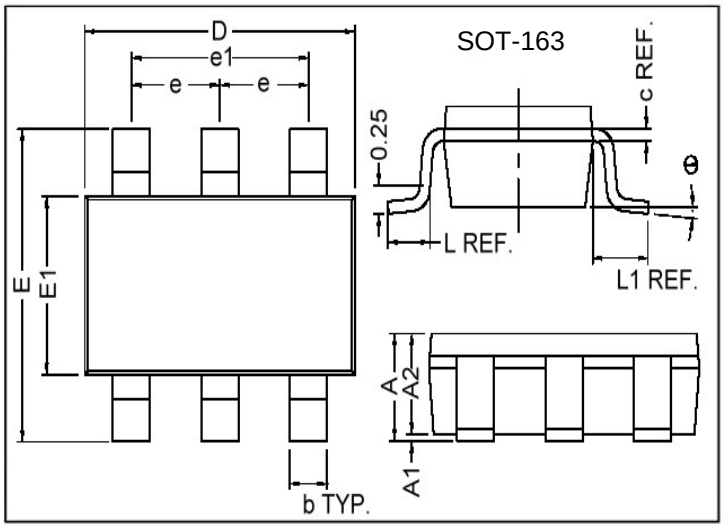
# 20V Dual N-Channel Enhancement Mode MOSFET

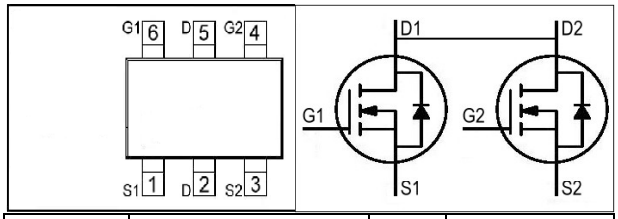
**VDS= 20V**
**RDS(ON), Vgs@2.5V, Ids@3.4A** < 46mΩ
**RDS(ON), Vgs@4.V, Ids@4.3A** < 30mΩ

## Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
High Power and Current handing capability
Ideal for Li ion battery pack applications

Package Dimensions




| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 1.10 MAX. | | L | 0.45 REF. | |
| A1 | 0 | 0.10 | L1 | 0.60 REF. | |
| A2 | 0.70 | 1.00 | θ | 0° | 10° |
| c | 0.12 REF. | | b | 0.30 | 0.50 |
| D | 2.70 | 3.10 | e | 0.95 REF. | |
| E | 2.60 | 3.00 | e1 | 1.90 REF. | |
| E1 | 1.40 | 1.80 | | | |

Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 12 | |
| Continuous Drain Current | | $I_D$ | 4 | A |
| Pulsed Drain Current [1] | | $I_{DM}$ | 25 | |
| Maximum Power Dissipation | TA = 25°C | $P_D$ | 1.4 | W |
| | TA = 75°C | | 1 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 150 | °C |
| Junction-to-Ambient Thermal Resistance (PCB mounted) [2] | | $R_{\theta JA}$ | 100 | °C/W |

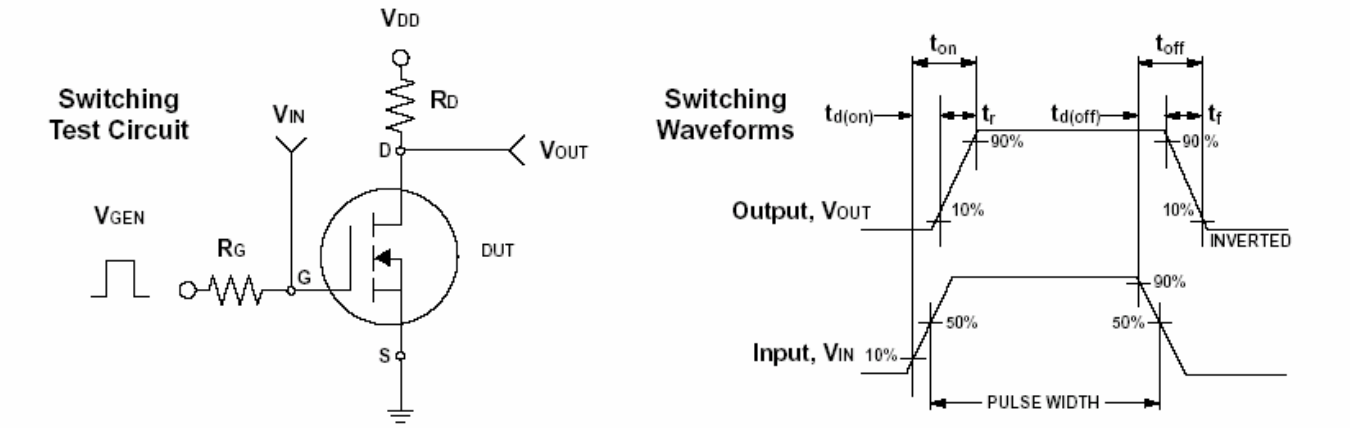
Notes
[1] Pulse width limited by maximum junction temperature.
[2] Surface Mounted on FR4 Board, t ≤ 5 sec.

## 20V Dual N-Channel Enhancement Mode MOSFET

### ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250uA | 20 | | | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 2.5V, $I_D$ = 3.4A | | 35 | 46 | mΩ |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 4.0V, $I_D$ = 4.3A | | 27 | 30 | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$, $I_D$ = 250uA | 0.5 | 0.8 | 1.5 | V |
| Zero Gate Voltage Drain Current 0 | $I_{DSS}$ | $V_{DS}$ = 16V, $V_{GS}$ = 0V | | | 1 | uA |
| Gate Body Leakage | $I_{GSS}$ | $V_{GS}$ = ± 8V, $V_{DS}$ = 0V | | | ±100 | nA |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 5V, $I_D$ = 4A | | 10 | __ | S |
| **Dynamic** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10V, $I_D$ = 4A<br>$V_{GS}$ = 4V | | 11 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 2.2 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 2.5 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10V, $R_G$ = 10Ω<br>$I_D$ = 1A, $V_{GS}$ = 4V | | 18.3 | | ns |
| Turn-On Rise Time | $t_r$ | | | 4.8 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 43.5 | | |
| Turn-Off Fall Time | $t_f$ | | | 20 | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 8V, $V_{GS}$ = 0V<br>f = 1.0 MHz | | 800 | | pF |
| Output Capacitance | $C_{oss}$ | | | 155 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 125 | | |
| **Source-Drain Diode** | | | | | | |
| Max. Diode Forward Current | $I_S$ | | | 2 | | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = 1.7A, $V_{GS}$ = 0V | | 0.8 | 1.2 | V |

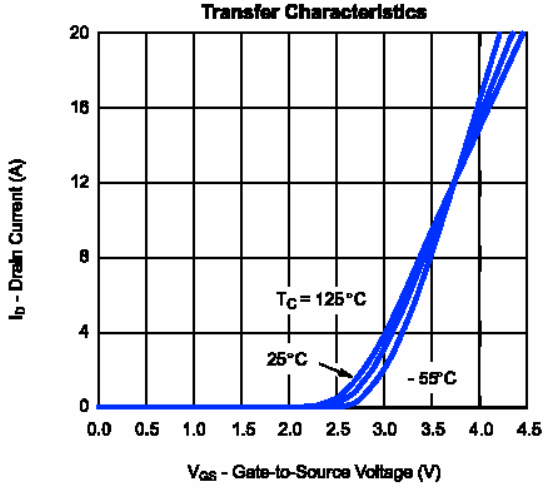
Note:Pulse test: pulse width <= 300us, duty cycle<= 2%



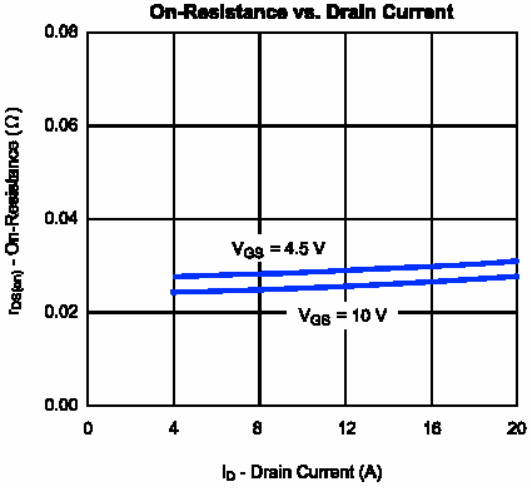
## 20V Dual N-Channel Enhancement Mode MOSFET

### Typical Characteristics ($T_J$ =25℃ Noted)

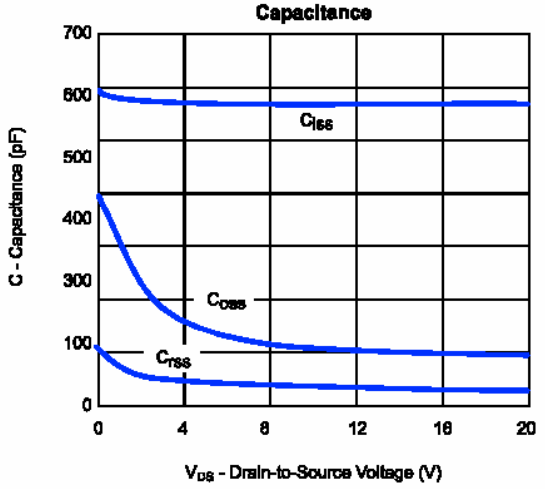
**Transfer Characteristics**



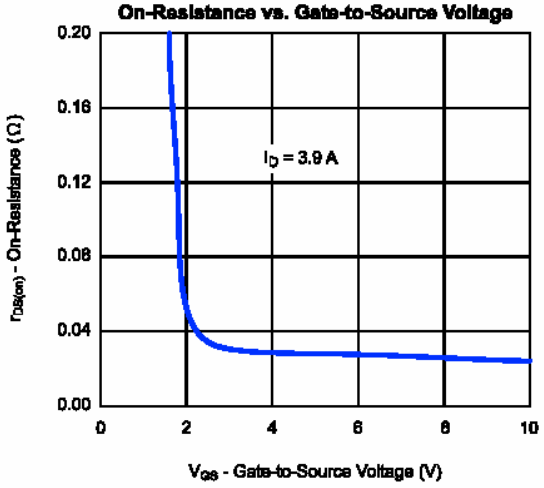

**On-Resistance vs. Drain Current**



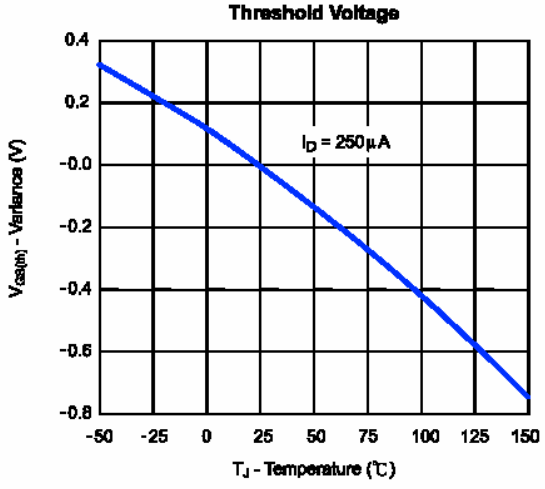

**Capacitance**




**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**




**On-Region Characteristics**

