



STD16NF06L STD16NF06L-1

N-channel 60V - 0.060Ω - 24A - DPAK/IPAK
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STD16NF06L-1	60V	<0.070Ω	24A
STD16NF06L	60V	<0.070Ω	24A

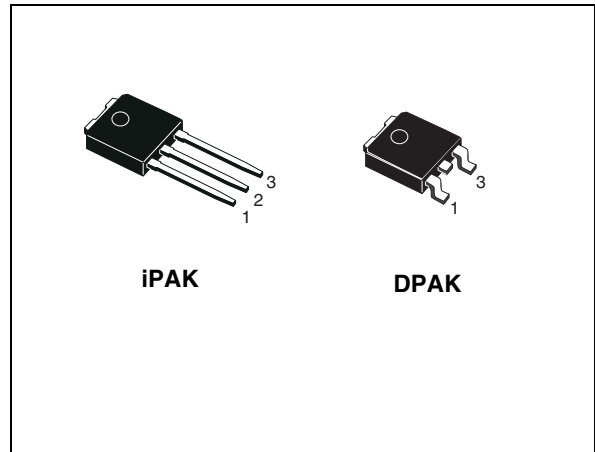
- Logic level device
- Low threshold drive

Description

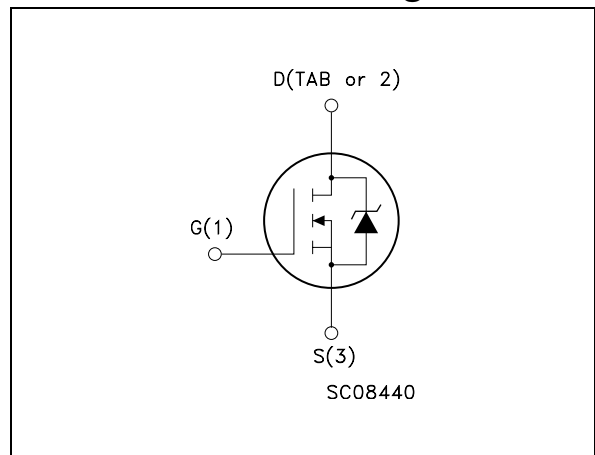
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD16NF06L-1	D16NF06L	IPAK	Tube
STD16NF06LT4	D16NF06L	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	60	V
V_{GS}	Gate- source voltage	± 18	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	24	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	17	A
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	40	W
	Derating Factor	0.27	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery avalanche energy	11.5	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	200	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 6\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 20\text{A}$, $V_{DD} = 48\text{V}$

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	3.75	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-to PCB max	62	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose ⁽¹⁾	300	$^\circ\text{C}$

1. When Mounted on 1 inch² FR-4 board, 2 oz. of Cu.

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 18\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 8\text{A}$ $V_{GS} = 5\text{V}$, $I_D = 8\text{A}$		0.060 0.070	0.070 0.085	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 12\text{A}$		12		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		370		pF
C_{oss}	Output capacitance			69		pF
C_{rss}	Reverse transfer capacitance			30		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{V}$, $I_D = 8\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 5\text{V}$ (see Figure 13)		12		ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turn-off delay time			20		ns
t_f	Fall time			6		ns
Q_g	Total gate charge	$V_{DD} = 30\text{V}$, $I_D = 8\text{A}$, $V_{GS} = 5\text{V}$, $R_G = 4.7\Omega$ (see Figure 14)		7.5		nC
Q_{gs}	Gate-source charge			2.5		nC
Q_{gd}	Gate-drain charge			4.2		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				16 64	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16A$, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 16A$, $di/dt = 100A/\mu s$, $V_{DD} = 25V$, $T_j = 150^\circ C$ (see Figure 15)		53 85 3.2		ns μC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

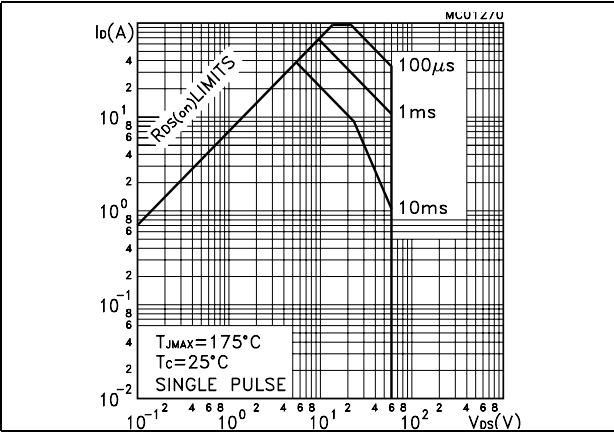


Figure 2. Thermal impedance

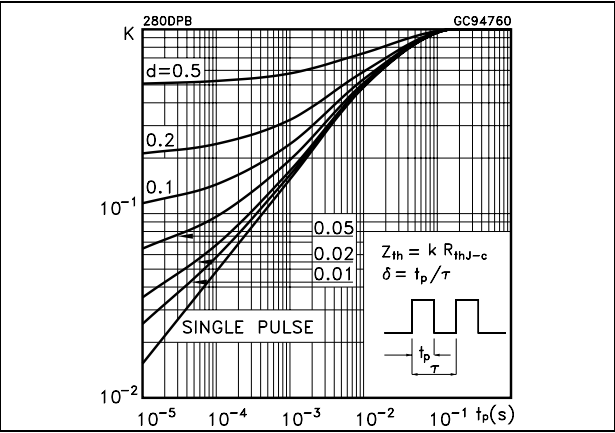


Figure 3. Output characteristics

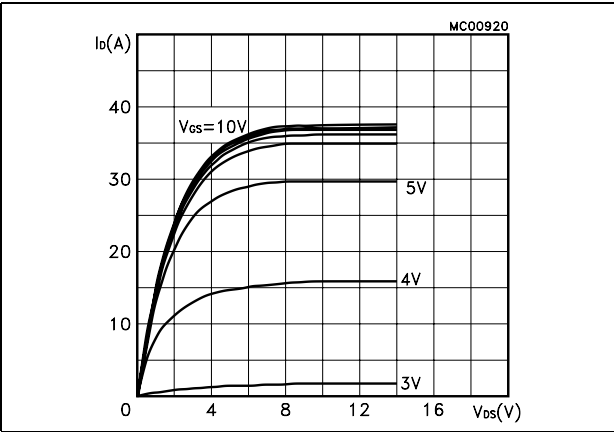


Figure 4. Transfer characteristics

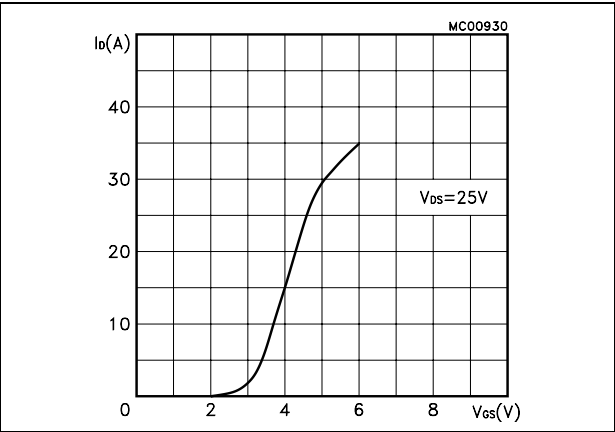


Figure 5. Transconductance

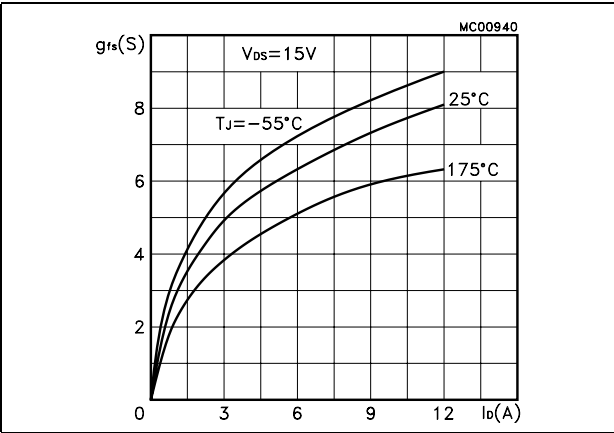


Figure 6. Static drain-source on resistance

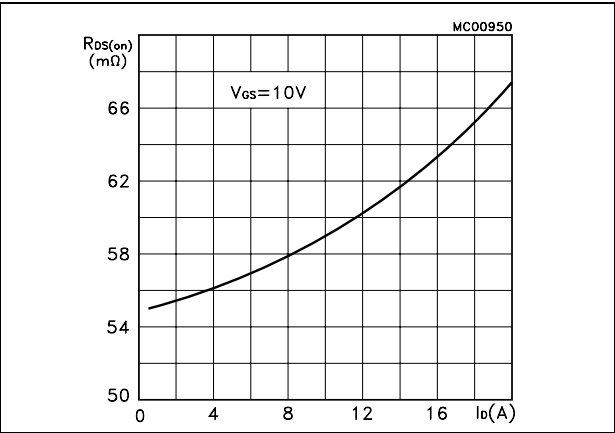


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

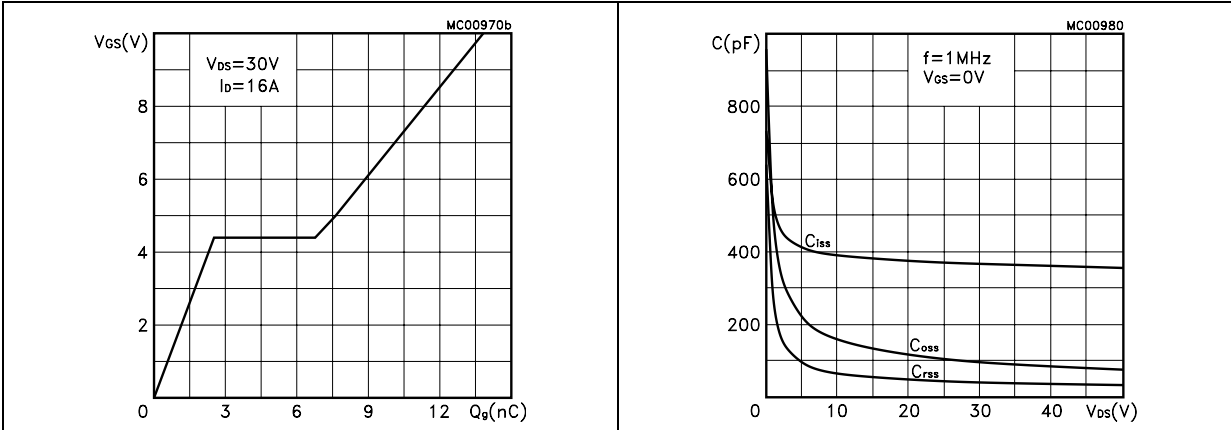


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

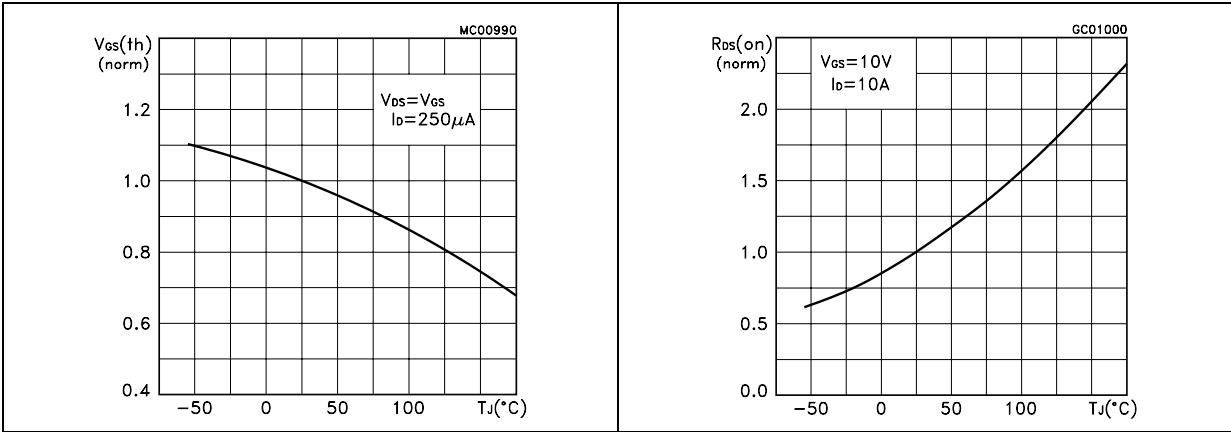
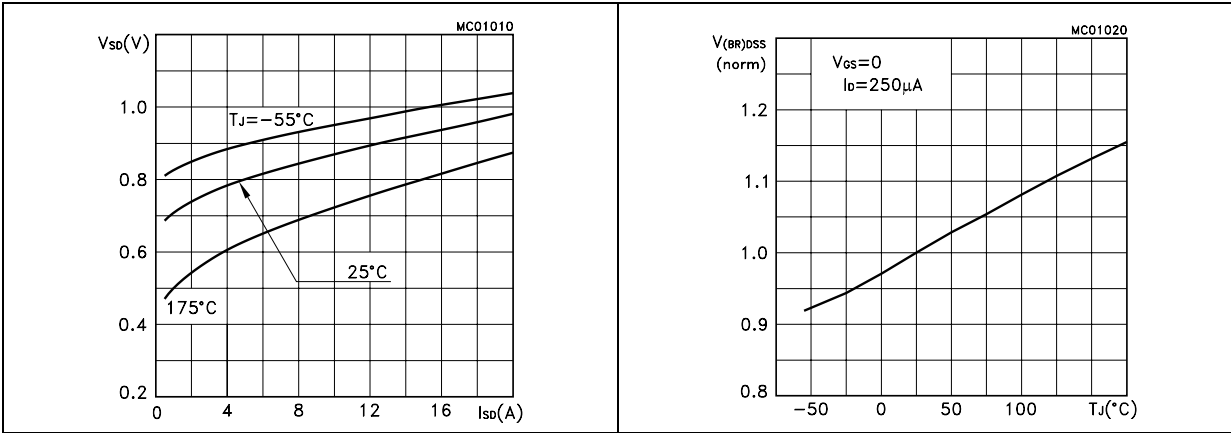


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs. temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

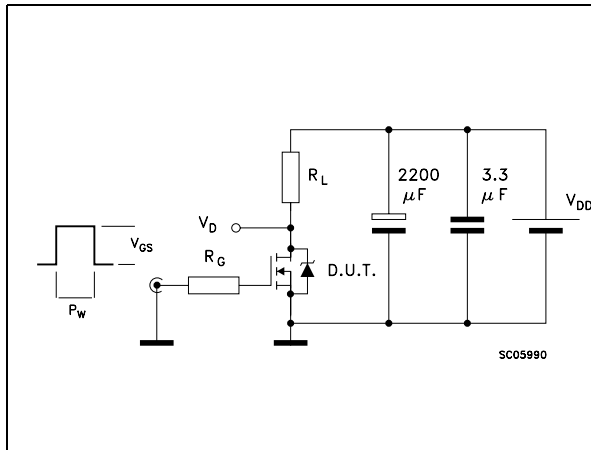


Figure 14. Gate charge test circuit

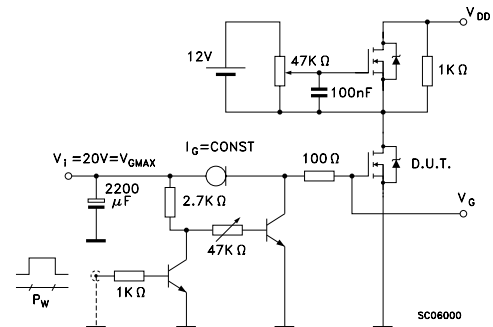


Figure 15. Test circuit for inductive load switching and diode recovery times

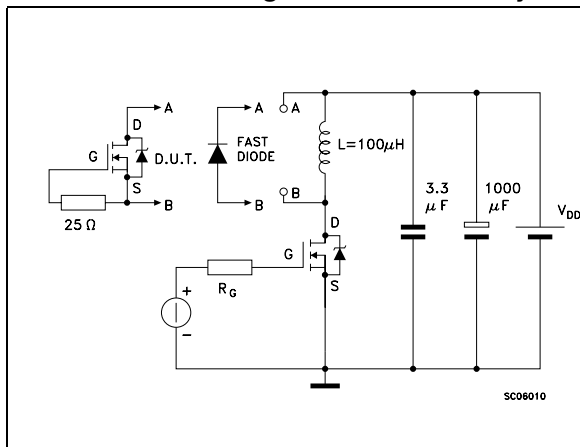


Figure 16. Unclamped Inductive load test circuit

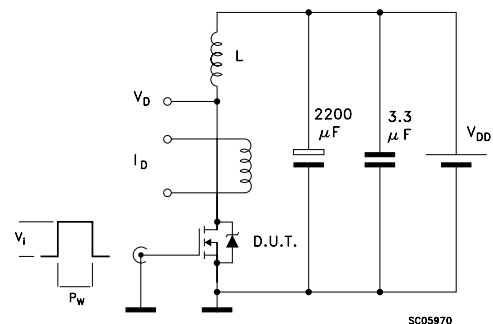


Figure 17. Unclamped inductive waveform

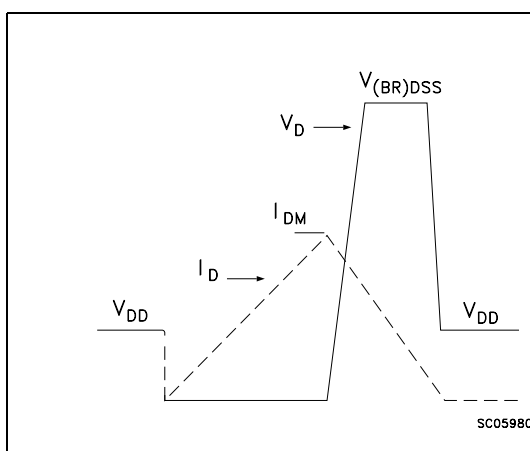
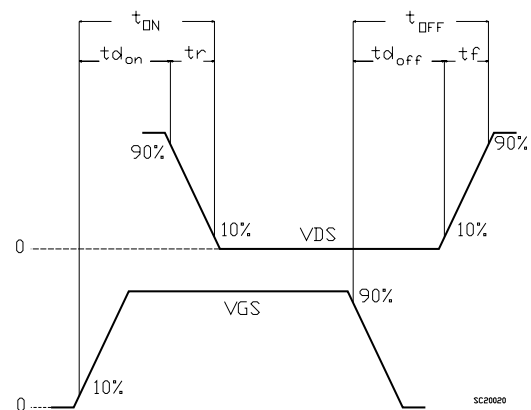


Figure 18. Switching time waveform

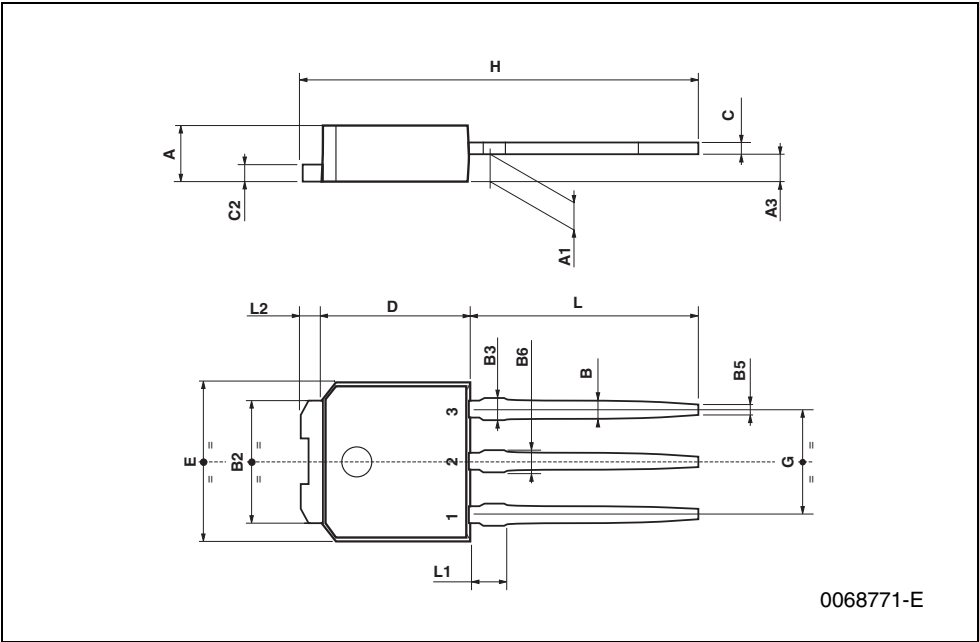


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



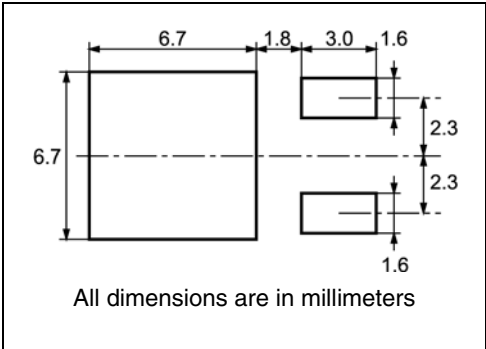
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the DPAK package geometry. It includes a top view showing dimensions E, b4, L2, L4, H, e, e1, and b(2x). A side view shows dimensions A, c2, L, D, A1, R, and c. A detail view of the lead shows dimensions E1, D1, A2, L, (L1), V2, and a gauge plane at 0.25. A thermal pad is also indicated.

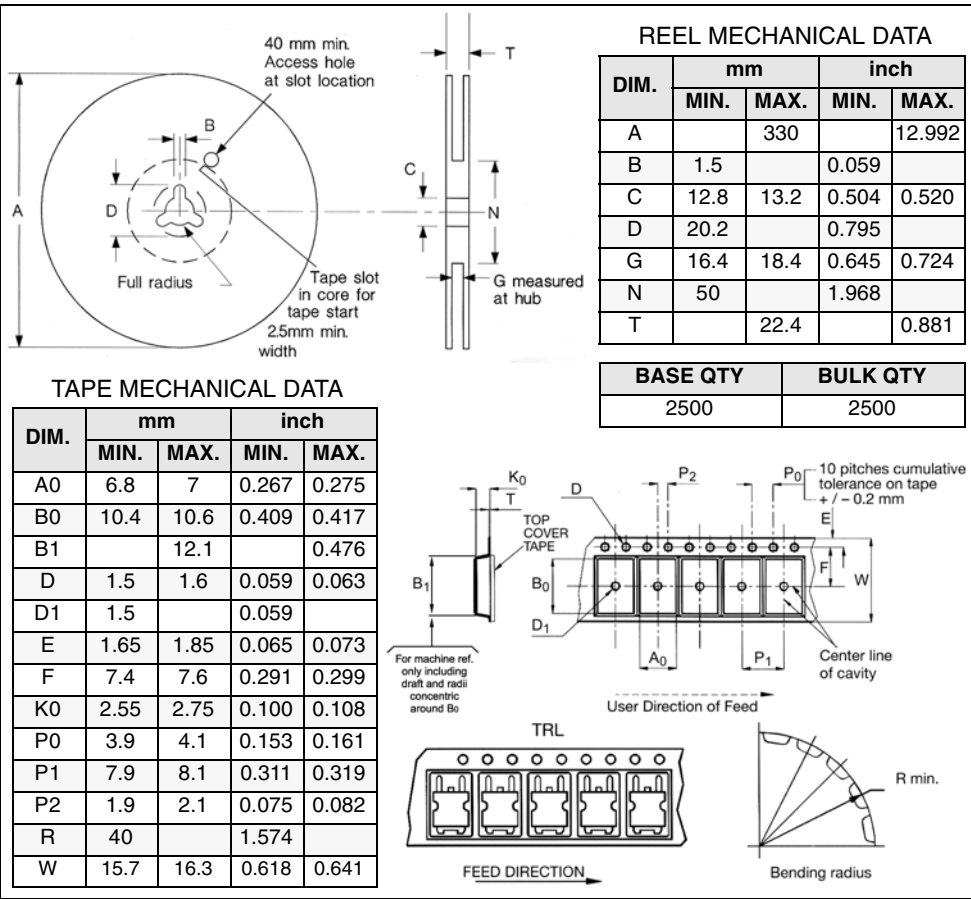
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5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 6. Revision history

Date	Revision	Changes
28-Feb-2005	1	Initial release
03-Mar-2005	2	Preliminary version
29-Nov-2005	3	Added package IPAK
03-Jul-2006	4	New template, no content change
19-Feb-2007	5	Typo mistake on page 1

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