

# Low-Voltage CMOS 18-Bit Universal Bus Transceiver

## With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16500 is a high performance, non-inverting 18-bit universal bus transceiver operating from a 2.7 to 3.6V supply. This part is not byte controlled; it is "18-bit" controlled. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX16500 inputs to be safely driven from 5V devices. The MC74LCX16500 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data flow in each direction is controlled by Output Enable (OEAB, OEBA), Latch Enable (LEAB, LEBA) and Clock inputs (CAB, CBA). When LEAB is HIGH, the A-to-B dataflow is transparent. When LEAB is LOW, and CAB is held at LOW or HIGH, the data A is latched; on the HIGH-to-LOW transition of CAB the A-data is stored in the latch/flip-flop. The outputs are active when OEAB is HIGH. When OEAB is LOW the B-outputs are in 3-state. Similarly, the LEBA, OEBA and CBA control the B-to-A dataflow. Please note that the output enables are complementary; OEAB is active HIGH, OEBA is active LOW.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation
- 6ns Maximum  $t_{pd}$
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

# MC74LCX16500

# LCX

## LOW-VOLTAGE CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER



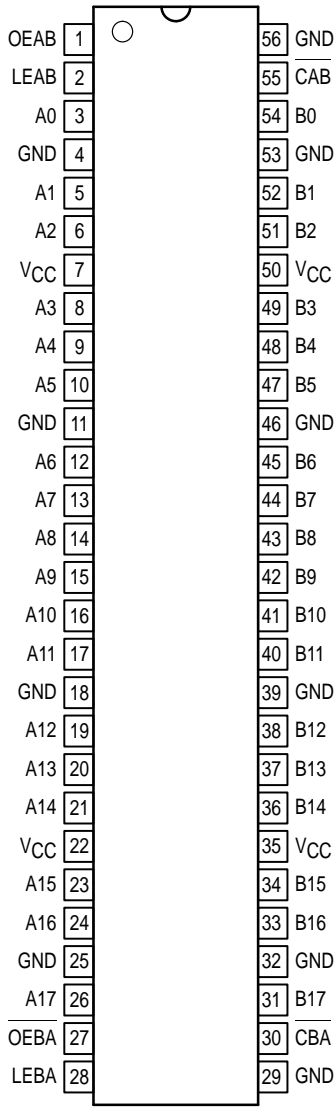
**DT SUFFIX**  
56-LEAD PLASTIC TSSOP PACKAGE  
CASE 1202-01

**PIN NAMES**

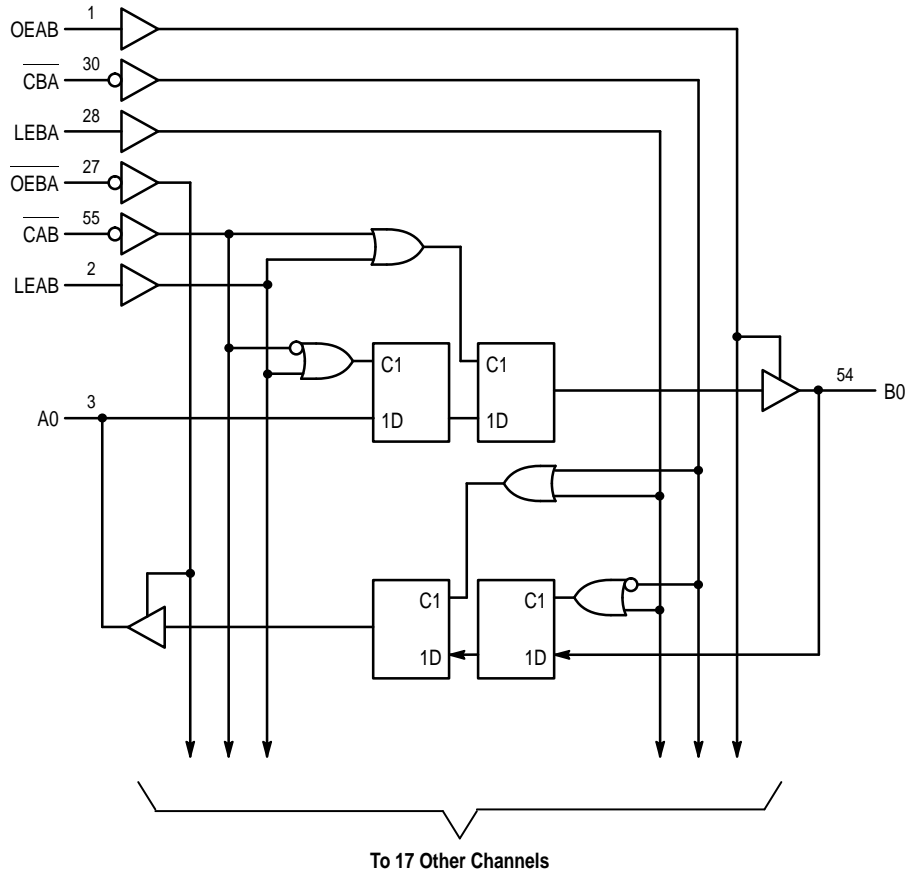
Pins	Function
OEAB, OEBA	Output Enable Inputs
CAB, CBA	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
A0-A17	Side A Inputs/Outputs
B0-B17	Side B Inputs/Outputs



# MC74LCX16500



**Figure 1. 56-Lead Pinout**  
(Top View)



**Figure 2. Logic Diagram**

FUNCTION TABLE

Inputs						Data Ports		Operating Mode
OEAB	OEBA	LEAB	LEBA	CAB	CBA	An	Bn	
L	H					Input	Input	
		L	L	H or L	H or L	X	X	Hold Data; A and B Outputs Disabled
				↓	↓	l h	l h	Clock A and/or B Data; A and B Outputs Disabled
H	H					Input	Output	
		L	X	H or L	X*	X	QA	Hold and Display B Data
				↓	X*	l h	L H	Clock A Data to B Bus; Store A Data
H	X	X	X*	L H	L H	A Data to B Bus; (Transparent)		
L	L					Output	Input	
		X	L	X*	H or L	QB	X	Hold and Display A Data
				X*	↓	L H	l h	Clock B Data to A Bus; Store B Data
X	H	X*	X	L H	L H	B Data to A Bus; (Transparent)		
H	L					Output	Output	
		L	L	H or L	H or L	QB	QA	Stored A Data to B Bus; Stored B Data to A Bus

H = High Voltage Level; L = Low Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Clock High-to-Low Transition; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Clock High-to-Low Transition; X = Don't Care; ↓ = High-to-Low Clock Transition; QA = A Input Storage Register; QB = B Input Storage Register; \* = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I<sub>CC</sub> reasons, Do Not Float Inputs.

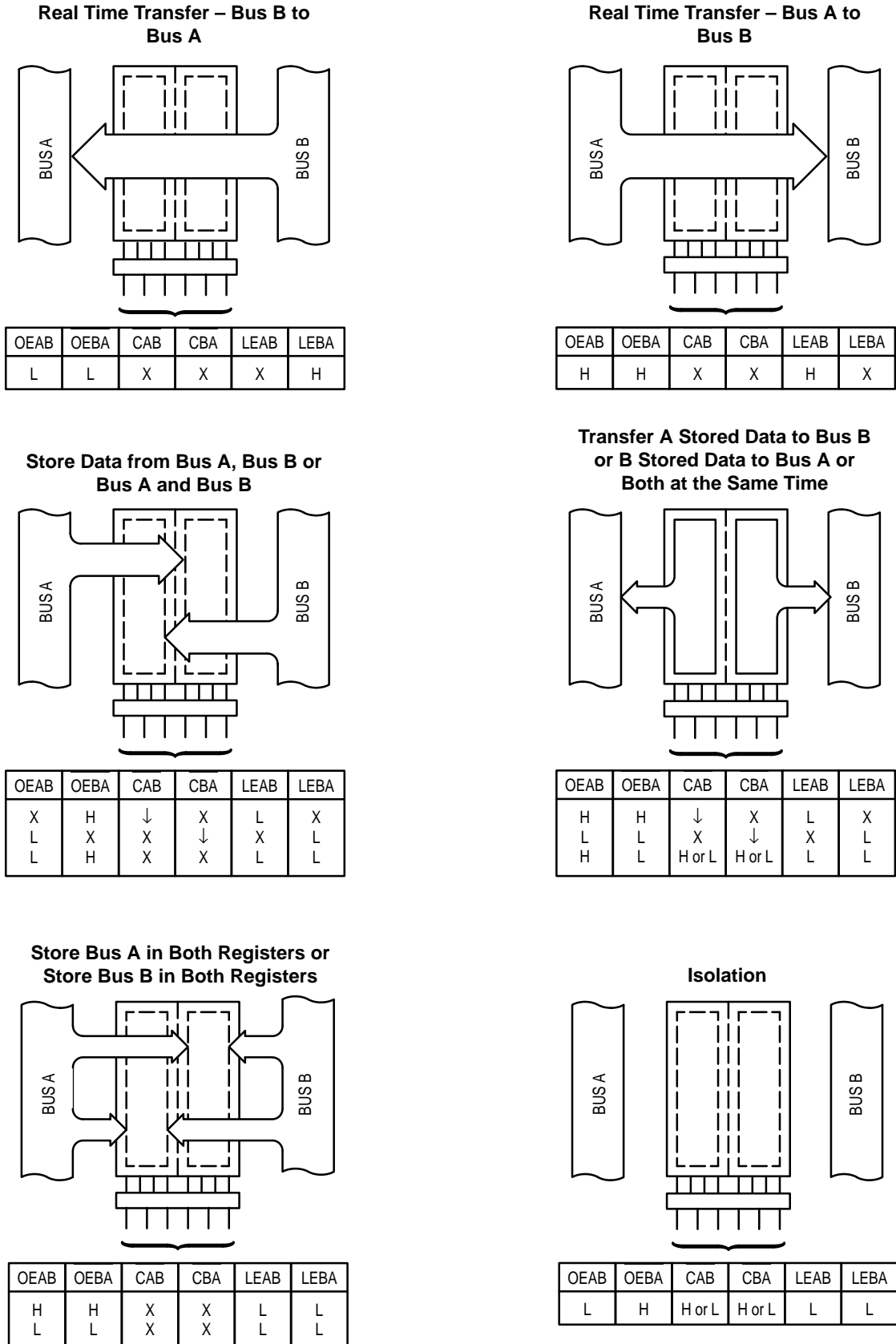


Figure 3. Bus Applications

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Note 1.	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I<sub>O</sub> absolute maximum rating must be observed.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating	2.0	3.3	3.6	V
		Data Retention Only	1.5	3.3	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V	
V <sub>O</sub>	Output Voltage (HIGH or LOW State) (3-State)	0		V <sub>CC</sub>	V	
		0		5.5		
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			-24	mA	
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA	
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			-12	mA	
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			12	mA	
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V	

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -18mA	2.4		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 100μA		0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

**DC ELECTRICAL CHARACTERISTICS** (continued)

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
$I_I$	Input Leakage Current	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_I \leq 5.5\text{V}$		$\pm 5.0$	$\mu\text{A}$
$I_{OZ}$	3-State Output Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_O \leq 5.5\text{V}; V_I = V_{IH} \text{ or } V_{IL}$		$\pm 5.0$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$V_{CC} = 0\text{V}; V_I \text{ or } V_O = 5.5\text{V}$		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_I = \text{GND or } V_{CC}$		20	$\mu\text{A}$
		$2.7 \leq V_{CC} \leq 3.6\text{V}; 3.6 \leq V_I \text{ or } V_O \leq 5.5\text{V}$		$\pm 20$	$\mu\text{A}$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_{IH} = V_{CC} - 0.6\text{V}$		500	$\mu\text{A}$

**AC CHARACTERISTICS** (Note 3.;  $t_R = t_F = 2.5\text{ns}; C_L = 50\text{pF}; R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits				Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			$V_{CC} = 3.0\text{V to } 3.6\text{V}$		$V_{CC} = 2.7\text{V}$		
			Min	Max	Min	Max	
$f_{max}$	Maximum Clock Frequency	3	170				MHz
$t_{PHL}$ $t_{PLH}$	Propagation Delay Input to Output	1	1.5    6.0	1.5    6.0	1.5    7.0	1.5    7.0	ns
$t_{PHL}$ $t_{PLH}$	Propagation Delay Clock to Output	3	1.5    6.7	1.5    6.7	1.5    8.0	1.5    8.0	ns
$t_{PHL}$ $t_{PLH}$	Propagation Delay LE <sub>xx</sub> to Output	4	1.5    7.0	1.5    7.0	1.5    8.0	1.5    8.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time to High and Low Level	2	1.5    7.2	1.5    7.2	1.5    8.2	1.5    8.2	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time From High and Low Level	2	1.5    7.0	1.5    7.0	1.5    8.0	1.5    8.0	ns
$t_s$	Setup Time	3,4	2.5		2.5		ns
$t_h$	Hold Time	3,4	1.5		1.5		ns
$t_w$	Pulse Width Time	3,4	3.0		3.0		ns
$t_{OSHL}$ $t_{OSLH}$	Output-to-Output Skew (Note 4.)			1.0			ns

3. These AC parameters are preliminary and may be modified prior to release.

4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

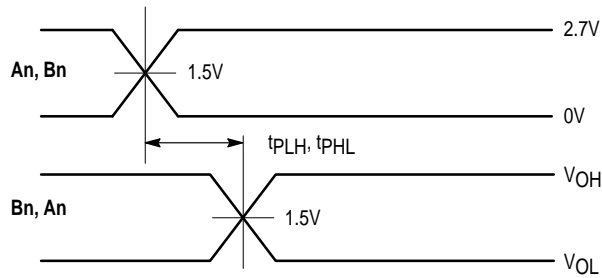
**DYNAMIC SWITCHING CHARACTERISTICS**

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 5.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 5.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V

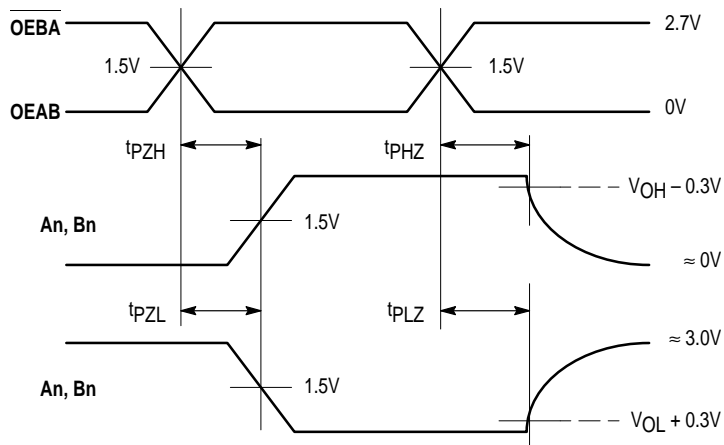
5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10MHz, V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	20	pF

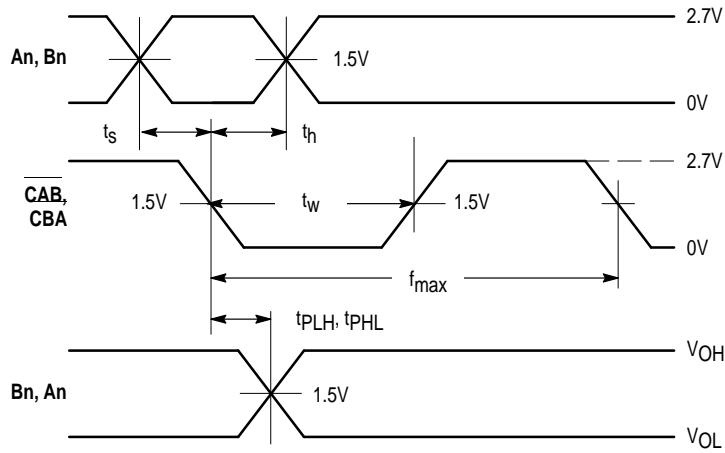


**WAVEFORM 1 – An to Bn PROPAGATION DELAYS**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



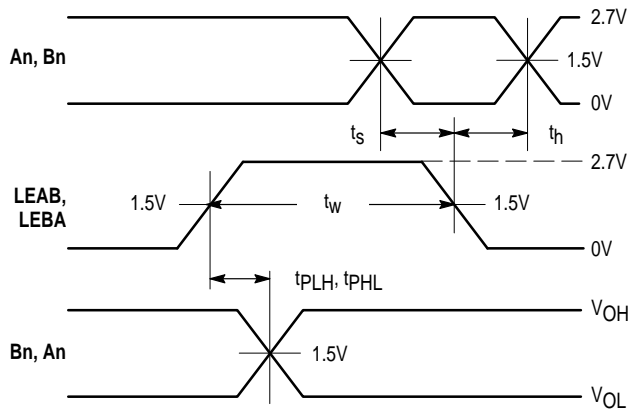
**WAVEFORM 2 – OEBA/OEAB to An/Bn OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 4. AC Waveforms**



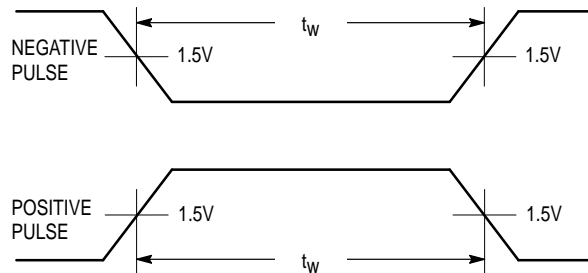
**WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES**

$t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$  except when noted



**WAVEFORM 4 – LExx to An, Bn PROPAGATION DELAYS, LExx MINIMUM PULSE WIDTH, An, Bn to LExx SETUP AND HOLD TIMES**

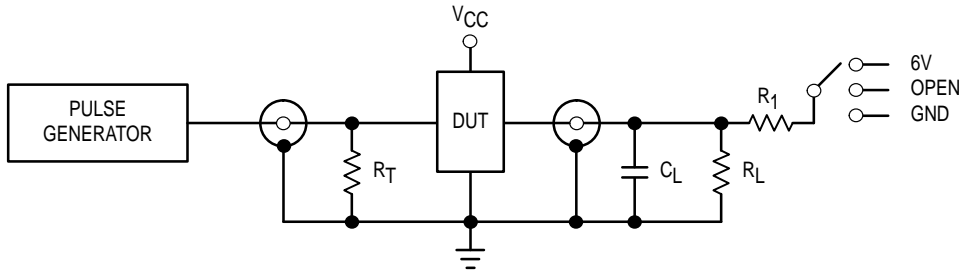
$t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$  except when noted



**WAVEFORM 5 – INPUT PULSE DEFINITION**

$t_R = t_F = 2.5\text{ns}$ , 10% to 90% of 0V to 2.7V

**Figure 5. AC Waveforms (continued)**



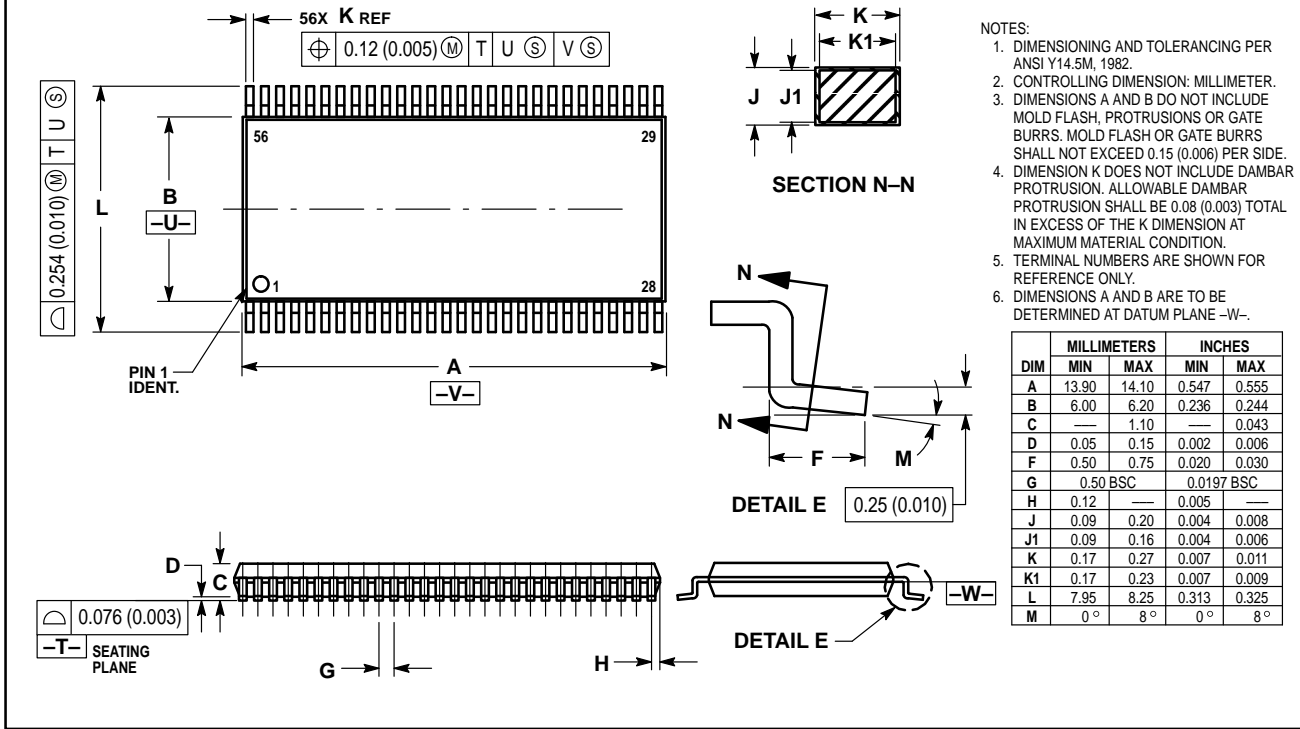
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 6. Test Circuit**

OUTLINE DIMENSIONS

DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 1202-01  
 ISSUE A



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