Advanced PWM and Dual Linear Power Control

Features

- 3 Regulated Voltage are provided
  - SYNC Switching Power for VTT(1.25V)
  - ASYNC Switching Power for NVVDD(2.05V)
  - Linear Regulator for FBVDDQ(2.5V)
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
  - VTT Output: ±1% Over Temperature
  - NVVDD Output: ±2% Over Temperature
  - FBVDDQ Output:±2.5% Over Temperature
- Fast Transient Response
  - On-Chip Feedback Compensation
  - Full 0% to 100% Duty Ratio
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
- Small Converter Size
  - Constant Frequency Operation(200kHz)
  - Programmable Oscillator from 50kHz to 800KHz
  - Reduce External Component Count

Applications

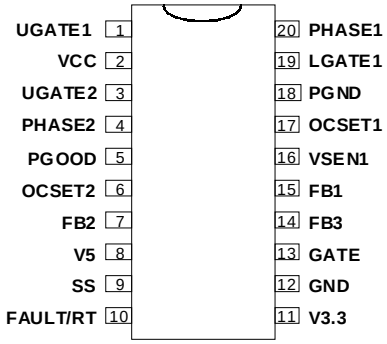
- VGA Card Power Regulation

General Description

The APW7026 Provides the power control and protection for three output voltages in VGA Card applications. It integrates two PWM controllers, one linear controller as well as the monitoring and protection functions into a single package. One PWM controller (PWM1) regulates the termination voltage VTT(1.25V) with a synchronous-rectified buck converter. The second PWM controller (PWM2) supplies the Core power NVVDD (2.05V) with a standard buck converter . The linear controller regulates 2.5V power for FBVDDQ.

The APW7026 can monitor all the output voltages (VTT ,NVVDD,FBVDDQ) and a single power good signal is issued when the VTT is within ± 10% of the reference voltage (V_{REF1}) and the other levels are above its lower power good threshold voltage. Additional built-in overvoltage protection (OVP) will be started when the VTT output is above 118% of the V_{REF1}.The OVP function will shutdown the upper MOSFET and turn on the lower MOSFET until the over-voltage is disappeared. The PWM controllers over-current function monitors the output current by sensing the voltage drop across the upper MOSFET $r_{DS(ON)}$, eliminating the need for a current sensing resistor.

Pin Description



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

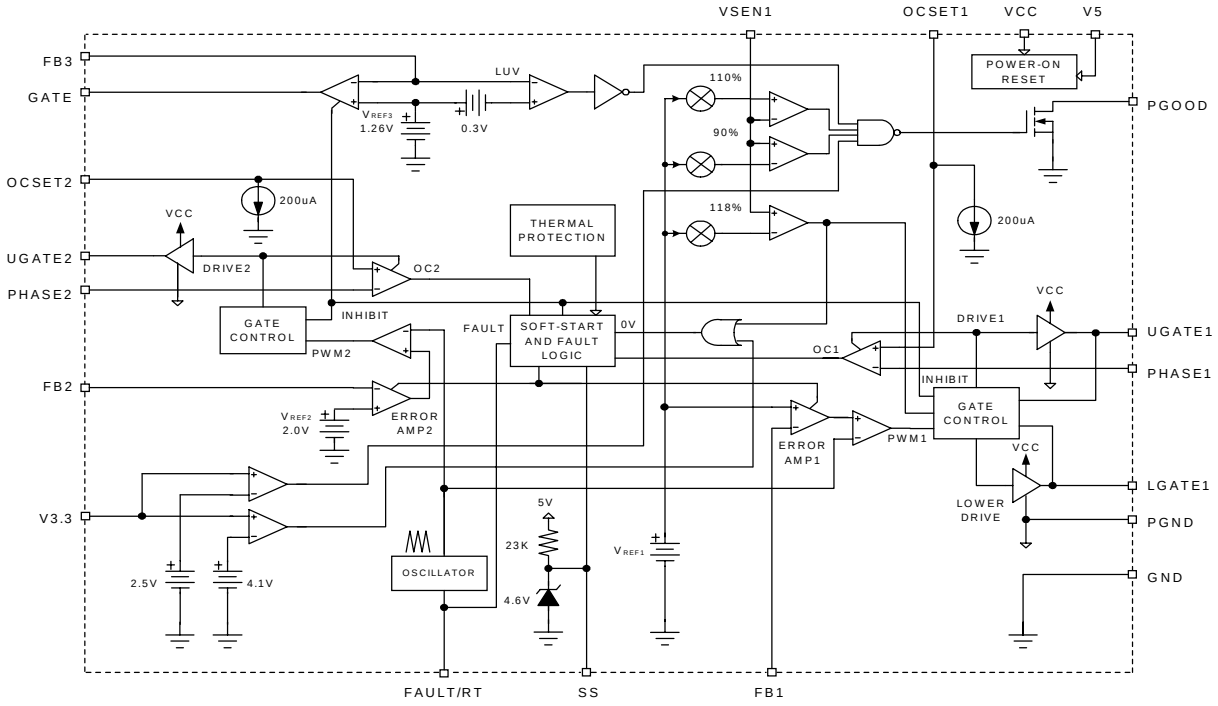
Ordering information

APW7026 □□ □□-□□□

- Lead Free Code
- Handling Code
- Temp. Range
- Package Code
- Voltage Code

Voltage Code
12 : 1.25V
Package Code
K : SOP - 20
Temp. Range
C : 0 to 70° C
Handling Code
TU : Tube TR : Tape & Reel
Lead Free Code
L : Lead Free Device Blank : Original Device

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCC	Supply Voltage	15	V
V_I , V_O	Input , Output or I/O Voltage	GND -0.3 V to VCC +0.3	V
T_A	Operating Ambient Temperature	Range 0 to 70	°C
T_J	Junction Temperature	Range 0 to 125	°C
T_{STG}	Storage Temperature	Range -65 to +150	°C
T_S	Soldering Temperature	300 ,10 seconds	°C

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Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{JA}	Thermal Resistance in Free Air SOIC SOIC (with 3in^2 of Copper)	75 65	°C

Electrical Characteristics

1. Recommended operating conditions, Unless otherwise noted.
2. Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7026			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{CC}	Nominal Supply Current	UGATE1, LGATE1, UGATE2, and GATE Open		6		mA
POWER-ON RESET						
	Rising VCC Threshold			9.5	10.4	V
	Falling VCC Threshold		8.2	9.0		V
	Rising V5 Threshold			4.4	4.7	V
	Falling V5 Threshold		3.7	4.0		V
OSCILLATOR						
F_{OSC}	Free Running Frequency	RT = Open	185	200	215	kHz
ΔV_{OSC}	Ramp Amplitude	RT = Open		1.9		V
PWM CONTROLLER REFERENCE VOLTAGE						
V_{REF1}	SYNC PWM Controller Reference Voltage			1.25		V
	V_{REF1} Accuracy		-1		+1	%
V_{REF2}	ASYNC PWM Controller Reference Voltage			2.0		V
	V_{REF2} Accuracy		-2		+2	%
LINEAR CONTROLLER						
V_{REF3}	Reference Voltage	GATE=FB3		1.26		V
	V_{REF3} Accuracy		-2.5		+2.5	%
	GATE Drive Current	V_{GATE}=4V	20	50		mA
PWM CONTROLLERS GATE DRIVERS						
I_{UGATE}	UGATE1,2 Source	VCC = 12V, V_{UGATE1} (or V_{UGATE2}) = 6V		1.0		A
R_{UGATE}	UGATE1,2 Sink	VCC = 12V, V_{UGATE1} (or V_{UGATE2}) = 1V		2.2	3.5	Ω
I_{LGATE}	LGATE1 Source	VCC = 12V, V_{LGATE1} = 1V		1.0		A
R_{LGATE}	LGATE1 Sink	VCC = 12V, V_{LGATE1} = 1V		1.6	3.0	Ω

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Electrical Characteristics Cont.

1. Recommended operating conditions, Unless otherwise noted.
2. Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7026			Unit
			Min	Typ	Max	
PROTECTION						
	VSEN1 O.V. trip point (VSEN1/V_{REF1})	VSEN 1 Rising		118		%
	VSEN1 O.V. Hysteresis			2		%
	V3.3 O.V. trip point	V3.3 Rising		4.1		V
	V3.3 O.V. Hysteresis			0.1		V
I_{OVP}	FAULT Souring Current	$V_{FAULT/RT}$ = 2.0V		25		mA
	OCSET 1,2 Current Source	Vocset= 4.5V	170	200	230	uA
R_{SS}	Pull up resistor to 5V			23		KΩ
POWER GOOD						
	VSEN1 Upper Threshold (VSEN 1/V_{REF1})	VSEN1 Rising		110		%
	VSEN 1 Lower Threshold	VSEN1 Rising		94		%
	VSEN1 PGD Hysteresis	Upper/Lower Threshold		2		%
	V3.3 Lower Threshold	V3.3 Rising		2.5		V
	V3.3 PGD Hysteresis			0.1		V
	FB3 Lower Threshold	V_{FB3} Rising		1.0		V
	FB3 PGD Hysteresis			0.1		V
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -4mA			0.8	V

Functional Pin Description

UGATE1 (Pin 1)

Connect UGATE1 pin to the SYNC PWM Converter's upper MOSFET gate .This pin provides the gate drive for the upper MOSFET.

VCC (Pin 2)

Provide a + 12V bias supply for the IC to this pin . This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purpose.

UGATE2 (Pin 3)

Connect UGATE2 pin to the ASYNC PWM converter's MOSFET gate . This pin provides the gate drive for the MOSFET.

PHASE2 (Pin 4)

Connect the PHASE2 pin to the ASYNC PWM converter's MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection.

PGOOD (Pin 5)

PGOOD is an open drain output used to indicate the status of the output voltages. This pin is pulled low when the SYNC PWM regulator output is not within ± 10% of the reference voltage (V_{REF1}) or when V3.3 or V_{FB3} is below its lower power good threshold.

OCSET2 (Pin 6)

Connect a resistor (R_{OCSET}) from this pin to the drain of the ASYNC PWM converter's MOSFET . R_{OCSET}, an internal 200μA current source (I_{OCSET}) , and the MOSFET's on-resistance ($r_{DS(ON)}$) set the converter's over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

FB2 (Pin 7)

Connect this pin to the output of the ASYNC PWM converter . The voltage at this pin is regulated to the reference voltage V_{REF2}. A resistor driver is connected from this pin to V_{OUT2}(R_{OUT2}) and to GND(R_{GND2}) that sets the output voltage as the following equation :

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Functional Pin Description Cont.

$$V_{OUT2} = \left(1+\frac{R_{OUT2}}{R_{GND2}}\right) \times V_{REF2}$$

The value of the resistor connected from V_{OUT2} to FB2 must be less than 150Ω .

V5 (Pin 8)

The +5V input voltage at this pin is monitored for power-on reset (POR) purpose.

SS (Pin 9)

This pin provides the soft-start for the all PWM converters and linear regulator . An internal resistor charges an external capacitor that is connected from 5V supply to this pin which ramps up the all outputs , preventing the outputs from overshooting as well as limiting the input current . The second function of the soft-start cap is to provides long off time for the synchronous MOSFET during current limiting .

FAULT / RT (Pin 10)

This pin provides oscillator switching frequency adjustment . By placing a resistor (R_T) from this pin to GND , the nominal 200kHz switching frequency is increased .Conversely, connecting a pull-up resistor (R_T) from this pin to VCC reduces the switching frequency. Nominally , the voltage at this pin is 1.26V. In the event of an over-voltage or over-current condition , this pin is internally pulled to VCC.

V3.3 (Pin 11)

This pin is connected to the +3.3V or the output of the ASYNC PWM converter for power good and over-voltage detection. When the output voltage of the ASYNC PWM converter is not in the range from 3V to 4V, connect this pin to +3.3V voltage.

GND (Pin 12)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

GATE (Pin 13)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the linear regulator's pass MOSFET.

FB3 (Pin 14)

Connect this pin to the output of the linear regulator . A resistor driver is connected from this pin to V_{OUT3} and GND that sets the output voltage as same as V_{OUT2}. This pin is monitored for power good function.

FB1 (Pin 15)

This pin provides the feedback for the SYNC PWM converter. Typically this pin can be connected directly to the output of the converter . However , a resistor divider is recommended to be connected from this pin to V_{OUT1} and GND to adjust the output voltage as same as V_{OUT2}. The value of the resistor connected from V_{OUT1} to FB1 must be less than 200Ω.

VSEN1 (Pin 16)

This pin is connected to the SYNC PWM converter's output voltage . The PGOOD and OVP comparator cicuits use this signal to report output voltage status and over-voltage protection.

OCSET1 (Pin 17)

Connect a resistor (R_{OCSET}) from this pin to the drain of the SYNC PWM converter's upper MOSFET . The over-current (OC) trip point for the SYNC PWM converter is set by the R_{OCSET} as same as the OCSET2. An over-current trip cycles the soft-start function.

PGND (Pin 18)

This is the power ground connection . Tie the SYNC PWM converter's lower MOSFET source to this pin.

LGATE1 (Pin 19)

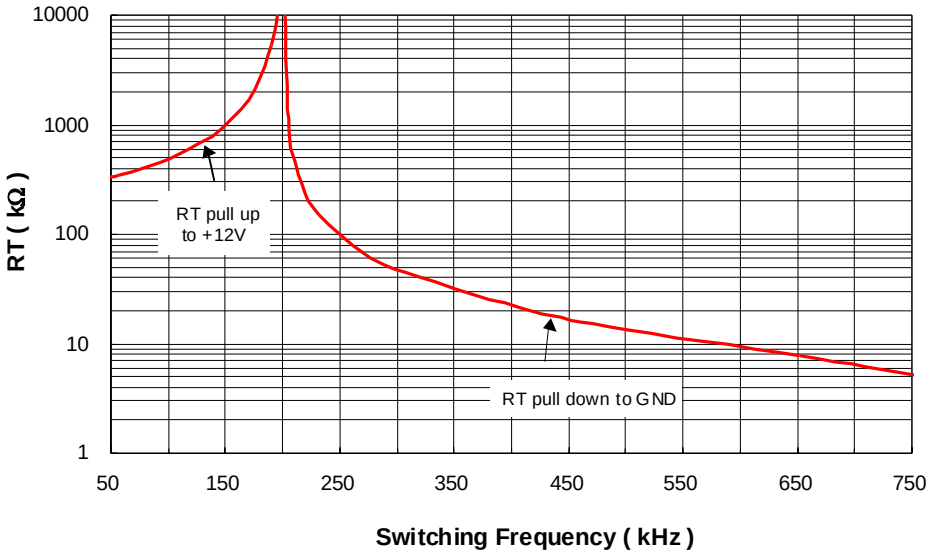
Connect LGATE1 to the SYNC PWM converter's lower MOSFET gate . This pin provides the gate drive for the lower MOSFET.

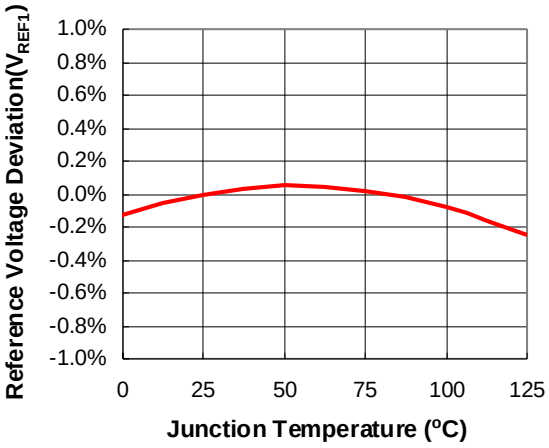
PHASE1 (Pin 20)

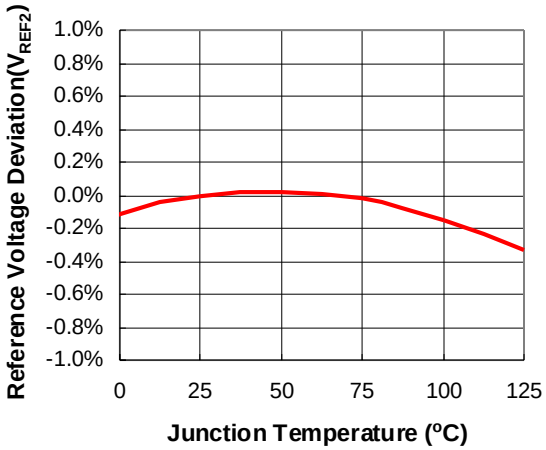
Connect the PHASE1 pin to the SYNC PWM Converter's upper MOSFET source. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection.

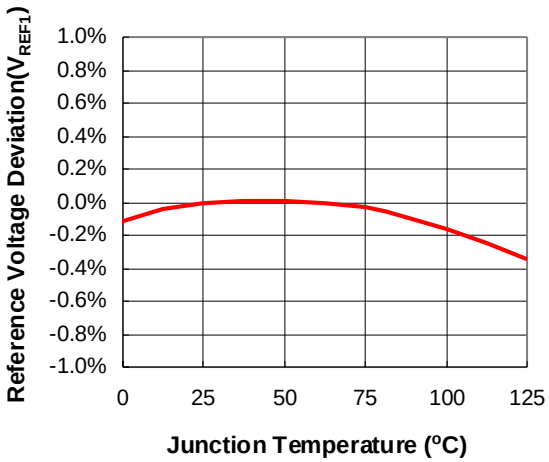
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Typical Performance Curves









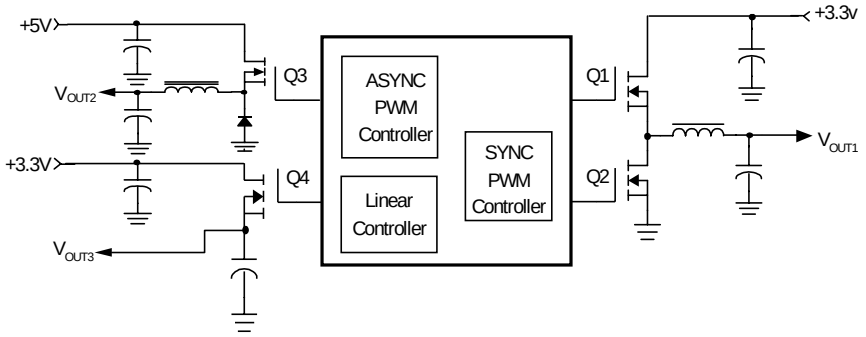
Note : The Referance Voltage(V_{REF}) Deviation is

$$\frac{V_{REF}(T_J) - V_{REF}(25^oC)}{V_{REF}(25^oC)} \times 100\%$$

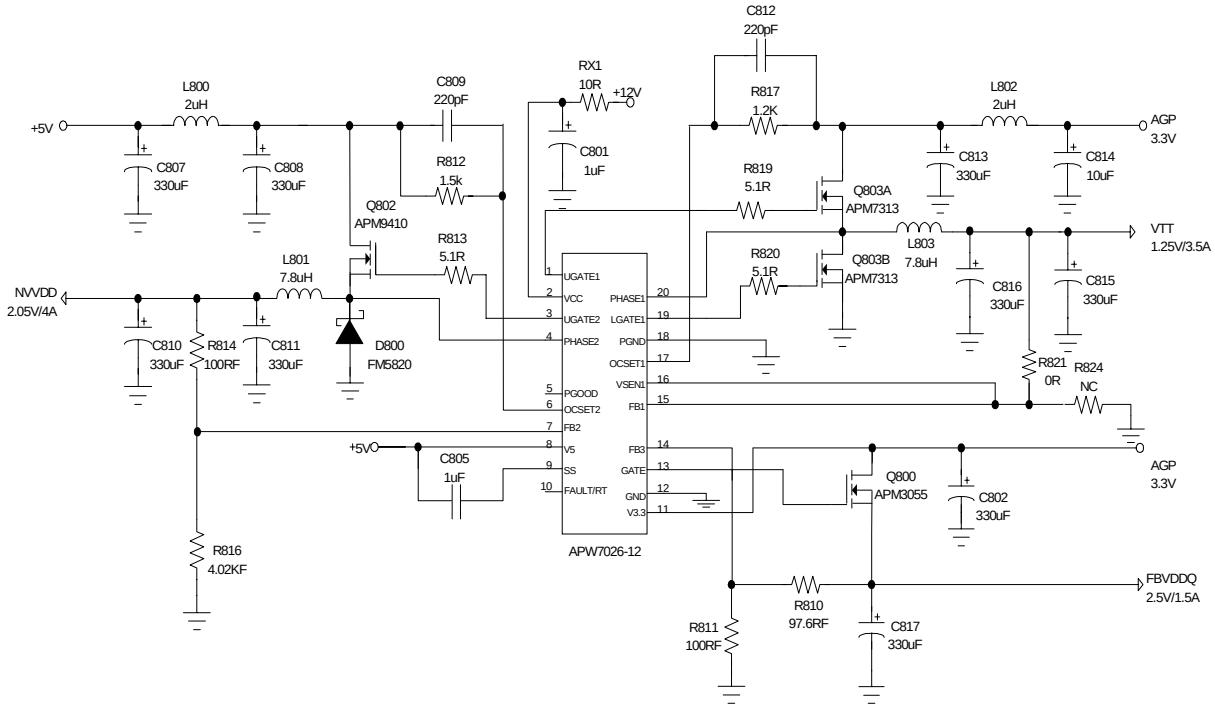
T_J is Junction Temperature.

rt

Simplified Power System Diagram

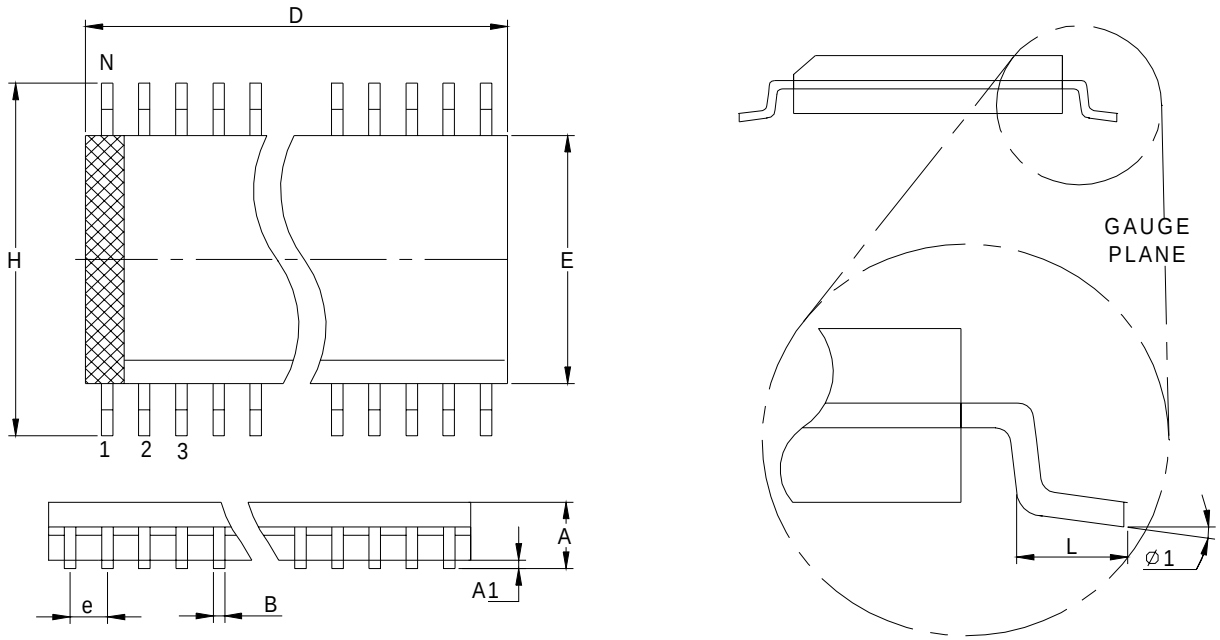


Typical Application Circuit



Packaging Information

SO – 300mil (Reference JEDEC Registration MS-013)



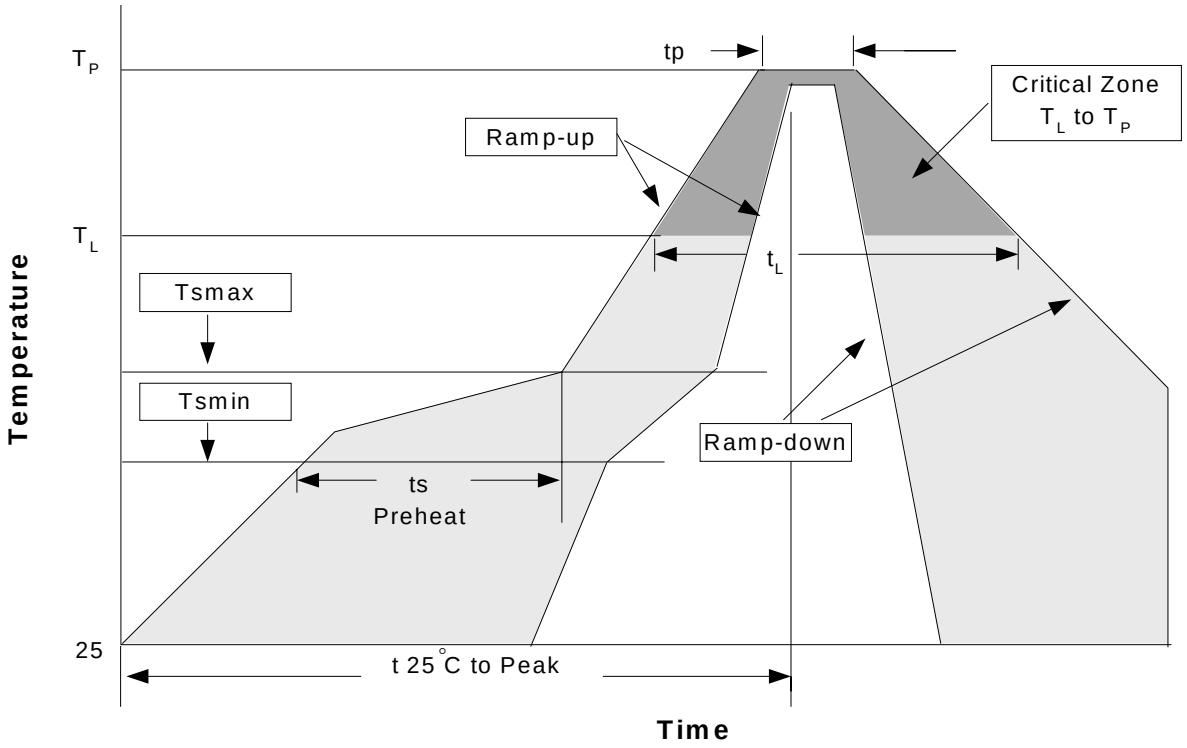
Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

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Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat - Temperature Min (Tsmin) - Temperature Mix (Tsmax) - Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L - Ramp-up Rate			3°C/second max	
Tsmax to T_L - Temperature(T_L) - Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(Tp)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature(tp)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

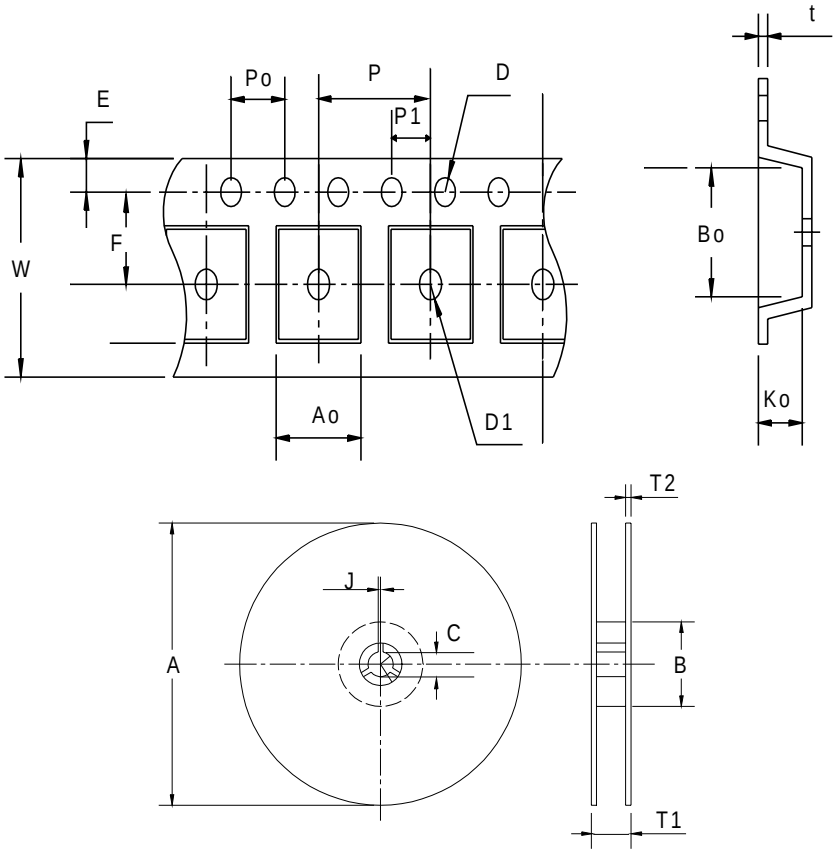
Note: All temperatures refer to topside of the package. Measured on the body surface.

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Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP- 28	330±1	62 ±1.5	12.75 ± 0. 5	2 ± 0.6	24.4 ± 0.2	2± 0.2	24 ± 0.3	12 ± 0.1	1.75± 0.1
Application	F	D	D1	Po	P1	Ao	Bo	Ko	t
SOP- 28	11.5 ± 0.1	1.5 +0.1	1.5+ 0.25	4.0 ± 0.1	2.0 ± 0.1	10.85 ± 0.1	18.34± 0.1	2.97± 0.1	0.35±0.01

(mm)

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Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 28	24	21.3	1000

Customer Service

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