KMB6D0NP40QA

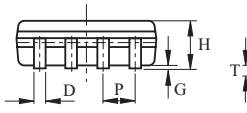
N and P-Ch Trench MOSFET

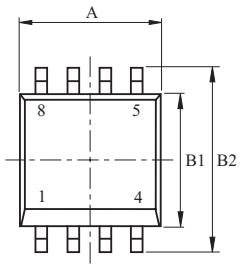
General Description

This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for Back-light Inverter.

FEATURES

· N-Channel
: V_{DSS}=40V, I_D=6A.
: $R_{DS(ON)}$=31mΩ (Max.) @ V_{GS}=10V
: $R_{DS(ON)}$=45mΩ (Max.) @ V_{GS}=4.5V
· P-Channel
: V_{DSS}=-40V, I_D=-5A.
: $R_{DS(ON)}$=45mΩ (Max.) @ V_{GS}=-10V
: $R_{DS(ON)}$=63mΩ (Max.) @ V_{GS}=-4.5V
· Super High Dense Cell Design.





DIM	MILLIMETERS
A	4.85±0.2
B1	3.94±0.2
B2	6.02±0.3
D	0.4±0.1
G	0.15+0.1/-0.05
H	1.63±0.2
L	0.65±0.2
P	1.27
T	0.20+0.1/-0.05

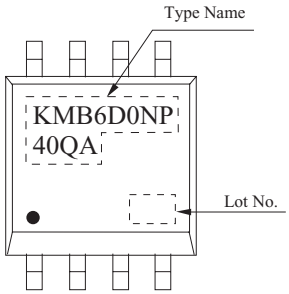
FLP-8

MAXIMUM RATING (Ta=25℃)

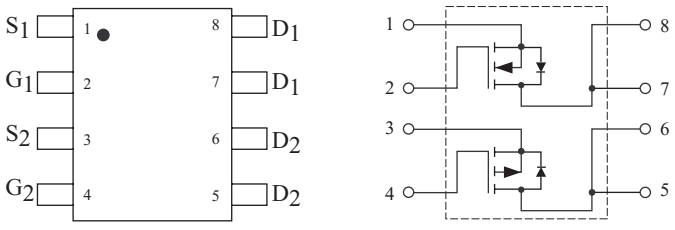
CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	40	-40	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current	DC	I_D*	6	-5	A
	Pulsed	I_{DP}*	20	-20	
Source-Drain Diode Current		I_S*	3.0	-3.2	A
Drain Power Dissipation	T_A=25℃	P_D*	2	2	W
	T_A=70℃		1.3	1.3	
Maximum Junction Temperature		T_j	150		℃
Storage Temperature Range		T_{stg}	-55～150		℃
Thermal Resistance, Junction to Ambient		R_{thJA}*	62.5		℃/W

* : Surface Mounted on FR4 Board.

Marking



PIN CONNECTION (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250㎂, V_{GS}=0V	N-Ch	40	-	-	V
		I_D=-250㎂, V_{GS}=0V	P-Ch	-40	-	-	
Drain Cut-off Current	I_{DSS}	V_{DS}=32V, V_{GS}=0V	N-Ch	-	-	1	㎂
		V_{DS}=-32V, V_{GS}=0V	P-Ch	-	-	-1	
Gate Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	N-Ch	-	-	±100	nA
			P-Ch	-	-	±100	
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250㎂	N-Ch	1.0	2.3	3.0	V
		V_{DS}=V_{GS}, I_D=-250㎂	P-Ch	-1.0	-2.0	-3.0	
Drain-Source ON Resistance	$R_{DS(ON)}$*	V_{GS}=10V, I_D=6A	N-Ch	-	19.6	31.0	mΩ
		V_{GS}=-10V, I_D=-5A	P-Ch	-	31.2	45.0	
		V_{GS}=4.5V, I_D=5A	N-Ch	-	39.9	45.0	
		V_{GS}=-4.5V, I_D=-2A	P-Ch	-	47.6	63.0	
Forward Transconductance	g_{fs}*	V_{DS}=5V, I_D=6A	N-Ch	-	2.2	-	S
		V_{DS}=-5V, I_D=-4A	P-Ch	-	9.5	-	
Dynamic							
Input Capacitance	C_{iss}	**N-Ch** : V_{DS}=20V, V_{GS}=0V, f=1MHz **P-Ch** : V_{DS}=-20V, V_{GS}=0V, f=1MHz	N-Ch	-	420	-	pF
			P-Ch	-	850	-	
Output Capacitance	C_{oss}		N-Ch	-	160	-	
			P-Ch	-	220	-	
Reverse transfer Capacitance	C_{rss}		N-Ch	-	40	-	
			P-Ch	-	82	-	
Total Gate Charge	Q_g*	**N-Ch** : V_{DS}=20V, I_D=6A, V_{GS}=10V **P-Ch** : V_{DS}=-20V, I_D=-5A, V_{GS}=-10V	N-Ch	-	12.0	-	nC
			P-Ch	-	15.0	-	
Gate-Source Charge	Q_{gs}*	**N-Ch** : V_{DS}=20V, I_D=6A, V_{GS}=10V **P-Ch** : V_{DS}=-20V, I_D=-5A, V_{GS}=-4.5V	N-Ch	-	1.6	-	
			P-Ch	-	2.0	-	
Gate-Drain Charge	Q_{gd}*		N-Ch	-	2.6	-	
			P-Ch	-	6.5	-	
Turn-on Delay time	$t_{d(on)}$*	**N-Ch** : V_{DD}=20V, I_D=6A, V_{GS}=10V, R_G=3Ω **P-Ch** : V_{DD}=-20V, V_{GS}=-10V, R_G=3Ω, I_D=-5A	N-Ch	-	9.0	-	ns
			P-Ch	-	17.0	-	
Turn-on Rise time	t_r*		N-Ch	-	8.9	-	
			P-Ch	-	13.2	-	
Turn-off Delay time	$t_{d(off)}$*		N-Ch	-	23.6	-	
			P-Ch	-	38.0	-	
Turn-off Fall time	t_f*		N-Ch	-	3.4	-	
			P-Ch	-	15.0	-	
Source-Drain Diode Ratings							
Source-Drain Diode Forward Voltage	V_{SDF}*	I_S=1.0A, V_{GS}=0V	N-Ch	-	0.71	1.2	V
		I_S=-1.0A, V_{GS}=0V	P-Ch	-	-0.71	-1.2	
Note>* Pulse Test : Pulse width <300㎲ , Duty cycle < 2%							

N-Channel

Fig1. I_D - V_{DS}

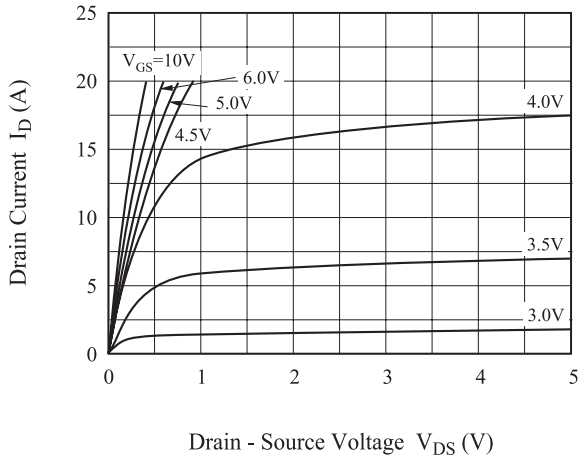


Fig2. $R_{DS(ON)}$-I_D

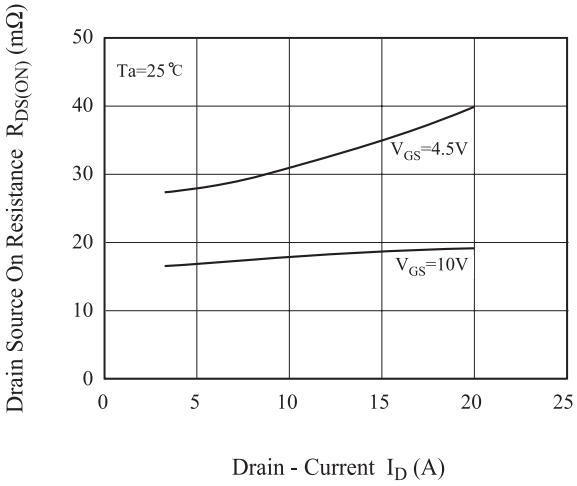


Fig3. I_D - V_{GS}

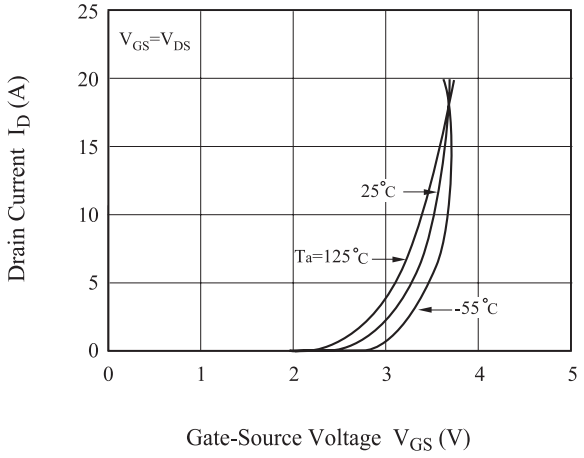


Fig4. $R_{DS(on)}$ - T_j

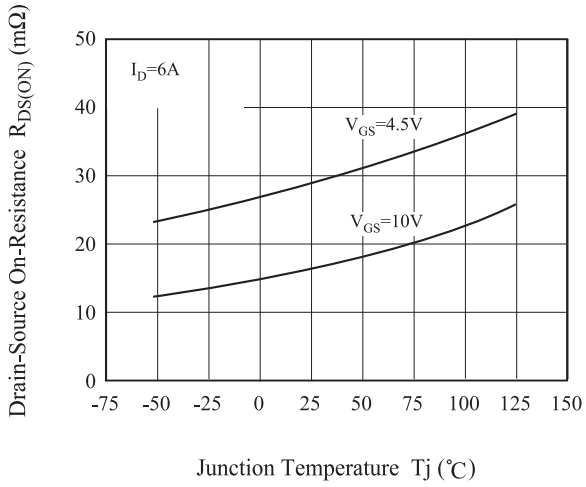


Fig5. V_{th} - T_j

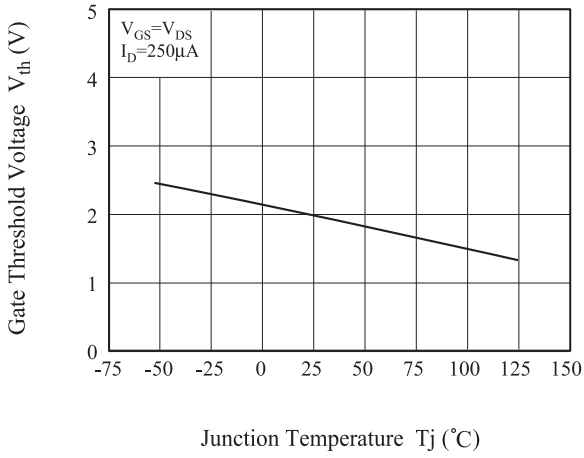


Fig6. I_S - V_{SDF}

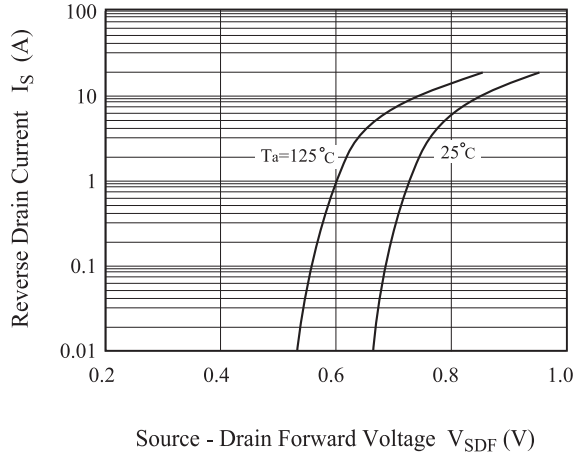


Fig 7. V_{GS} - Q_g

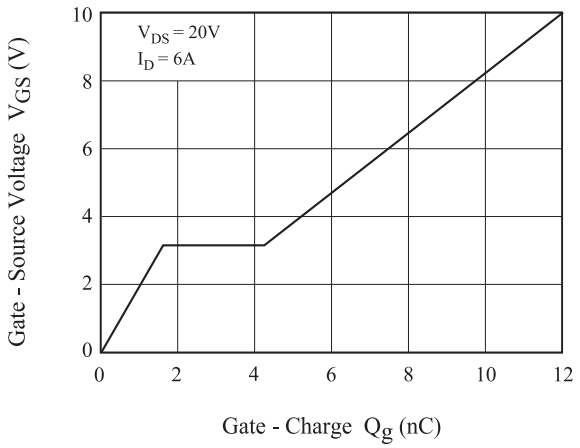


Fig 8. C - V_{DS}

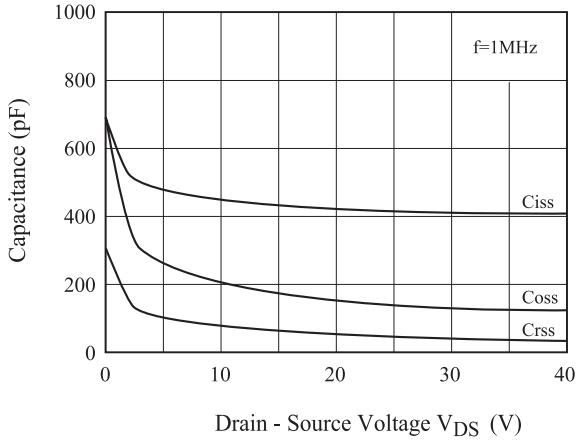


Fig9. Safe Operation Area

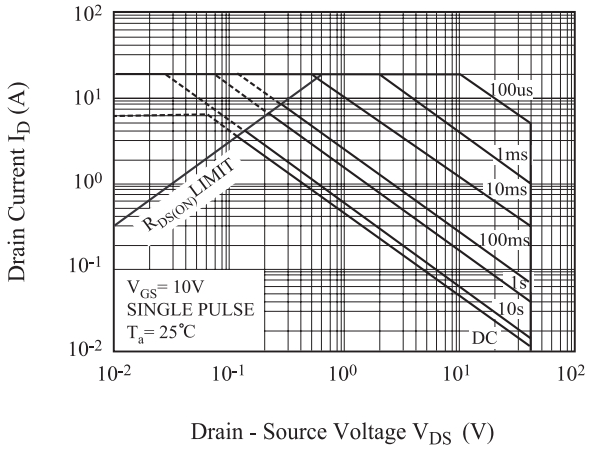


Fig10. Transient Thermal Response Curve

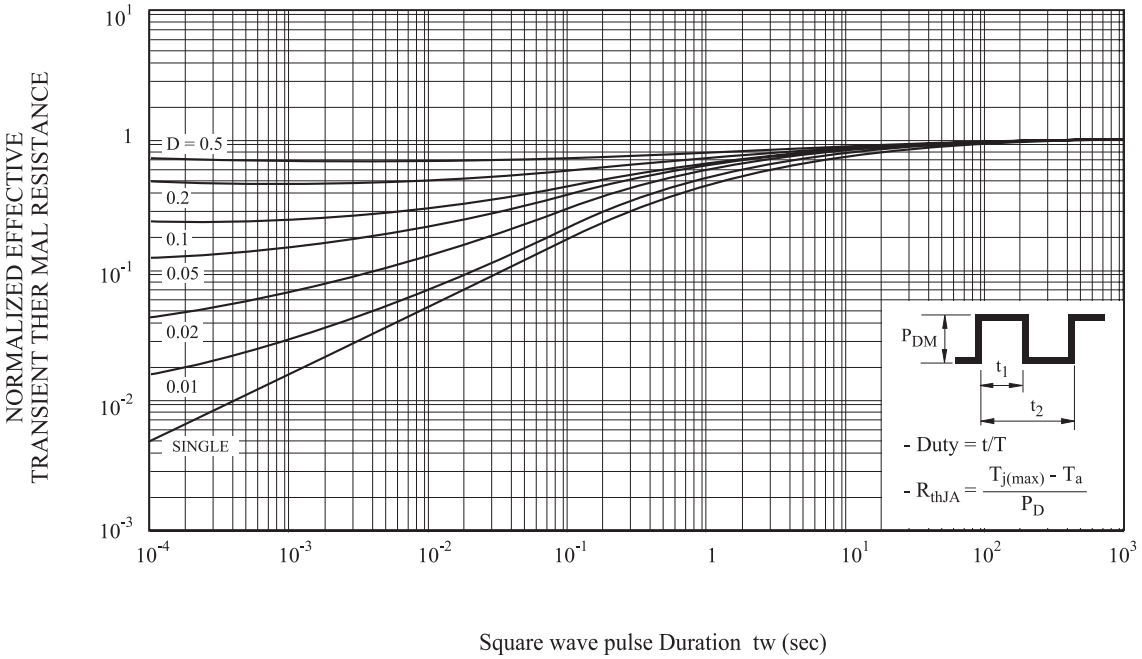


Fig11. Gate Charge Circuit and Wave Form

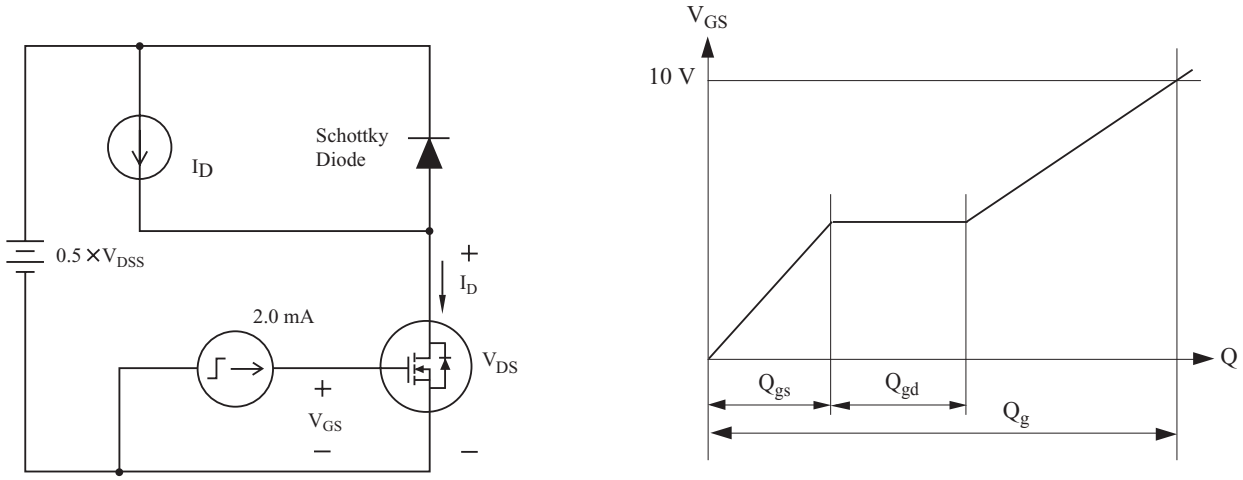
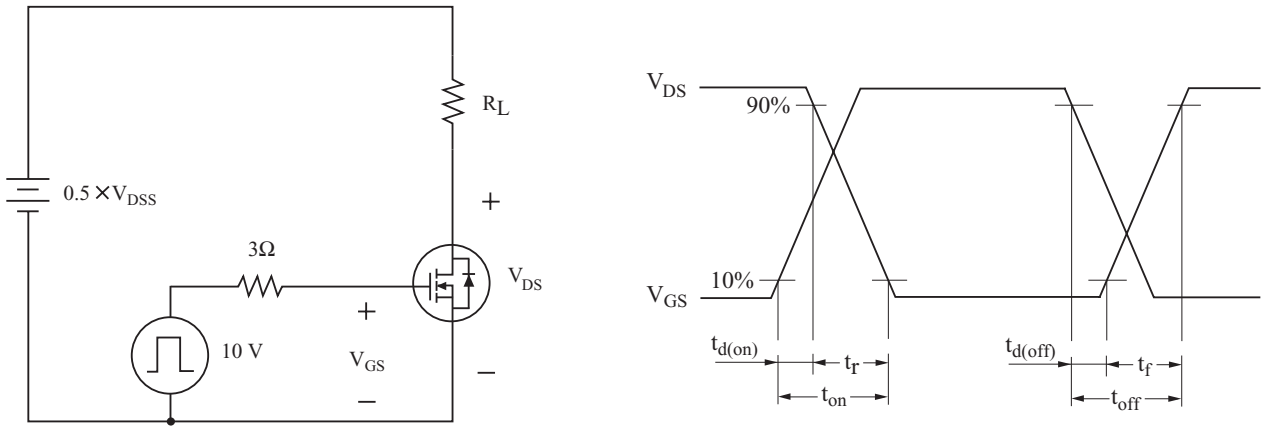


Fig12. Resistive Load Switching



P-Channel

Fig1. I_D - V_{DS}

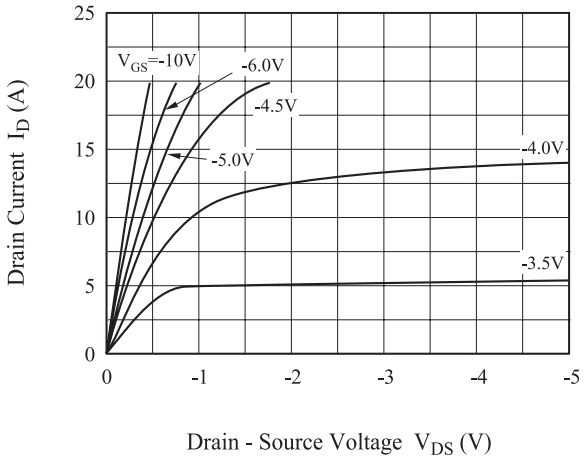


Fig2. $R_{DS(ON)}$-I_D

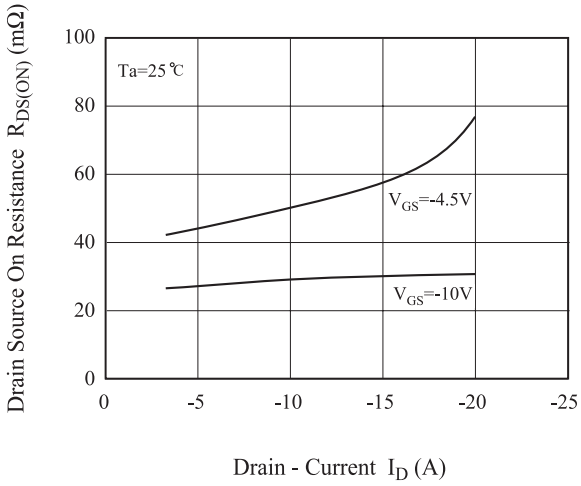


Fig3. I_D - V_{GS}

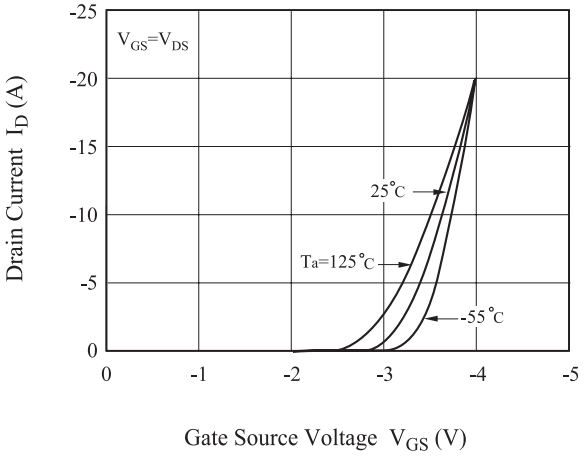


Fig4. $R_{DS(on)}$ - T_j

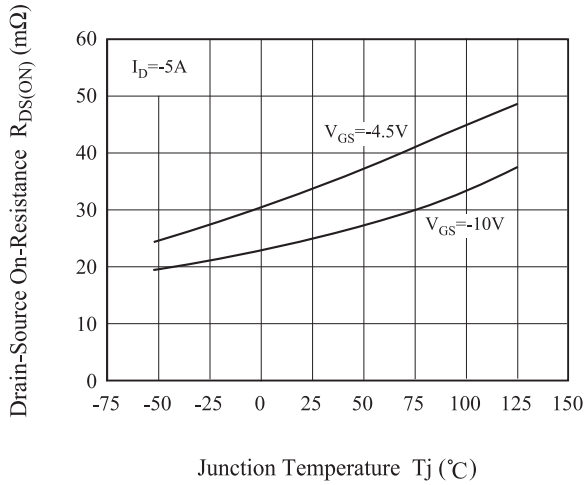


Fig5. V_{th} - T_j

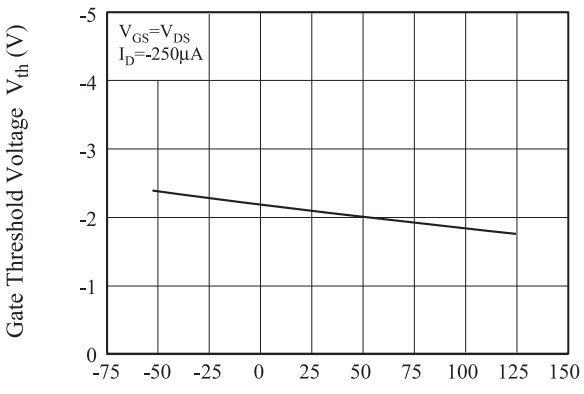


Fig6. I_S - V_{SDF}

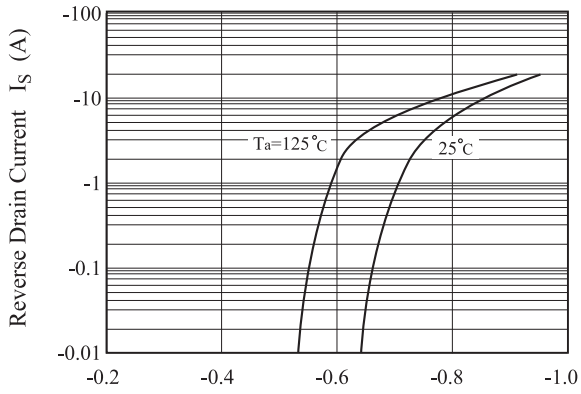


Fig 7. V_{GS} - Q_g

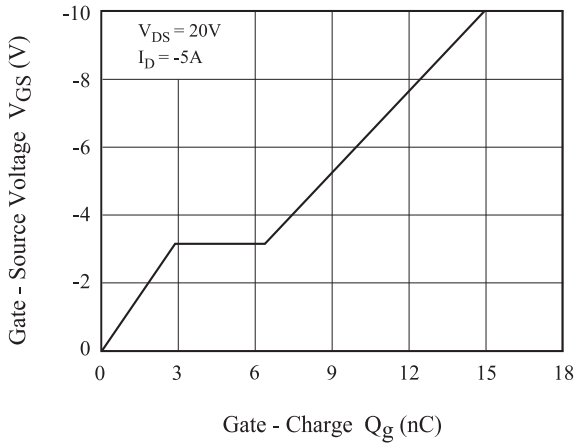


Fig 8. C - V_{DS}

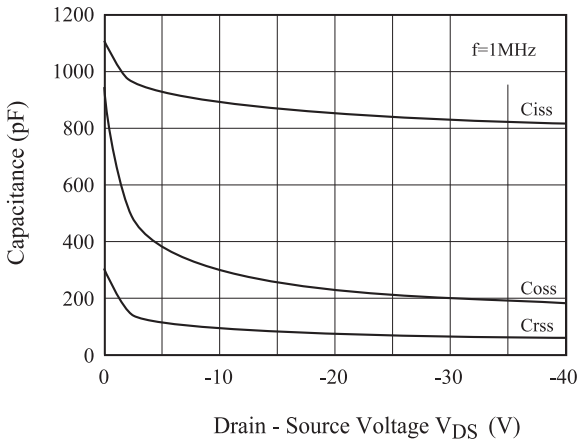


Fig9. Safe Operation Area

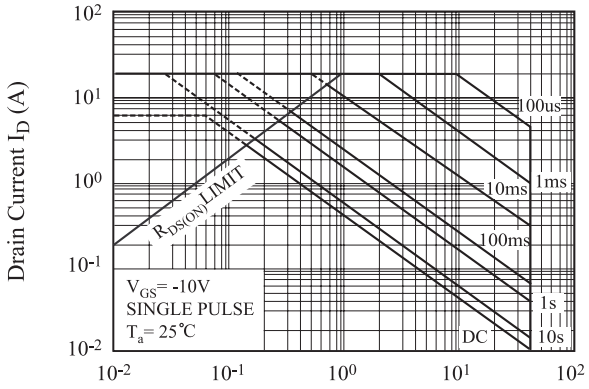


Fig10. Transient Thermal Response Curve

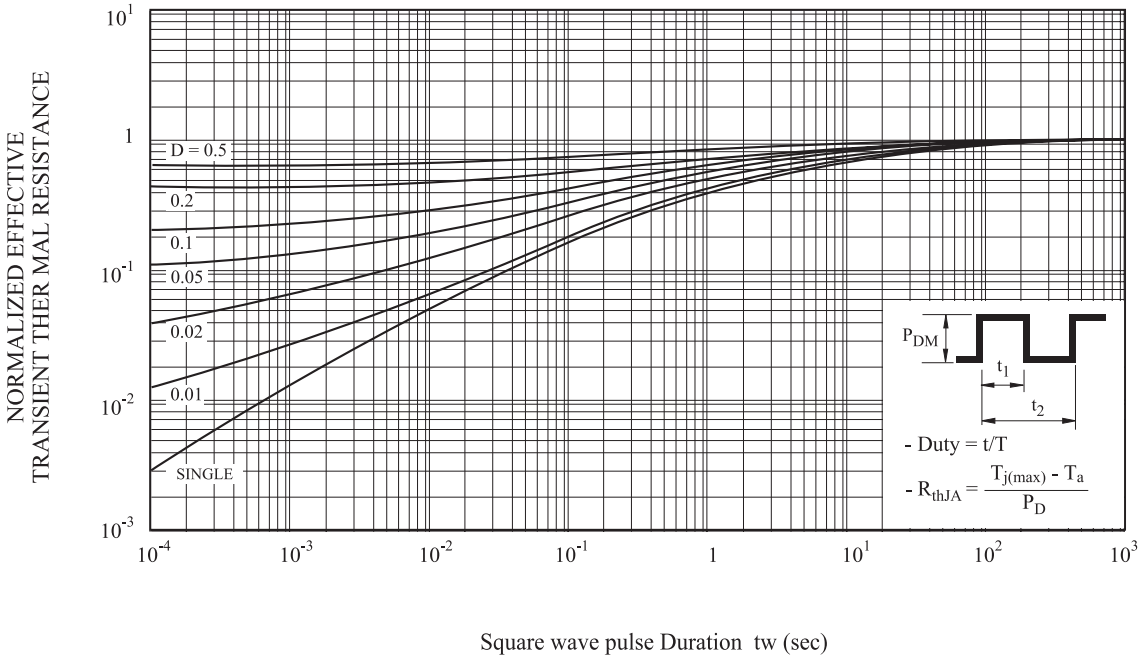


Fig. 11 Gate Charge

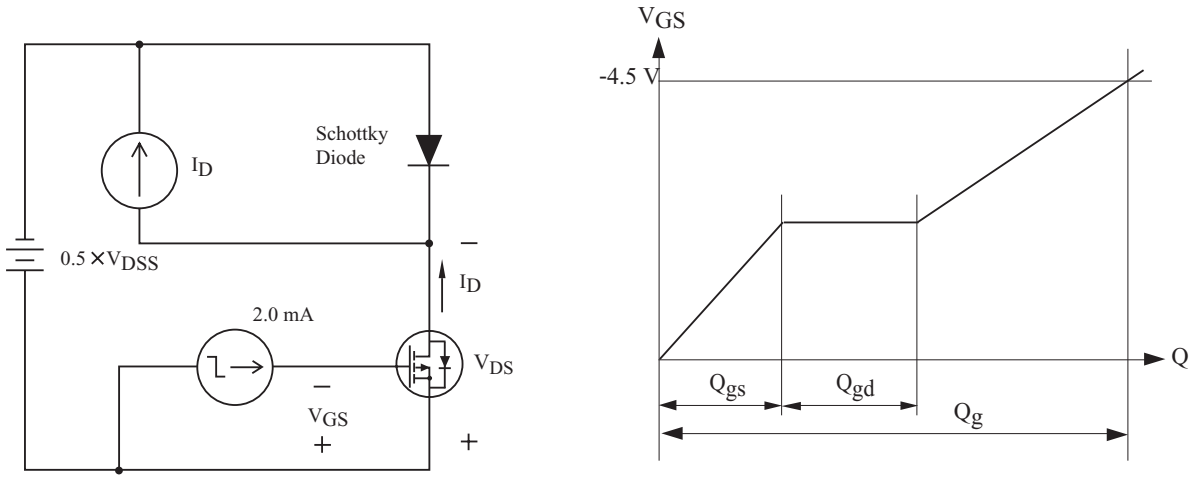


Fig. 12 Resistive Load Switching

