# WST8205

**Dual N-Ch MOSFET**

## General Description

The WST8205 is the highest performance trench N-ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST8205 meet the RoHS and Green Product requirement with full function reliability approved.

## Product Summery

| BVDSS | RDSON | ID |
|---|---|---|
| 20V | 24mΩ | 5.8A |

## Applications

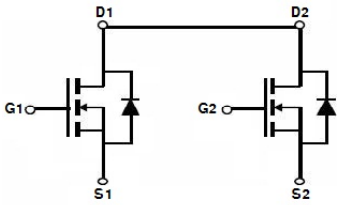
- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

## SOT-23-6L Pin Configuration






## Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 20 | V |
| $V_{GS}$ | Gate-Source Voltage | ±12 | V |
| $I_D$@$T_c$=25℃ | Continuous Drain Current, $V_{GS}$ @ 4.5V[1] | 5.8 | A |
| $I_D$@$T_c$=70℃ | Continuous Drain Current, $V_{GS}$ @ 4.5V[1] | 3.8 | A |
| $I_{DM}$ | Pulsed Drain Current[2] | 16 | A |
| $P_D$@$T_A$=25℃ | Total Power Dissipation[3] | 2.1 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |

## Thermal Data

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance Junction-ambient [1] | --- | 125 | ℃/W |
| $R_{\theta JC}$ | Thermal Resistance Junction-Case[1] | --- | 70 | ℃/W |

## Electrical Characteristics ($T_J$=25 ℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 20 | --- | --- | V |
| $\triangle BV_{DSS}/\triangle T_J$ | BVDSS Temperature Coefficient | Reference to 25℃ , $I_D$=1mA | --- | 0.022 | --- | V/℃ |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=4.5V , $I_D$=5.5A | --- | 24 | 28 | mΩ |
| | | $V_{GS}$=2.5V , $I_D$=3.5A | --- | 30 | 45 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$=$V_{DS}$ , $I_D$ =250uA | 0.5 | 0.7 | 1.2 | V |
| $\triangle V_{GS(th)}$ | $V_{GS(th)}$ Temperature Coefficient | | --- | -2.33 | --- | mV/℃ |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=16V , $V_{GS}$=0V , $T_J$=25℃ | --- | --- | 1 | uA |
| | | $V_{DS}$=16V , $V_{GS}$=0V , $T_J$=55℃ | --- | --- | 5 | |
| $I_{GSS}$ | Gate-Source Leakage Current | $V_{GS}$=±12V , $V_{DS}$=0V | --- | --- | ±100 | nA |
| gfs | Forward Transconductance | $V_{DS}$=5V , $I_D$=5A | --- | 25 | --- | S |
| $R_g$ | Gate Resistance | $V_{DS}$=0V , $V_{GS}$=0V , f=1MHz | --- | 1.5 | 3 | Ω |
| $Q_g$ | Total Gate Charge (4.5V) | $V_{DS}$=10V , $V_{GS}$=4.5V , $I_D$=5.5A | --- | 8.3 | 11.9 | nC |
| $Q_{gs}$ | Gate-Source Charge | | --- | 1.4 | 2.0 | |
| $Q_{gd}$ | Gate-Drain Charge | | --- | 2.2 | 3.2 | |
| $T_{d(on)}$ | Turn-On Delay Time | $V_{DD}$=10V , $V_{GEN}$=4.5V , RG=6Ω $I_D$=5A, RL=10Ω | --- | 5.7 | 11.6 | ns |
| $T_r$ | Rise Time | | --- | 34 | 63 | |
| $T_{d(off)}$ | Turn-Off Delay Time | | --- | 22 | 46 | |
| $T_f$ | Fall Time | | --- | 9.0 | 18.4 | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=10V , $V_{GS}$=0V , f=1MHz | --- | 625 | --- | pF |
| $C_{oss}$ | Output Capacitance | | --- | 69 | --- | |
| $C_{rss}$ | Reverse Transfer Capacitance | | --- | 61 | --- | |

## Diode Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current[1,4] | $V_G$=$V_D$=0V , Force Current | --- | --- | 1.5 | A |
| $I_{SM}$ | Pulsed Source Current[2,4] | | --- | --- | 16 | A |
| $V_{SD}$ | Diode Forward Voltage[2] | $V_{GS}$=0V , $I_S$=1A , $T_J$=25℃ | --- | --- | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | IF=5A , dI/dt=100A/μs , $T_J$=25℃ | --- | 7.1 | --- | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | --- | 1.8 | --- | nC |

Note :
1.The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

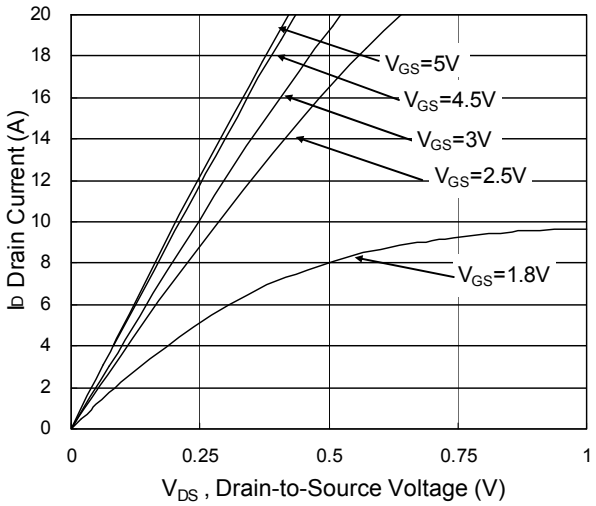



Fig.1 Typical Output Characteristics

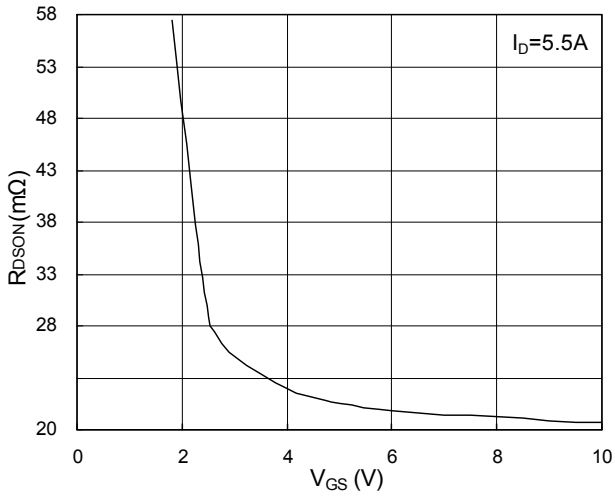



Fig.2 On-Resistance vs. Gate-Source

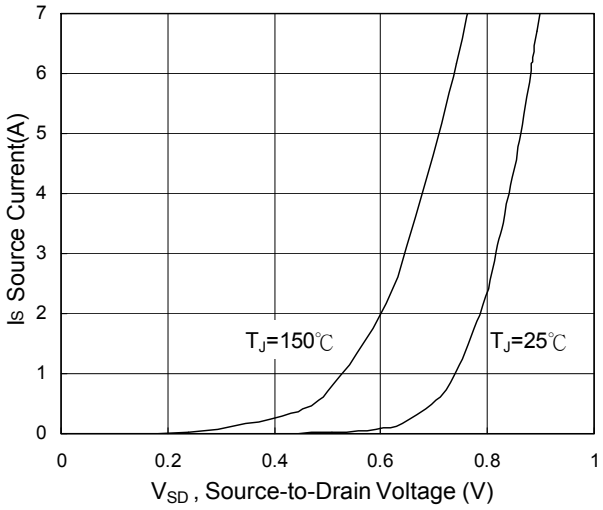



Fig.3 Forward Characteristics Of Reverse

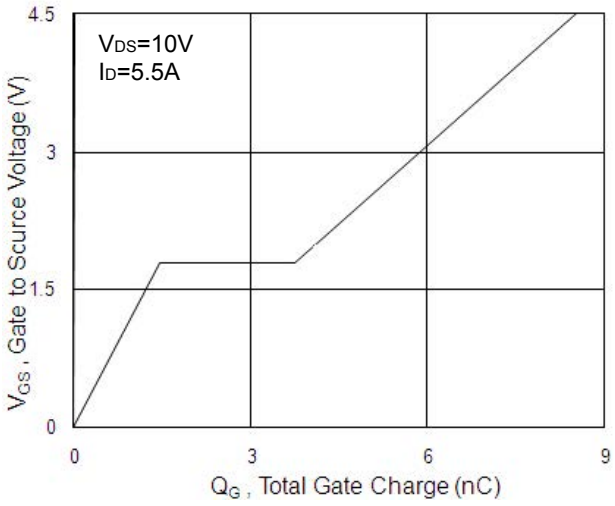



Fig.4 Gate-Charge Characteristics

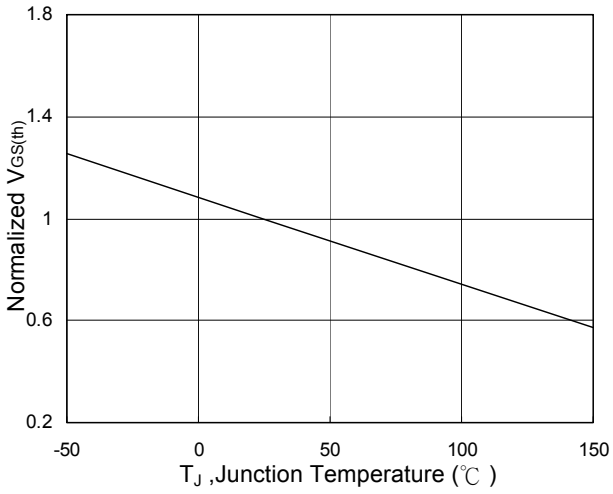



Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$

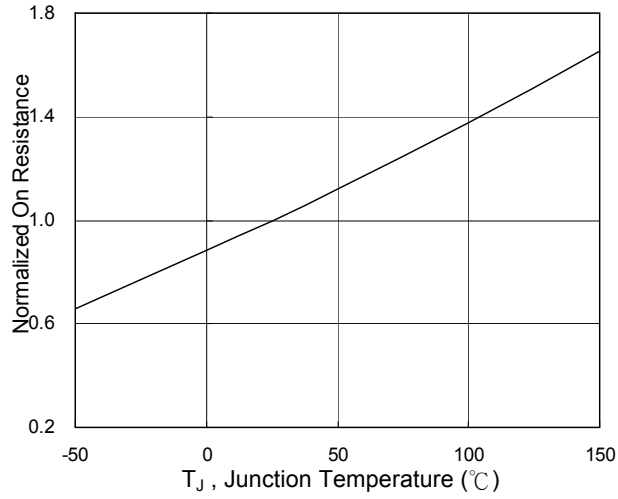



Fig.6 Normalized $R_{DSON}$ vs. $T_J$

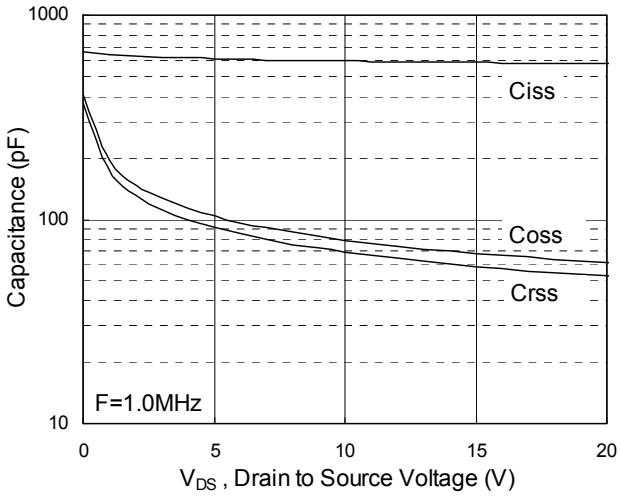



Fig.7 Capacitance

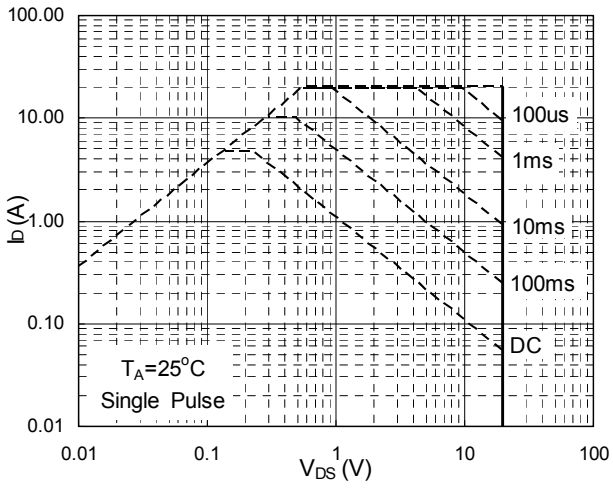



Fig.8 Safe Operating Area

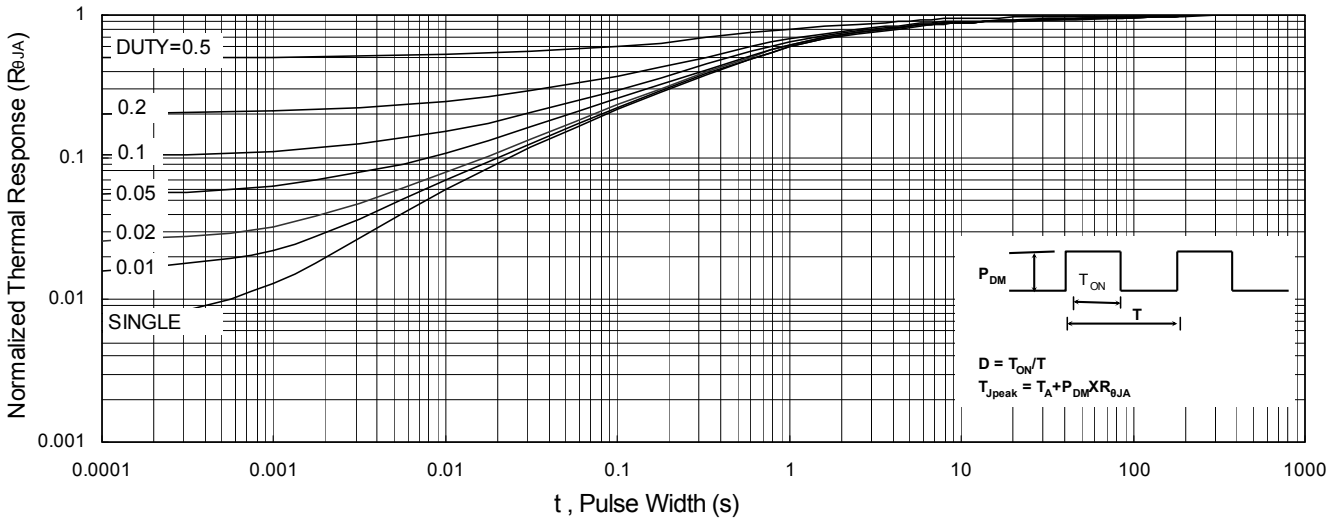



Fig.9 Normalized Maximum Transient Thermal Impedance

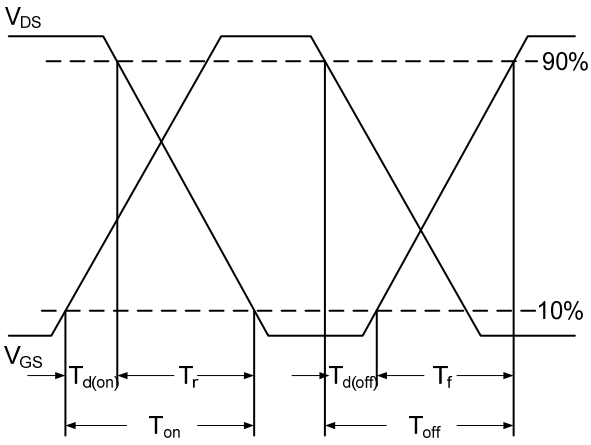



Fig.10 Switching Time Waveform

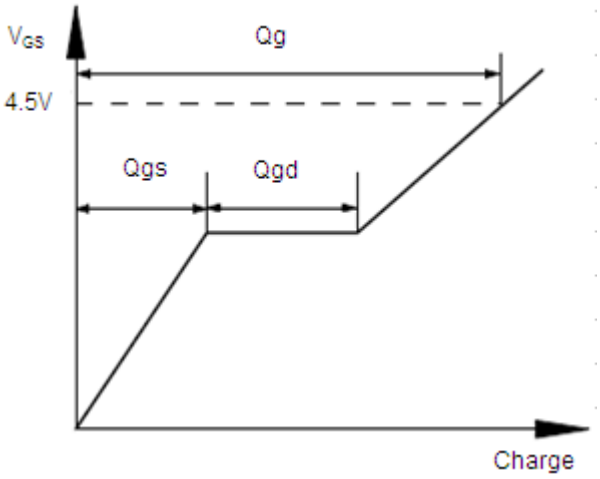



Fig.11 Gate Charge Waveform

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