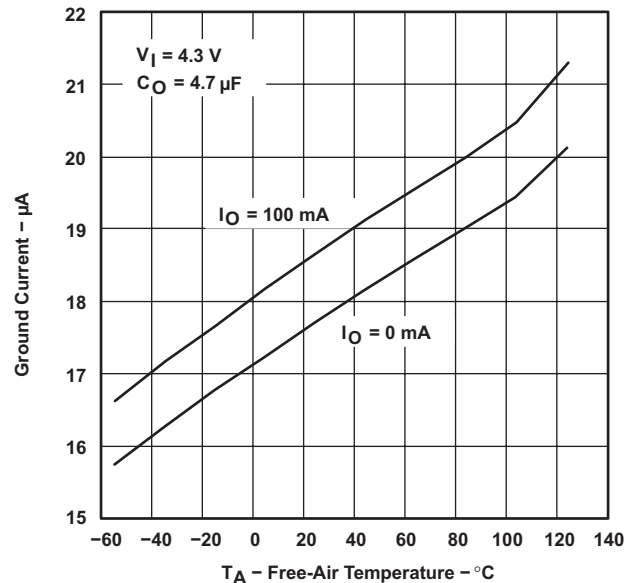
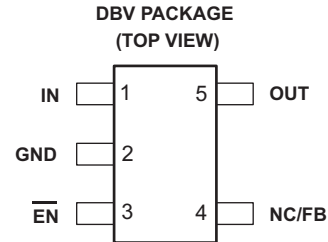


Ultralow-Power 100-mA Low-Dropout Linear Regulators

Check for Samples: [TPS76901-Q1](#), [TPS76912-Q1](#), [TPS76915-Q1](#), [TPS76918-Q1](#), [TPS76925-Q1](#), [TPS76927-Q1](#), [TPS76928-Q1](#), [TPS76930-Q1](#), [TPS76933-Q1](#), [TPS76950-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 100-mA Low-Dropout Regulator
- Available in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V and 5-V Fixed-Output and Adjustable Versions
- Only 17- μ A Quiescent Current at 100 mA
- 1- μ A Quiescent Current in Standby Mode
- Dropout Voltage Typically 71 mV at 100 mA
- Over Current Limitation
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



DESCRIPTION

The TPS769xx-Q1 family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, ultralow-power operation, and miniaturized packaging. These regulators feature low-dropout voltages and ultralow quiescent current compared to conventional LDO regulators. Offered in a 5-pin small outline integrated-circuit SOT-23 package, the TPS769xx-Q1 series devices are ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 71 mV at 100 mA of load current (TPS76950-Q1), and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (28 μ A maximum) and is stable over the entire range of output load current (0 mA to 100 mA). The ultralow-dropout voltage feature and ultralow-power operation result in a significant increase in system battery operating life, making this device suitable for use in automotive applications.

The TPS769xx-Q1 devices also feature a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μ A typical at $T_J = 25^\circ\text{C}$. The TPS769xx-Q1 devices are offered in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.2 V to 5.5 V).



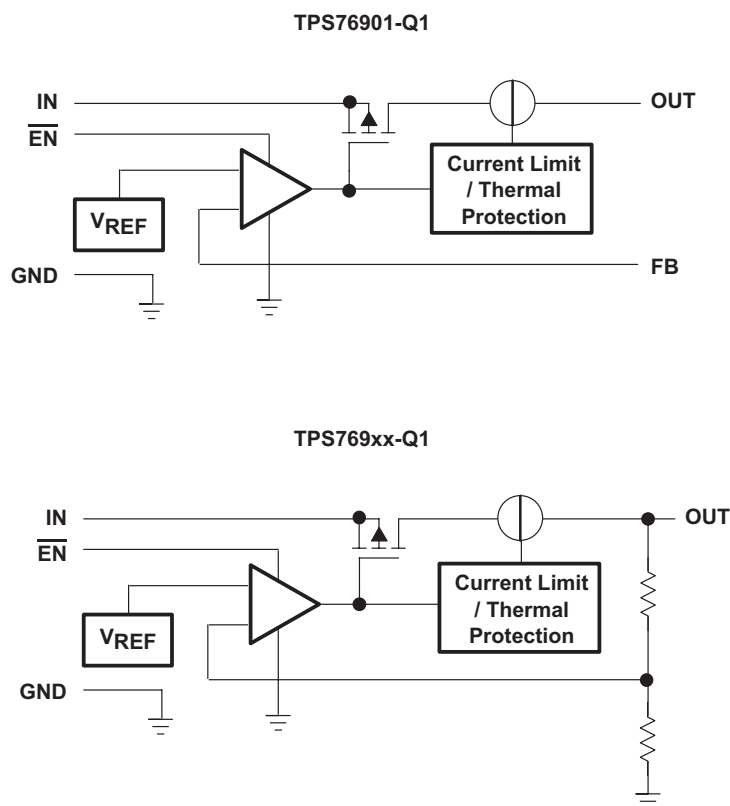
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

T _J	VOLTAGE	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER		SYMBOL
-40°C to 125°C	Variable 1.2 V to 5.5 V	SOT-23 (DBV)	TPS76901QDBVTQ1 ⁽³⁾	TPS76901QDBVRQ1 ⁽⁴⁾	PCFQ
	1.2 V		TPS76912QDBVTQ1	TPS76912QDBVRQ1	PCGQ
	1.5 V		TPS76915QDBVTQ1	TPS76915QDBVRQ1	PCHQ
	1.8 V		TPS76918QDBVTQ1	TPS76918QDBVRQ1	PCIQ
	2.5 V		TPS76925QDBVTQ1	TPS76925QDBVRQ1	PCJQ
	2.7 V		TPS76927QDBVTQ1	TPS76927QDBVRQ1	PCKQ
	2.8 V		TPS76928QDBVTQ1	TPS76928QDBVRQ1	PCLQ
	3 V		TPS76930QDBVTQ1	TPS76930QDBVRQ1	PCMQ
	3.3 V		TPS76933QDBVTQ1	TPS76933QDBVRQ1	PCNQ
	5 V		TPS76950QDBVTQ1	TPS76950QDBVRQ1	PCOQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
 (3) The DBVT indicates a tape and reel of 250 parts.
 (4) The DBVR indicates a tape and reel of 3000 parts.

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	2		Ground
$\overline{\text{EN}}$	3	I	Enable input
FB	4	I	Feedback voltage (TPS76901-Q1 only)
IN	1	I	Input supply voltage
NC	4		No connection (Fixed options only)
OUT	5	O	Regulated output voltage

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Input voltage range ⁽²⁾	-0.3 to 13.5	V
Voltage range at $\overline{\text{EN}}$	-0.3 to $V_I + 0.3$	V
Voltage on OUT, FB	7	V
Peak output current	Internally Limited	
ESD rating, HBM	2	kV
Continuous total power dissipation	See Dissipation Rating Table	
T_J Operating virtual junction temperature range	-40 to 150	°C
T_{stg} Storage temperature range	-65 to 150	°C

- Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Low K ⁽¹⁾	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K ⁽²⁾	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C	555 mW	305 mW	222 mW

- The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
- The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_I ⁽¹⁾	2.7		10	V
Output voltage range, V_O	1.2		5.5	V
Continuous output current, I_O ⁽²⁾	0		100	mA
Operating junction temperature, T_J	-40		125	°C

- To calculate the minimum input voltage for your maximum output current, use the following formula: $V_I (\text{min}) = V_O (\text{max}) + V_{\text{DO}}$ (max load)
- Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_I = V_O$ (typ) + 1 V, $I_O = 100$ mA, $\overline{EN} = 0$ V, $C_O = 4.7$ μ F (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output voltage (10 μ A to 100 mA load) ⁽¹⁾	TPS76901-Q1	$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$		V_O		
		$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C		$0.97 V_O$	$1.03 V_O$	
	TPS76912-Q1	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{IN} < 10 \text{ V}$		1.224		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{IN} < 10 \text{ V}$		1.187	1.261	
	TPS76915-Q1	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{IN} < 10 \text{ V}$		1.5		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{IN} < 10 \text{ V}$		1.455	1.545	
	TPS76918-Q1	$T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{IN} < 10 \text{ V}$		1.8		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{IN} < 10 \text{ V}$		1.746	1.854	
	TPS76925-Q1	$T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{IN} < 10 \text{ V}$		2.5		
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{IN} < 10 \text{ V}$		2.425	2.575	
	TPS76927-Q1	$T_J = 25^\circ\text{C}$, $3.7 \text{ V} < V_{IN} < 10 \text{ V}$		2.7		
		$T_J = -40^\circ\text{C}$ to 125°C , $3.7 \text{ V} < V_{IN} < 10 \text{ V}$		2.619	2.781	
	TPS76928-Q1	$T_J = 25^\circ\text{C}$, $3.8 \text{ V} < V_{IN} < 10 \text{ V}$		2.8		
		$T_J = -40^\circ\text{C}$ to 125°C , $3.8 \text{ V} < V_{IN} < 10 \text{ V}$		2.716	2.884	
	TPS76930-Q1	$T_J = 25^\circ\text{C}$, $4 \text{ V} < V_{IN} < 10 \text{ V}$		3		
		$T_J = -40^\circ\text{C}$ to 125°C , $4 \text{ V} < V_{IN} < 10 \text{ V}$		2.910	3.090	
	TPS76933-Q1	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{IN} < 10 \text{ V}$		3.3		
		$T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{IN} < 10 \text{ V}$		3.201	3.399	
TPS76950-Q1	$T_J = 25^\circ\text{C}$, $6 \text{ V} < V_{IN} < 10 \text{ V}$		5			
	$T_J = -40^\circ\text{C}$ to 125°C , $6 \text{ V} < V_{IN} < 10 \text{ V}$		4.850	5.150		
Quiescent current (GND current) ⁽¹⁾⁽²⁾	$\overline{EN} = 0$ V, $0 \text{ mA} < I_O < 100 \text{ mA}$, $T_J = 25^\circ\text{C}$		17		μ A	
	$\overline{EN} = 0$ V, $I_O = 100 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			28		
Load regulation	$\overline{EN} = 0$ V, $I_O = 0$ to 100 mA , $T_J = 25^\circ\text{C}$		12		mV	
Output voltage line regulation ($\Delta V_O/V_O$) ⁽²⁾	$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$ ⁽¹⁾		0.04		%V	
	$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C ⁽¹⁾			0.1		
Output noise voltage	BW = 300 Hz to 50 kHz, $C_O = 10 \mu$ F, $T_J = 25^\circ\text{C}$		190		μ V _{rms}	
Output current limit	$V_O = 0$ V ⁽¹⁾		350	750	mA	
Standby current	$\overline{EN} = V_I$, $2.7 \text{ V} < V_I < 10 \text{ V}$		1		μ A	
	$T_J = -40^\circ\text{C}$ to 125°C			2	μ A	
FB input current	FB = 1.224 V (TPS76901-Q1)		-1	1	μ A	
High level enable input voltage	$2.7 \text{ V} < V_I < 10 \text{ V}$		1.7		V	
Low level enable input voltage	$2.7 \text{ V} < V_I < 10 \text{ V}$			0.9	V	
Power supply ripple rejection	f = 1 kHz, $C_O = 10 \mu$ F, $T_J = 25^\circ\text{C}$		60		dB	
Input current (\overline{EN})	$\overline{EN} = 0$ V		-1	0	μ A	
	$\overline{EN} = V_I$		-1	1	μ A	

(1) Minimum IN operating voltage is 2.7 V or V_O (typ) + 1 V, whichever is greater. The maximum IN voltage is 10 V, minimum output current is 10 μ A, and maximum output current is 100 mA.

(2) If $V_O \leq 1.8$ V then $V_{Imin} = 2.7$ V, $V_{Imax} = 10$ V:
 Line Reg. (mV) = (% / V) $\times \frac{V_O (V_{Imax} - 2.7 \text{ V})}{100} \times 1000$

If $V_O \geq 2.5$ V then $V_{Imin} = V_O + 1$ V, $V_{Imax} = 10$ V:
 Line Reg. (mV) = (% / V) $\times \frac{V_O (V_{Imax} - (V_O + 1 \text{ V}))}{100} \times 1000$

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $V_I = V_O$ (typ) + 1 V, $I_O = 100$ mA, $\overline{EN} = 0$ V, $C_O = 4.7$ μ F (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout voltage ⁽³⁾	TPS76928-Q1	$I_O = 50$ mA, $T_J = 25^\circ\text{C}$		60		mV
		$I_O = 50$ mA, $T_J = -40^\circ\text{C}$ to 125°C			125	
		$I_O = 100$ mA, $T_J = 25^\circ\text{C}$		122		
		$I_O = 100$ mA, $T_J = -40^\circ\text{C}$ to 125°C			245	
	TPS76930-Q1	$I_O = 50$ mA, $T_J = 25^\circ\text{C}$		57		
		$I_O = 50$ mA, $T_J = -40^\circ\text{C}$ to 125°C			115	
		$I_O = 100$ mA, $T_J = 25^\circ\text{C}$		115		
		$I_O = 100$ mA, $T_J = -40^\circ\text{C}$ to 125°C			230	
	TPS76933-Q1	$I_O = 50$ mA, $T_J = 25^\circ\text{C}$		48		
		$I_O = 50$ mA, $T_J = -40^\circ\text{C}$ to 125°C			100	
		$I_O = 100$ mA, $T_J = 25^\circ\text{C}$		98		
		$I_O = 100$ mA, $T_J = -40^\circ\text{C}$ to 125°C			200	
	TPS76950-Q1	$I_O = 50$ mA, $T_J = 25^\circ\text{C}$		35		
		$I_O = 50$ mA, $T_J = -40^\circ\text{C}$ to 125°C			85	
		$I_O = 100$ mA, $T_J = 25^\circ\text{C}$		71		
		$I_O = 100$ mA, $T_J = -40^\circ\text{C}$ to 125°C			170	

(3) The IN voltage equals V_O (typ) – 100 mV; the TPS76901-Q1 output voltage is set to 3.3 V nominal with an external resistor divider. TPS76912-Q1, TPS76915-Q1, TPS76918-Q1, TPS76925-Q1, and TPS76927-Q1 dropout voltage is limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

TPS76925-Q1 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

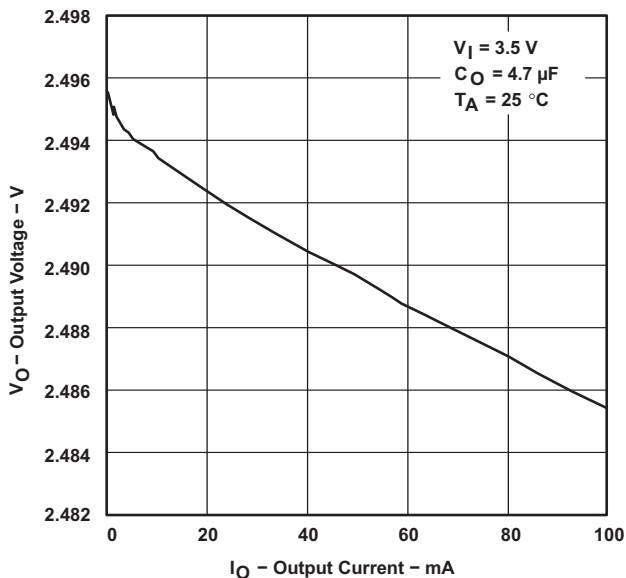


Figure 1.

TPS76915-Q1 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

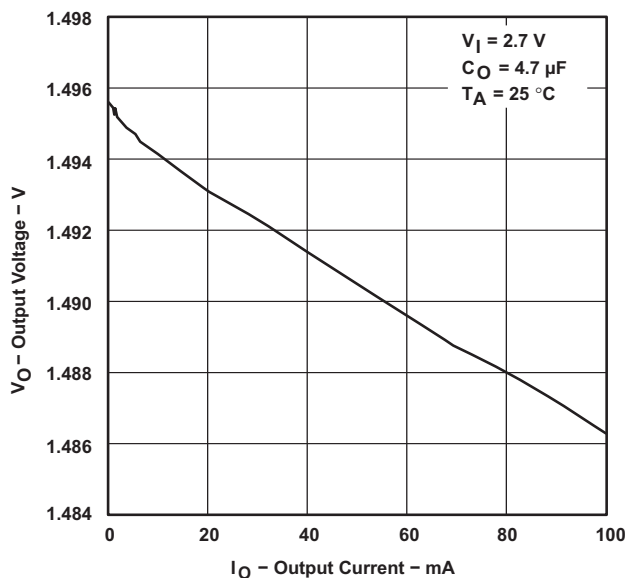


Figure 2.

TPS76933-Q1 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

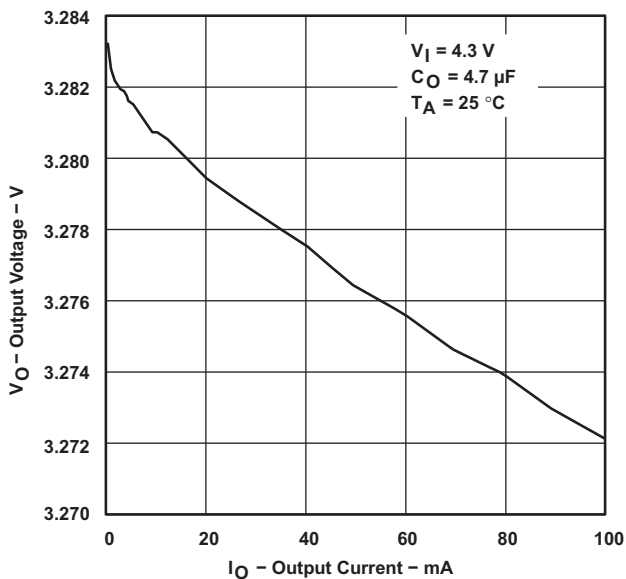


Figure 3.

TPS76915-Q1 OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

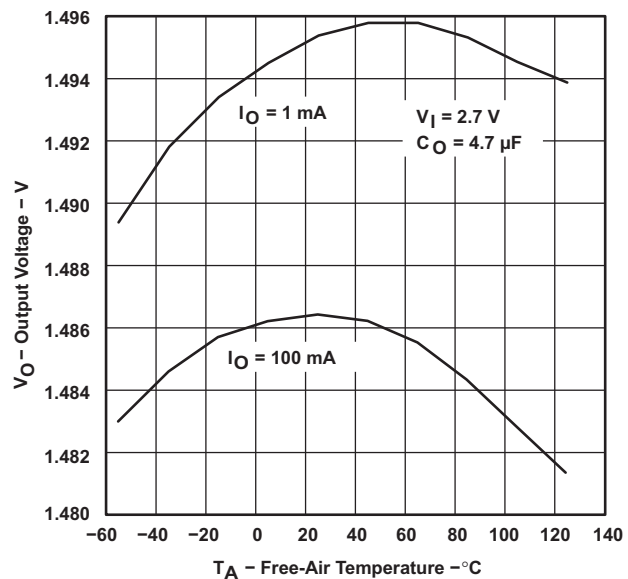


Figure 4.

TYPICAL CHARACTERISTICS (continued)

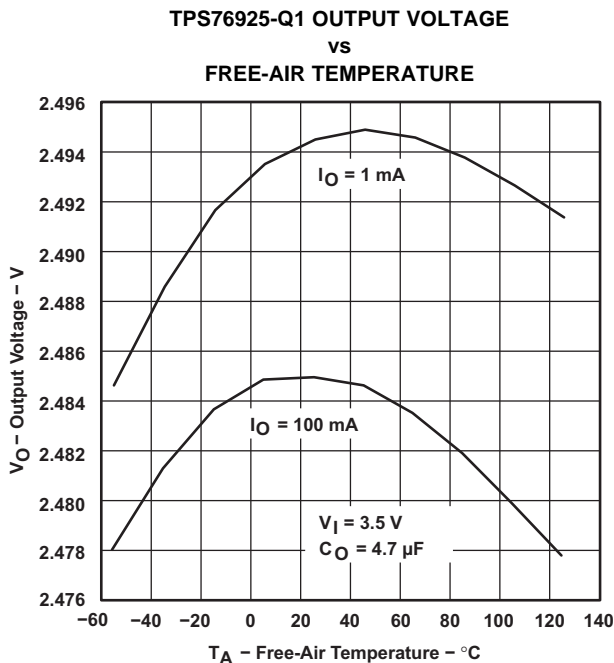


Figure 5.

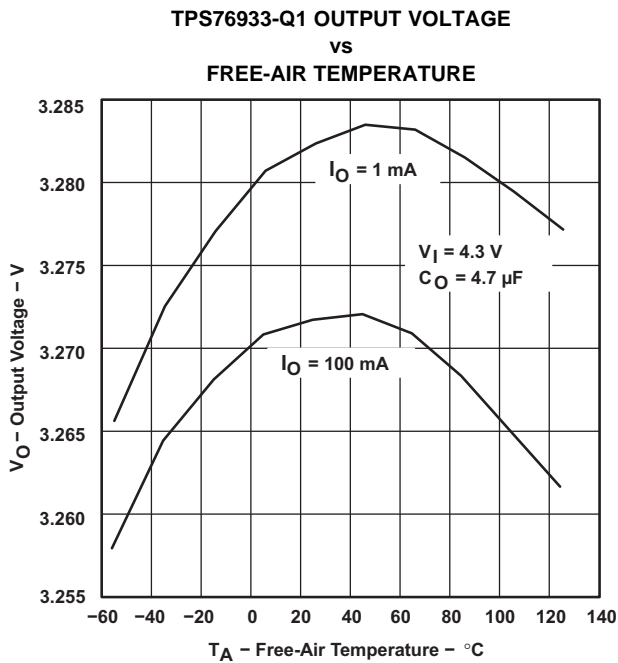


Figure 6.

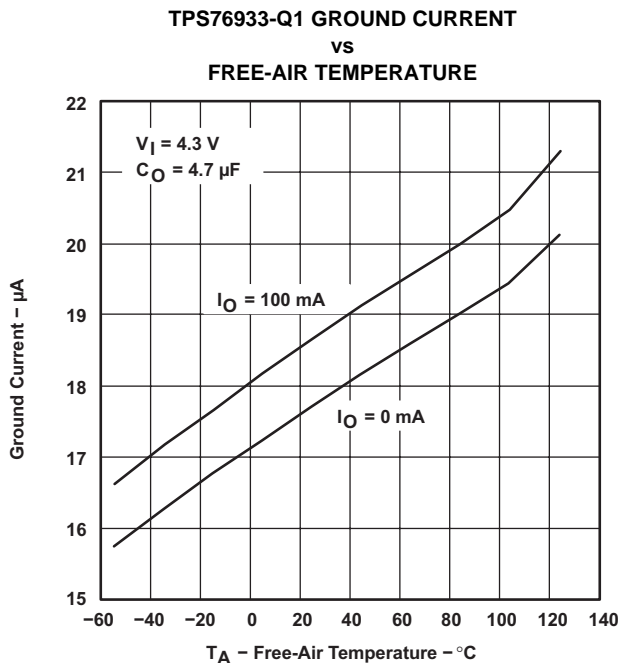


Figure 7.

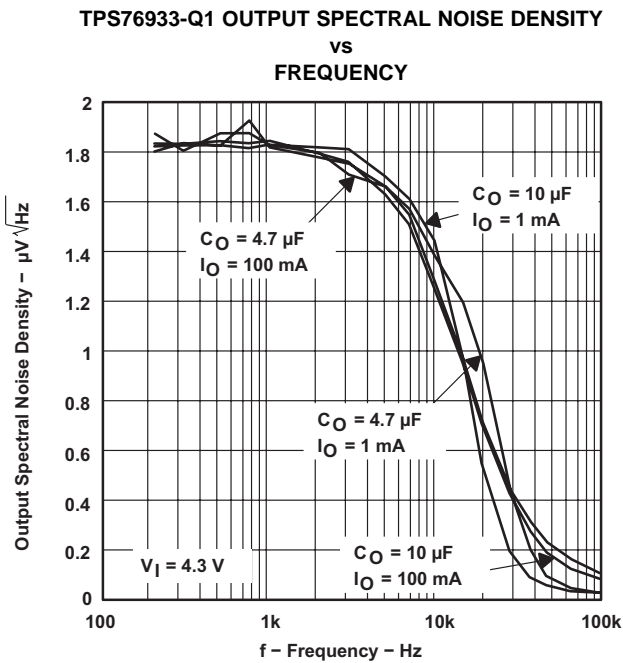
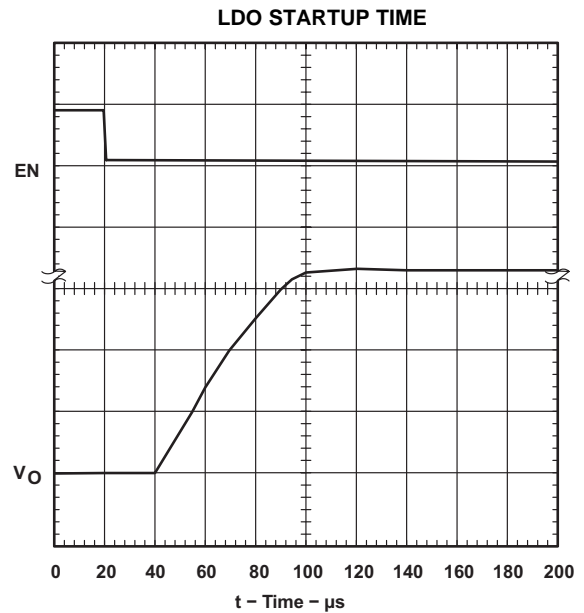
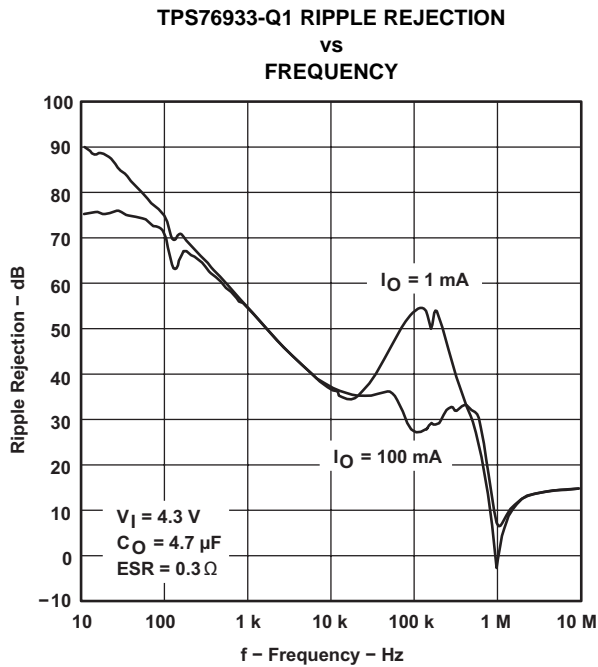
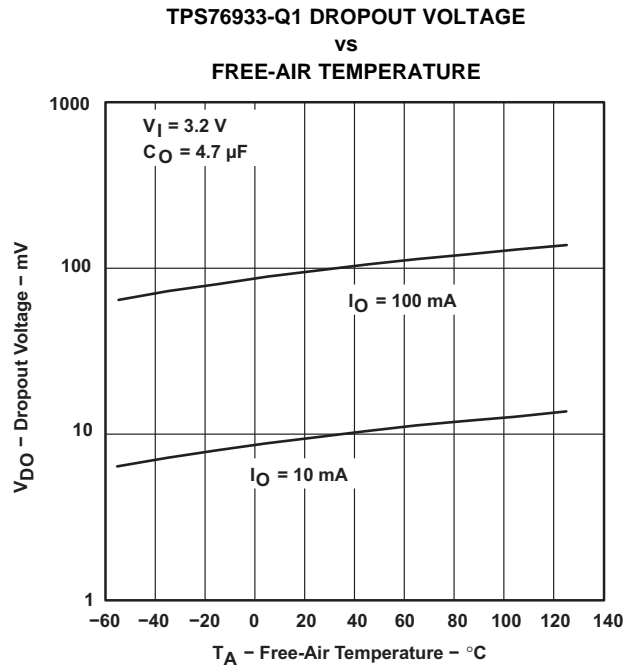
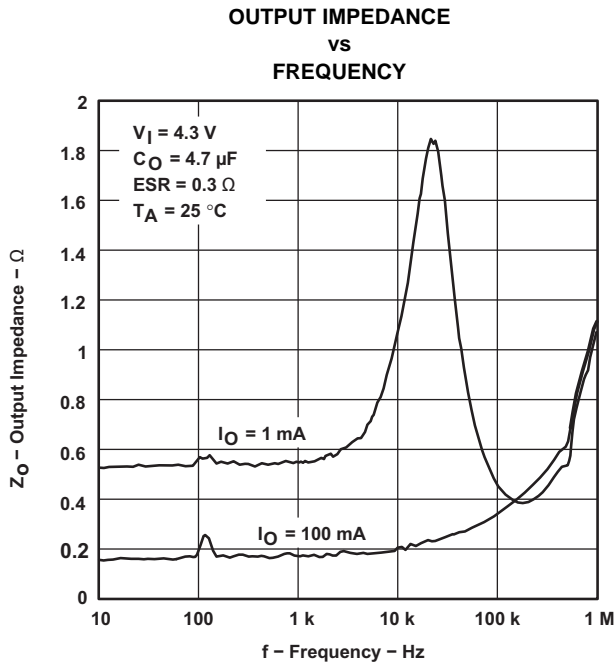


Figure 8.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

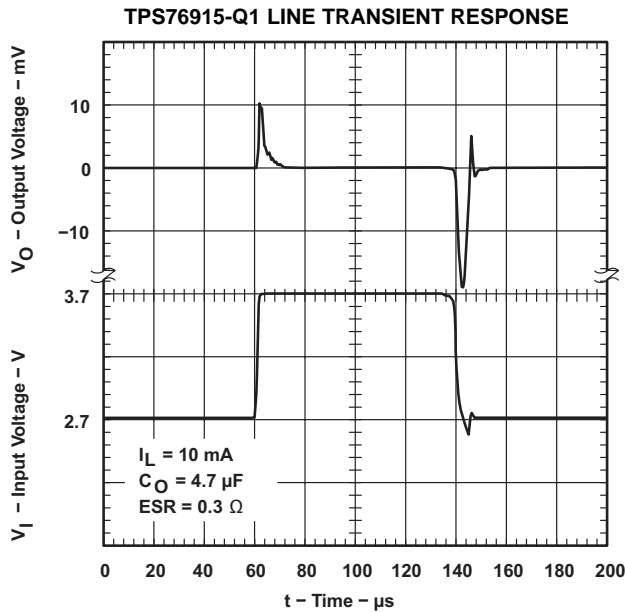


Figure 13.

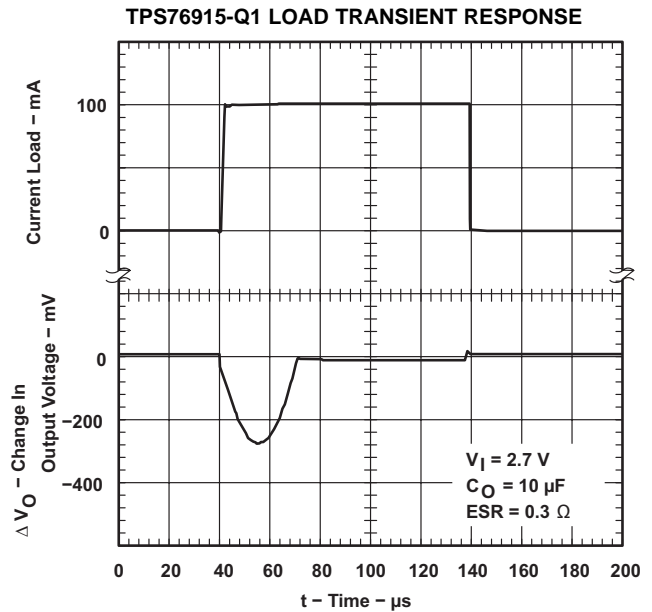


Figure 14.

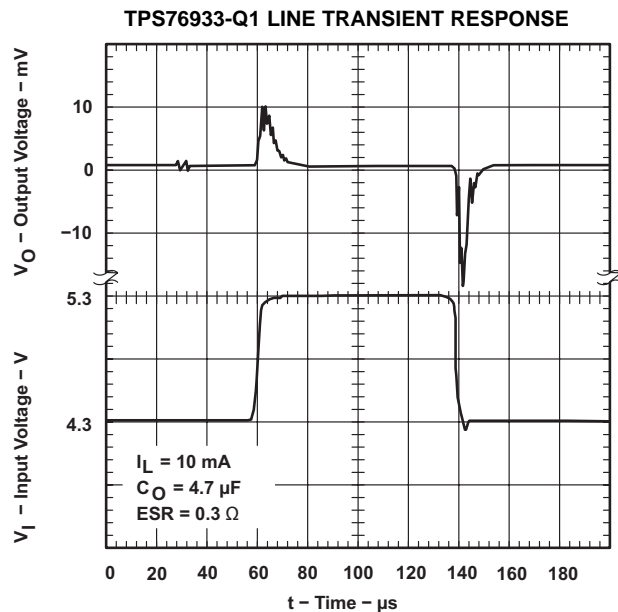


Figure 15.

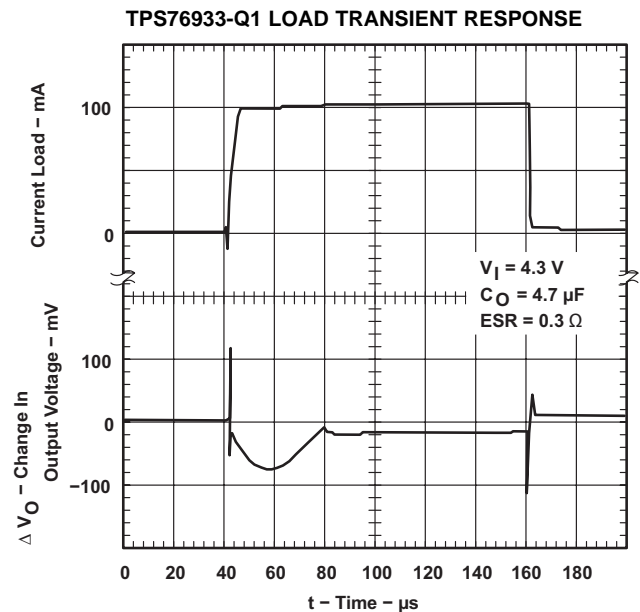


Figure 16.

TYPICAL CHARACTERISTICS (continued)

TPS76933-Q1 TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

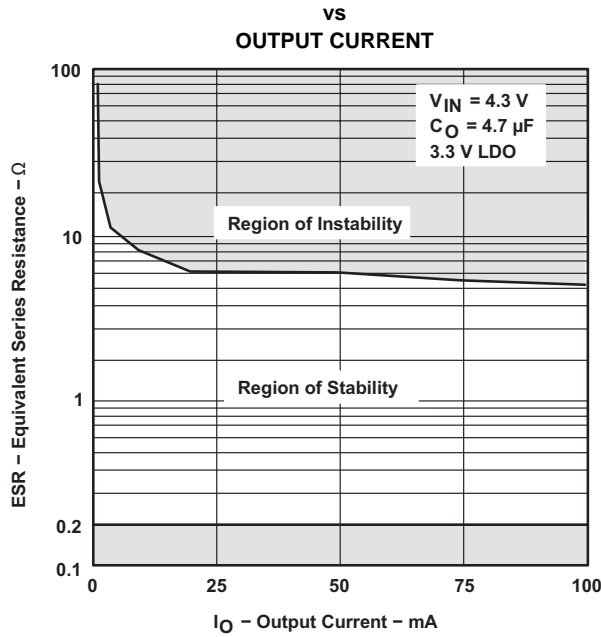


Figure 17.

TPS76933-Q1 TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

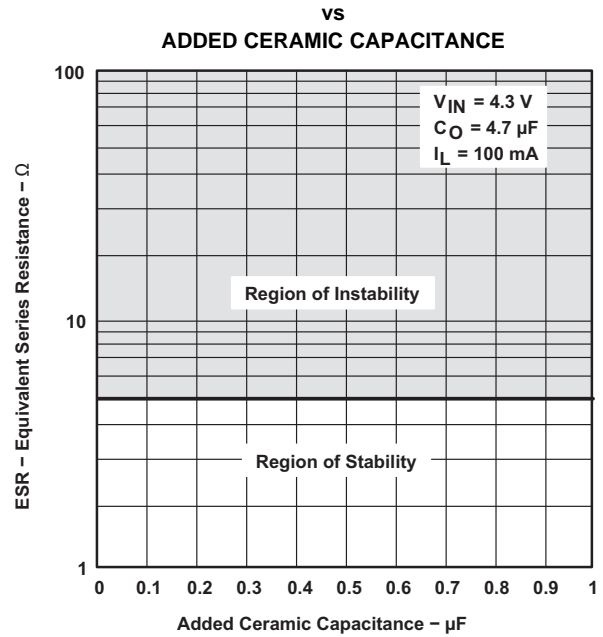


Figure 18.

TPS76933-Q1 TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

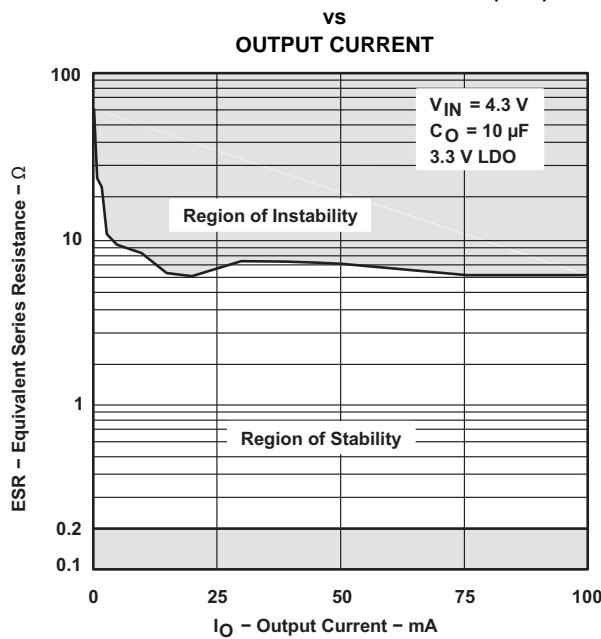


Figure 19.

TPS76933-Q1 TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

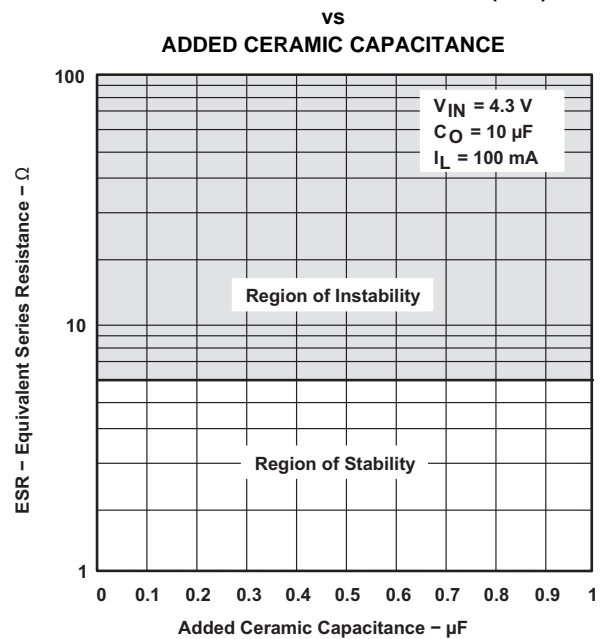


Figure 20.

APPLICATION INFORMATION

The TPS769xx-Q1 family of low-dropout (LDO) regulators are optimized for use in battery-operated equipment and automotive applications. They feature extremely low dropout voltages, low quiescent current (17 μA nominally), and enable inputs to reduce supply currents to 1 μA when the regulators are turned off.

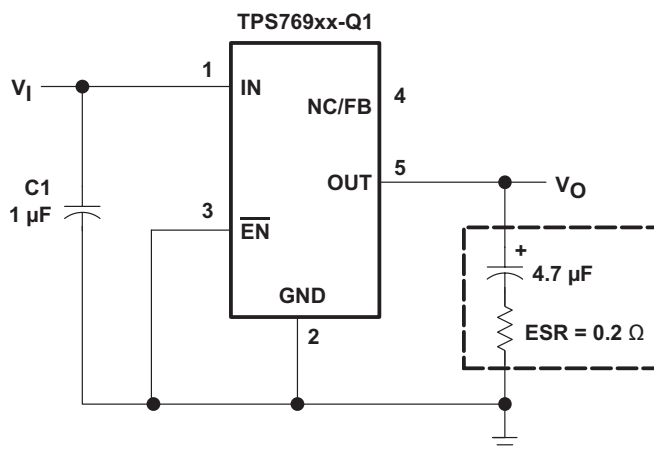
Device Operation

The TPS769xx-Q1 uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS769xx-Q1 is essentially constant from no load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the $\overline{\text{EN}}$ input will disable the TPS769xx-Q1 internal circuitry, reducing the supply current to 1 μA . A voltage of less than 0.9 V on the $\overline{\text{EN}}$ input will enable the TPS769xx and will enable normal operation to resume. The $\overline{\text{EN}}$ input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

A typical application circuit is shown in [Figure 21](#).



TPS76912-Q1, TPS76915-Q1, TPS76918-Q1, TPS76925-Q1, TPS76927-Q1, TPS76928-Q1, TPS76930-Q1, TPS76933-Q1, TPS76950-Q1 (fixed-voltage options).

Figure 21. Typical Application Circuit

External Capacitor Requirements

Although not required, a 0.047- μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS769xx-Q1, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS769xx-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μF . The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω to ensure stability. Capacitor values larger than 4.7 μF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 μF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum

electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may therefore require the addition of a low value series resistor to ensure stability.

Table 1. Capacitor Selection

PART NO.	MFR.	VALUE	MAX ESR	SIZE (H x L x W) ⁽¹⁾
T494B475K016AS	KEMET	4.7 μF	1.5 Ω	1.9 x 3.5 x 2.8
195D106x0016x2T	SPRAGUE	10 μF	1.5 Ω	1.3 x 7 x 2.7
695D106x003562T	SPRAGUE	10 μF	1.3 Ω	2.5 x 7.6 x 2.5
TPSC475K035R0600	AVX	4.7 μF	0.6 Ω	2.6 x 6 x 3.2

(1) Size is in mm. ESR is maximum resistance in Ω at 100 kHz and $T_A = 25^\circ\text{C}$. Contact manufacturer for minimum ESR values.

Output Voltage Programming

The output voltage of the TPS76901-Q1 adjustable regulator is programmed using an external resistor divider as shown in [Figure 22](#). The output voltage is calculated using:

$$V_O = V_{\text{ref}} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

$V_{\text{ref}} = 1.224 \text{ V typ}$ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7- μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose $R2 = 169 \text{ k}\Omega$ to set the divider current at 7 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \times R2 \quad (2)$$

Table 2. Output Voltage Programming Guide

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (k Ω) ⁽¹⁾	
	R1	R2
2.5	174	169
3.3	287	169
3.6	324	169
4	383	169
5	523	169

(1) 1% values shown.

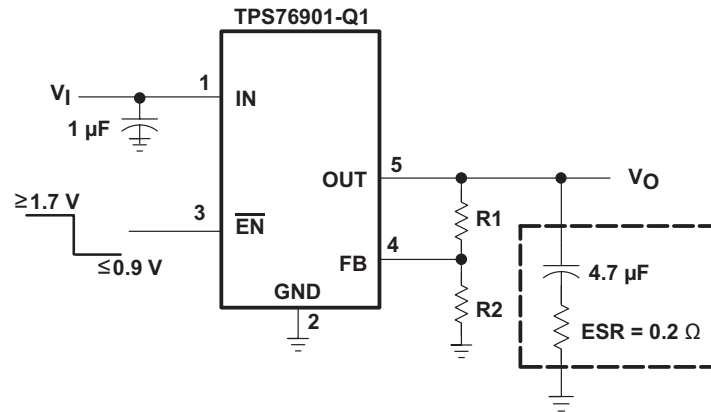


Figure 22. TPS76901-Q1 Adjustable LDO Regulator Programming

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (3)$$

Where:

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

Regulator Protection

The TPS769xx-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS769xx-Q1 features internal current limiting and thermal protection. During normal operation, the TPS769xx-Q1 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

REVISION HISTORY

Changes from Revision B (April, 2008) to Revision C	Page
• Changed TPS769xx part names to TPS769xx-Q1 in text and images.	1
• Updated Figures 17 and 19 to include region of Instability below 0.2 Ω	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76901QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCFQ	Samples
TPS76901QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCFQ	Samples
TPS76912QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCGQ	Samples
TPS76915QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCHQ	Samples
TPS76915QDBVRQ1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
TPS76918QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCIQ	Samples
TPS76918QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCIQ	Samples
TPS76925QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCJQ	Samples
TPS76925QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCJQ	Samples
TPS76927QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCKQ	Samples
TPS76927QDBVRQ1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
TPS76928QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCLQ	Samples
TPS76930QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCMQ	Samples
TPS76930QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCMQ	Samples
TPS76933QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCNQ	Samples
TPS76933QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCNQ	Samples
TPS76950QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCOQ	Samples
TPS76950QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCOQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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● Catalog: [TPS76901](#), [TPS76912](#), [TPS76915](#), [TPS76918](#), [TPS76925](#), [TPS76927](#), [TPS76928](#), [TPS76930](#), [TPS76933](#), [TPS76950](#)

- Enhanced Product: [TPS76901-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76901QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76901QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76912QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76915QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76918QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76918QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76925QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76925QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76927QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76928QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76930QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76930QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76933QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76933QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76950QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76950QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76901QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76901QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76912QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76915QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76918QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76918QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76925QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76925QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76927QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76928QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76930QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76930QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76933QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76933QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76950QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76950QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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