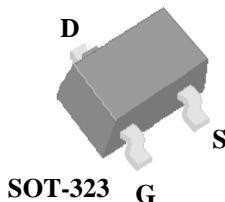




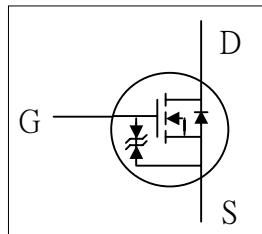
- ▼ Lower Gate Charge
- ▼ Capable of 2.5V Gate Drive
- ▼ Small Package Outline
- ▼ RoHS Compliant & Halogen-Free



| | |
|--------------|-------|
| BV_{DSS} | 20V |
| $R_{DS(ON)}$ | 0.6 Ω |
| I_D^3 | 600mA |

Description

AP1332 series are from Advanced Power innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.



Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Rating | Unit |
|--------------------------------|---|------------|------|
| V_{DS} | Drain-Source Voltage | 20 | V |
| V_{GS} | Gate-Source Voltage | ± 8 | V |
| $I_D @ T_A = 25^\circ\text{C}$ | Drain Current ³ , $V_{GS} @ 4.5\text{V}$ | 600 | mA |
| $I_D @ T_A = 70^\circ\text{C}$ | Drain Current ³ , $V_{GS} @ 4.5\text{V}$ | 470 | mA |
| I_{DM} | Pulsed Drain Current ¹ | 2.5 | A |
| $P_D @ T_A = 25^\circ\text{C}$ | Total Power Dissipation | 0.35 | W |
| T_{STG} | Storage Temperature Range | -55 to 150 | °C |
| T_J | Operating Junction Temperature Range | -55 to 150 | °C |

Thermal Data

| Symbol | Parameter | Value | Unit |
|-------------|---|-------|------|
| R_{thj-a} | Maximum Thermal Resistance, Junction-ambient ³ | 360 | °C/W |



Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------------|--|--|------|------|----------|---------------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$ | 20 | - | - | V |
| $R_{\text{DS}(\text{ON})}$ | Static Drain-Source On-Resistance ² | $V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=600\text{mA}$ | - | - | 0.6 | Ω |
| | | $V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=300\text{mA}$ | - | - | 2 | Ω |
| $V_{\text{GS}(\text{th})}$ | Gate Threshold Voltage | $V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$ | 0.5 | - | 1.25 | V |
| g_{fs} | Forward Transconductance | $V_{\text{DS}}=5\text{V}, I_{\text{D}}=600\text{mA}$ | - | 1 | - | S |
| I_{DSS} | Drain-Source Leakage Current | $V_{\text{DS}}=16\text{V}, V_{\text{GS}}=0\text{V}$ | - | - | 10 | μA |
| I_{GSS} | Gate-Source Leakage | $V_{\text{GS}}=\pm 8\text{V}, V_{\text{DS}}=0\text{V}$ | - | - | ± 30 | μA |
| Q_g | Total Gate Charge | $I_{\text{D}}=600\text{mA}$ | - | 1.3 | 2 | nC |
| Q_{gs} | Gate-Source Charge | | - | 0.3 | - | nC |
| Q_{gd} | Gate-Drain ("Miller") Charge | | - | 0.5 | - | nC |
| $t_{\text{d}(\text{on})}$ | Turn-on Delay Time | $V_{\text{DS}}=10\text{V}$ $I_{\text{D}}=600\text{mA}$ | - | 21 | - | ns |
| t_r | Rise Time | | - | 53 | - | ns |
| $t_{\text{d}(\text{off})}$ | Turn-off Delay Time | | - | 100 | - | ns |
| t_f | Fall Time | | - | 125 | - | ns |
| C_{iss} | Input Capacitance | $V_{\text{GS}}=0\text{V}$ $V_{\text{DS}}=10\text{V}$ | - | 38 | 60 | pF |
| C_{oss} | Output Capacitance | | - | 17 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | | - | 12 | - | pF |

Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------|---------------------------------|--|------|------|------|------|
| V_{SD} | Forward On Voltage ² | $I_{\text{S}}=300\text{mA}, V_{\text{GS}}=0\text{V}$ | - | - | 1.2 | V |

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test.
- 3.Surface mounted on FR4 board, $t \leq 10$ sec.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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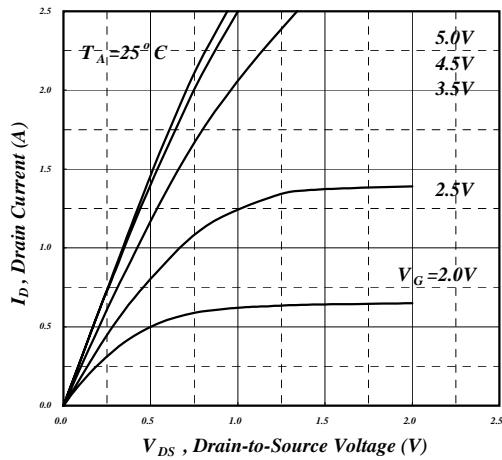


Fig 1. Typical Output Characteristics

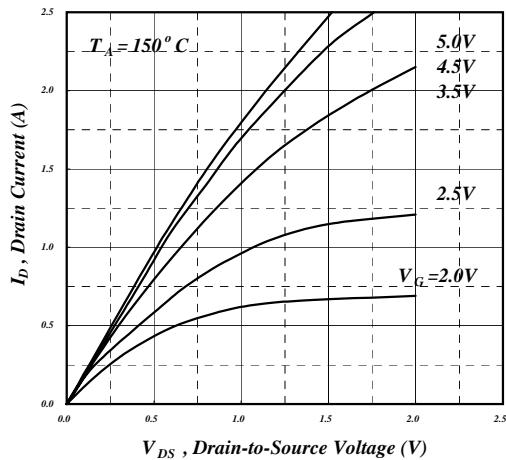


Fig 2. Typical Output Characteristics

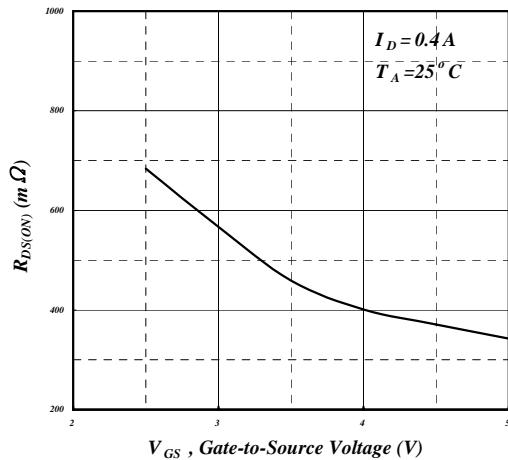


Fig 3. On-Resistance v.s. Gate Voltage

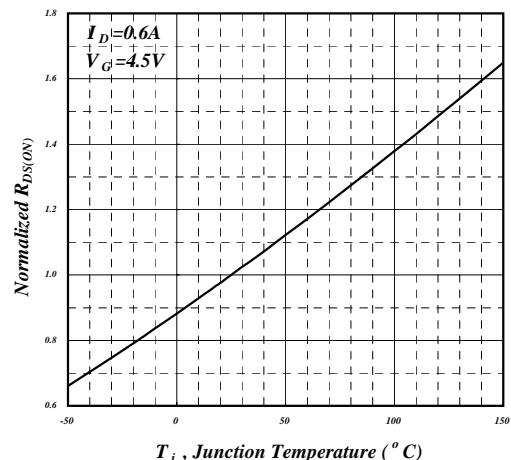


Fig 4. Normalized On-Resistance v.s. Junction Temperature

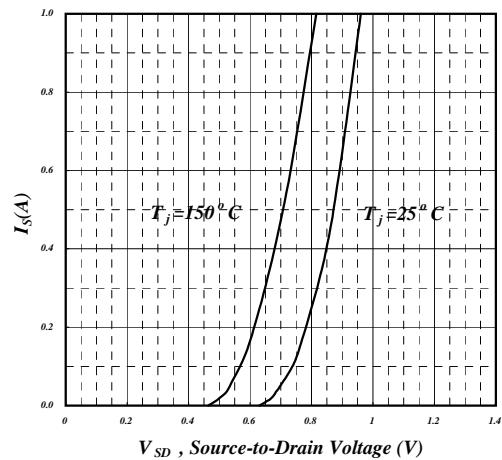


Fig 5. Forward Characteristic of Reverse Diode

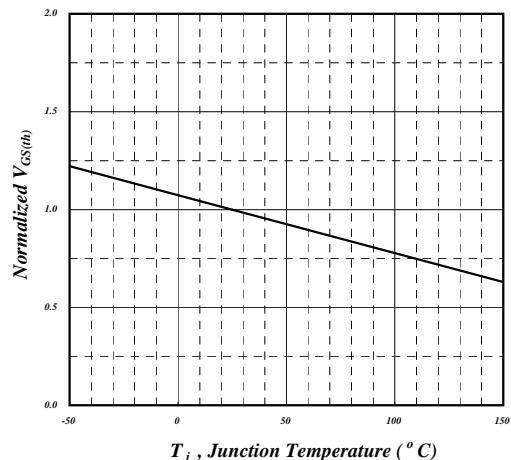


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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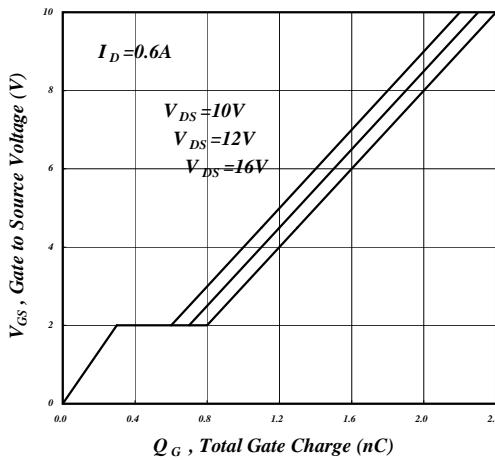


Fig 7. Gate Charge Characteristics

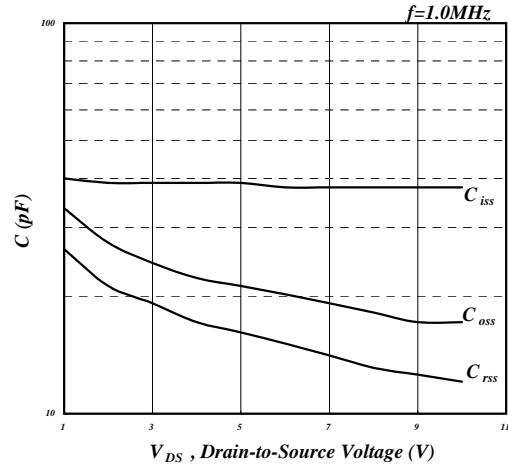


Fig 8. Typical Capacitance Characteristics

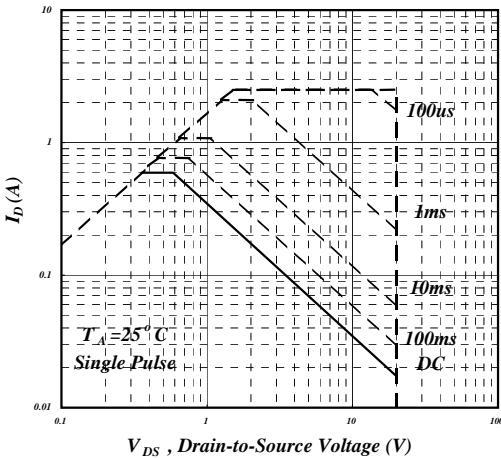


Fig 9. Maximum Safe Operating Area

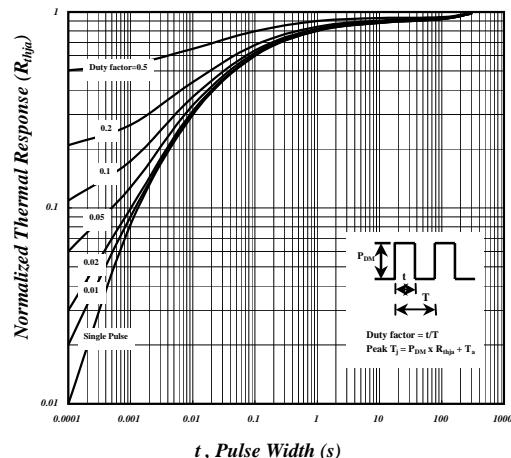


Fig 10. Effective Transient Thermal Impedance

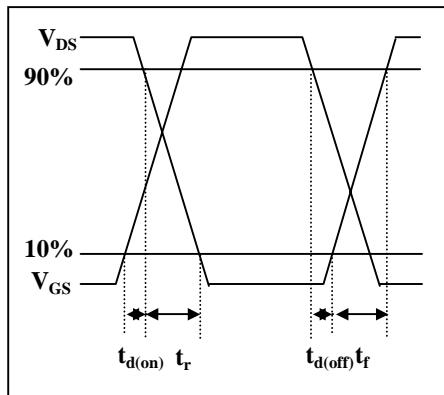


Fig 11. Switching Time Waveform

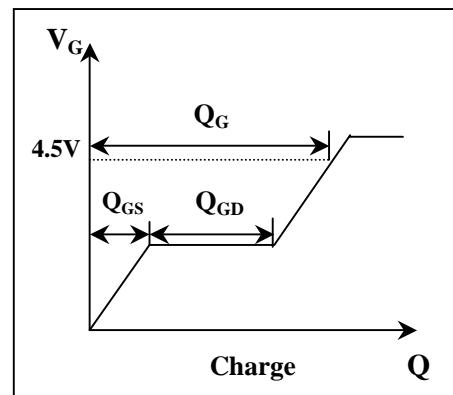


Fig 12. Gate Charge Waveform



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MARKING INFORMATION

