BITSTREAM CONVERSION

TFA9881

3.4 W PDM input class-D audio amplifier

Rev. 1 — 5 January 2011 Preliminary data sheet

1. General description

The TFA9881 is a mono, filter-free class-D audio amplifier in a 9-bump WLCSP (Wafer Level Chip-Size Package) with a 400 μm pitch.

The digital input interface is an over-sampled Pulse Density Modulated (PDM) bit stream. The TFA9881 receives audio and control settings via this interface. Dedicated silence patterns are used to configure the control settings of the device, such as mute, gain, Pulse Width Modulated (PWM) output slope, clip control and bandwidth extension (this control mechanism is not required if the default settings are used). The Power-down to Operating mode transition is triggered when a clock signal is detected.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in the TFA9881 provides excellent audio performance and high supply voltage ripple rejection.

2. Features and benefits

- Small outline WLCSP9 package: 1.3 × 1.3 × 0.6 mm
- Wide supply voltage range (fully operational from 2.5 V to 5.5 V)
- High efficiency (90 %, 4 Ω/20 μH load) and low power dissipation
- Quiescent power:
  - 6.5 mW (V_{DDD} = 1.8 V, V_{DDP} = 3.6 V, 4 Ω/20 μH load, f_{clk} = 2.048 MHz)
  - 7.8 mW (V_{DDD} = 1.8 V, V_{DDP} = 3.6 V, 4 Ω/20 μH load, f_{clk} = 6.144 MHz)
- Output power:
  - 1.4 W into 4 Ω at 3.6 V supply (THD = 1 %)
  - 2.7 W into 4 Ω at 5.0 V supply (THD = 1 %)
  - 3.4 W into 4 Ω at 5.0 V supply (THD = 10 %)
- Output noise voltage: 24 μV (A-weighted)
- Signal-to-noise ratio: 103 dB (V_{DDP} = 5 V, A-weighted)
- Fully short-circuit proof across load and to supply lines
- Current limiting to avoid audio holes
- Thermally protected
- Undervoltage and overvoltage protection
- High-pass filter for DC blocking
- Invalid data protection
- Simple two-wire interface for audio and control settings
- Left/right selection
- Three gain settings: −3 dB, 0 dB and +3 dB
- PWM output slope setting for EMI reduction

- Bandwidth extension to support low sampling frequencies
- Clip control for smooth clipping
- Mute mode
- 'Pop noise' free at all mode transitions
- Short power-up time: 2 ms
- Short power-down time: 5 μs
- 1.8 V/3.3 V tolerant digital inputs
- Low RF susceptibility
- Insensitive to input clock jitter
- Only two external components required

3. Applications

- Mobile phones
- PDAs
- Portable gaming devices
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- MP3 players/Portable media players

4. Quick reference data

Table 1. Quick reference data

All parameters are guaranteed for $V_{TEST} = V_{DDP} = 3.6$ V; $V_{DDD} = 1.8$ V; $R_L = 4\ \Omega$[1]; $L_L = 20\ \mu H$[1]; $f_i = 1$ kHz; $f_{clk} = 6.144$ MHz; $T_{amb} = 25$ °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}	2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{DDP}	power supply current	Operating mode with load	-	1.5	1.7	mA
		Mute mode	-	1.1	1.2	mA
		Power-down mode	-	0.1	1	μA
I_{DDD}	digital supply current	Operating mode	-	1.35	1.5	mA
		Mute mode	-	1.25	1.4	mA
		Power-down mode CLK = 0 V; DATA = 0 V	-	2	8	μA
$P_{o(RMS)}$	RMS output power	THD + N = 1 %				
		$V_{DDP} = 3.6$ V, $f_i = 100$ Hz	-	1.4	-	W
		$V_{DDP} = 5.0$ V, $f_i = 100$ Hz	-	2.7	-	W
		THD + N = 10 %				
		$V_{DDP} = 5.0$ V, $f_i = 100$ Hz	-	3.4	-	W
η_{po}	output power efficiency	$P_{o(RMS)} = 1.4$ W	-	90	-	%

[1] R_L = load resistance; L_L = load inductance.

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5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9881UK	WLCSP9	wafer level chip-size package; 9 bumps; 1.3 x 1.3 x 0.6 mm	TFA9881UK

6. Block diagram

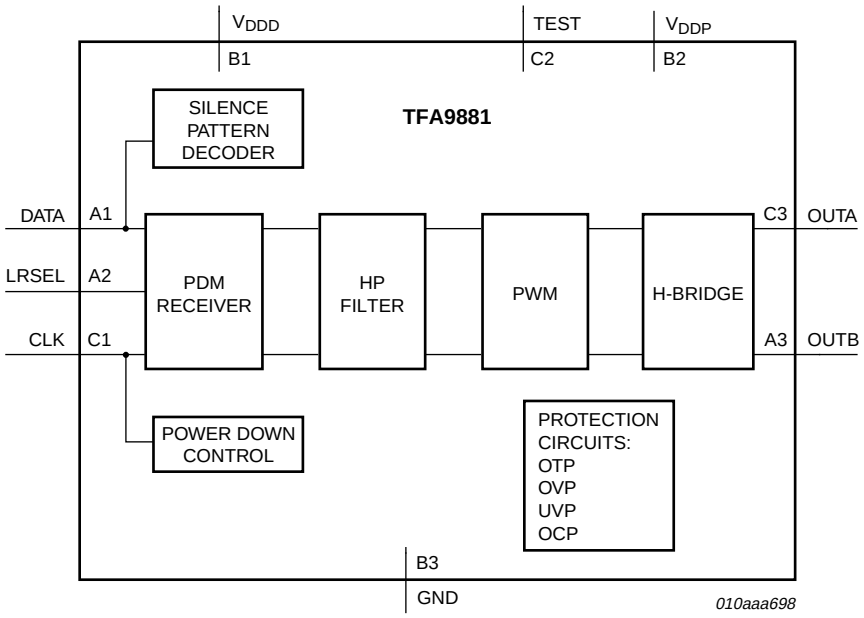


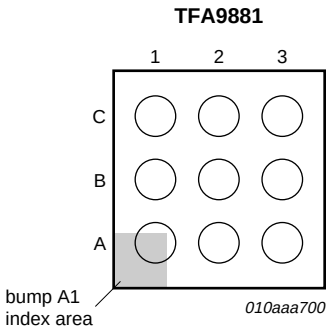
Fig 1. Block diagram

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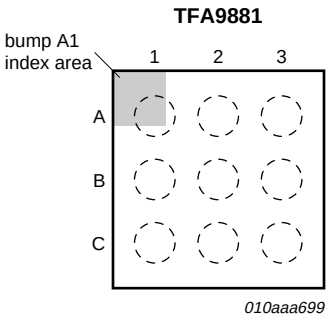
7. Pinning information

7.1 Pinning



Bottom view

Fig 2. Bump configuration for WLCSP9 (bottom view)



Transparent top view

Fig 3. Bump configuration for WLCSP9 (top view)

	1	2	3
A	DATA	LRSEL	OUTB
B	V_{DDD}	V_{DDP}	GND
C	CLK	TEST	OUTA

010aaa701

Transparent top view

Fig 4. Bump mapping for WLCSP9

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
DATA	A1	I	data input
LRSEL	A2	I	left/right selection
OUTB	A3	O	inverting output
V_{DDD}	B1	P	digital supply voltage (1.8 V)
V_{DDP}	B2	P	power supply voltage (2.5 V to 5.5 V)
GND	B3	P	ground reference
CLK	C1	I	clock input
TEST	C2	I	test pin (must be connected to V_{DDP})
OUTA	C3	O	non-inverting output

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8. Functional description

The TFA9881 is a high-efficiency mono Bridge Tied Load (BTL) class-D audio amplifier with a digital stereo PDM input interface. A High-Pass (HP) filter removes the DC components from the incoming PDM stream. This stream is subsequently converted into two PWM signals. A 3-level PWM scheme supports filterless speaker drive.

8.1 Mode selection and interfacing

The TFA9881 supports four operating modes:

- **Power-down mode**, with low supply current
- **Mute mode**, in which the output stages are floating so that the audio input signal is suppressed
- **Operating mode**, in which the amplifier is fully operational, delivering an output signal
- **Fault mode**

The TFA9881 switches to Fault mode automatically when a protection mechanism is activated (see Section 8.6). The defined patterns required on the CLK and DATA inputs to select the other three modes are given in Table 4.

Power-down mode is selected when there is no clock signal on the CLK input. Applying the clock signal will cause the TFA9881 to switch from Power-down mode to Operating mode. Power-down mode is also activated when the power-down silence pattern (at least 128 consecutive 0xAC bytes) is detected on the DATA input (see Section 8.4.1). The TFA9881 will switch to Power-down mode after byte 128 and will remain in Power-down mode as long as a continuous stream of consecutive 0xAC bytes is being received. It will switch to Operating mode if a byte other than 0xAC is received.

Mute mode is activated when the mute silence pattern (at least 32 consecutive 0x66 bytes) is detected on the DATA input. The TFA9881 will switch to Mute mode after byte 32 and will remain in Mute mode until a byte other than 0x66 is received.

Table 4. Mode selection

Mode	Pins		
	CLK frequency	Data pattern	OUTA, OUTB
Power-down	0 Hz	don't care	floating
	2 MHz to 8 MHz	activated after 128 consecutive 0xAC bytes	floating
Mute	2 MHz to 8 MHz	activated after 32 consecutive 0x66 bytes	floating
Operating	2 MHz to 8 MHz	PDM bit stream	switching

8.2 Digital stereo PDM audio input

The TFA9881 supports the digital stereo PDM stream illustrated in Figure 5. Table 5 shows the pin control configuration for left and right selection.

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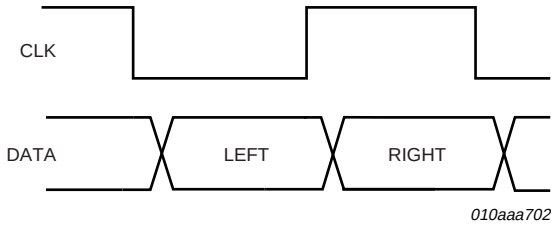


Fig 5. Digital stereo PDM selection

Table 5. Left/right selection

LRSEL pin state	Description
LOW	left content amplified
HIGH	right content amplified

8.3 Power up/down sequence

The TFA9881 power-up/power-down sequence is shown in Figure 6. External power supplies V_{DDP} and V_{DDD} should be within their operating limits before the TFA9881 switches to Operating mode. The TFA9881 should be switched to Power-down mode before the power supplies are disconnected or turned off.

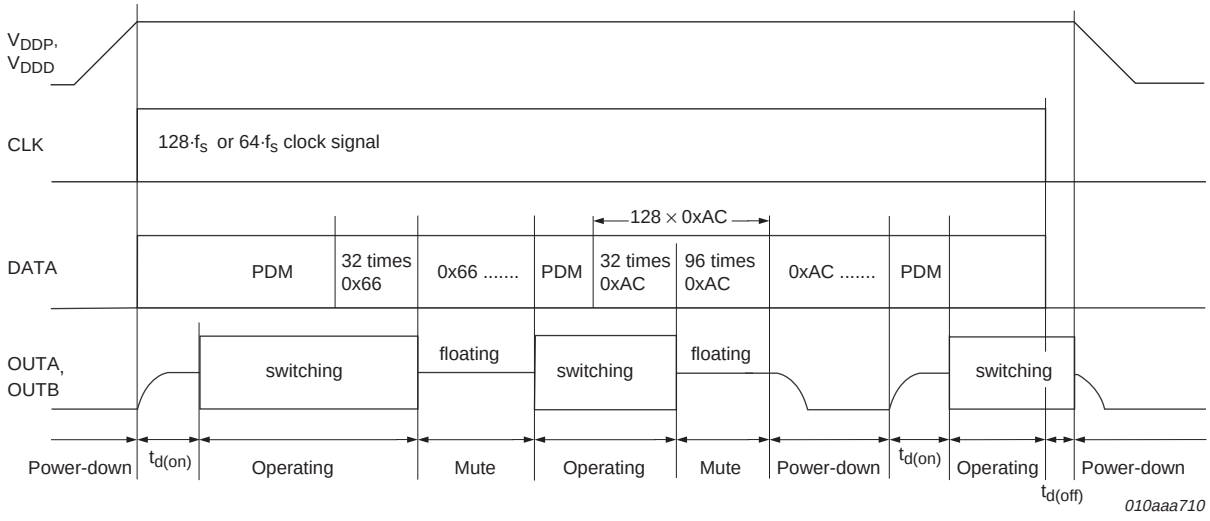


Fig 6. Power-up/power-down sequence

Table 6. Power-up/power-down timing

All parameters are guaranteed for $V_{TEST} = V_{DDP} = 3.6$ V; $V_{DDD} = 1.8$ V; $R_L = 4\ \Omega$ [1]; $L_L = 20\ \mu H$ [1]; $f_i = 1$ kHz; $f_{clk} = 6.144$ MHz; $T_{amb} = 25$ °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time		[2]	-	-	2	ms
$t_{d(off)}$	turn-off delay time		[2]	-	-	5	µs

[1] R_L = load resistance; L_L = load inductance.

[2] Inversely proportional to f_{clk}.

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8.4 Control settings

Control settings are not needed if the default values are adequate.

8.4.1 Silence pattern recognition

The TFA9881 can detect control settings on the PDM input by means of silence pattern recognition. A silence pattern has the following properties:

- All audio bytes have the same value
- Each audio byte must contain four zeros and four ones

The ten silence patterns recognized by the TFA9881 are listed in the first column of Table 7. The second column contains the related audio bytes that are generated when the silence patterns are phase shifted by 1, 2, 3, 4, 5, 6 and 7 bits.

The TFA9881 reacts as follows on receiving a silence pattern (see Table 8):

- After receiving 32 consecutive silence pattern audio bytes, the TFA9881 sets the outputs floating.
- After receiving 128 consecutive silence pattern audio bytes, the TFA9881 activates the appropriate control setting (see column three of Table 7).

Remark: Only the control settings associated with silence patterns containing audio bytes 0xD2, 0xD4, 0xD8, 0xE1, 0xE2, 0xE4 and 0xAA can be set during power-up (before the power-up delay time, $t_{d(on)}$, has expired). After power-up, only silence patterns containing bytes 0x66 and 0xAC will be recognized. All other silence patterns are ignored.

All control settings can be activated when:

- control silence patterns are transmitted after the TFA9881 has been switched to Power-down mode on receipt of a power-down silence pattern (at least 128 consecutive 0xAC bytes)
- control silence patterns are transmitted after the clock input has stopped and then started again (power-up)

If a silence pattern containing more than 128 consecutive silence pattern audio bytes is received during power-up, the TFA9881 outputs will remain floating until a different audio byte is received. It will then switch to Operating mode. Once the TFA9881 has powered up, only ‘mute’ (0x66) and ‘power-down’ (0xAC) control patterns are recognized.

All registers are reset to their default values if silence pattern 0xAA is received or the V_{DDD} supply is removed.

Table 7. Silence patterns

Byte	Related bytes[1]	Control settings
0xD1	0xE8/74/3A/1D/8E/47/A3	reserved for test purposes
0xD2	0x69/B4/5A/2D/96/4B/A5	clip control on; see Section 8.4.2
0xD4	0x6A/35/9A/4D/A6/53/A9	gain = −3 dB (V_{DDP} = 2.5 V); see Section 8.4.3
0xD8	0x6C/36/1B/8D/C6/63/B1	gain = +3 dB (V_{DDP} = 5.0 V); see Section 8.4.3
0xE1	0xF0/78/3C/1E/0F/87/C3	slope low (EMC); see Section 8.4.4
0xE2	0x71/B8/5C/2E/17/8B/C5	Dynamic Power Stage Activation (DPSA) off; see Section 8.4.5

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Table 7. Silence patterns *...continued*

Byte	Related bytes[1]	Control settings
0xE4	0x72/39/9C/4E/27/93/C9	bandwidth extension on (f_s = 32 kHz or $f_{clk} = 64f_s$); see Section 8.4.6
0xAA	0x55	defaults; no mute, reset settings to default
0x66[2]	0x33/99/CC	Mute mode (no setting); see Section 8.4.7
0xAC[2]	0x56/2B/95/CA/65/B2/59	Power-down mode; see Section 8.4.8

[1] The related bytes are the bytes from the first column phase shifted by 1, 2, 3, 4, 5, 6 and 7 bits.

[2] A silence pattern containing this byte will be recognized once the TFA9881 has powered up.

Table 8. Silence pattern recognition

Bytes 1 to 32	33 ..... 127, 128	129
	Mute mode (outputs floating)	control setting activated

8.4.2 Clip control

TFA9881 clip control is off by default. Clip control can be turned on via silence pattern 0xD2 (see Section 8.4.1). The TFA9881 clips smoothly with clip control on. Output power is at maximum with clip control off.

8.4.3 Gain selection

Signal conversion from digital audio in to PWM modulated audio out is independent of supply voltages V_{DDP} and V_{DDD}. At the default gain setting (0 dB), the audio output signal level is just below the clipping point at a supply voltage of 3.6 V at −6 dBFS (peak) input. The TFA9881 supports two further gain settings to support full output power at V_{DDP} = 2.5 V and V_{DDP} = 5.0 V. The gain settings can be selected via silence patterns 0xD4 and 0xD8 (see Section 8.4.1).

Table 9 details the corresponding peak output voltage level at −6 dBFS for the three gain settings.

Table 9. Output voltage

All parameters are guaranteed for $V_{TEST} = V_{DDP} = 3.6$ V; $V_{DDD} = 1.8$ V; $L_L = 20$ µH[1], $f_{clk} = 6.144$ MHz, $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{oM}	peak output voltage	at −6 dBFS (peak) digital input					
		gain = −3 dB, V_{DDP} = 2.5 V, R_L = 4 Ω	[1]	-	2.3	-	V
		gain = 0 dB, V_{DDP} = 3.6 V, R_L = 4 Ω; default	[1]	-	3.3	-	V
		gain = +3 dB, V_{DDP} = 5.0 V, R_L = 8 Ω, L_L = 44 µH	[1]	-	4.7	-	V

[1] R_L = load resistance; L_L = load inductance.

8.4.4 PWM slope selection

The rise and fall times of the PWM output edges can be set to one of two values, as detailed in Table 10. The default setting is 'slope normal' (10 ns with V_{DDP} = 3.6 V). 'Slope low' is selected via silence pattern 0xE1 (see Section 8.4.1). This function is implemented to reduce Electro-Magnetic Interference (EMI).

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Table 10. Slope rise and fall times

Setting	Rise and fall times of the PWM output edges
slope low	40 ns with V_{DDP} = 3.6 V
slope normal; default setting	10 ns with V_{DDP} = 3.6 V

8.4.5 Dynamic Power Stage Activation (DPSA)

The TFA9881 uses DPSA to regulate current consumption in line with the level of the incoming audio stream. This function switches off power stage sections that are not needed, reducing current consumption.

Each of the TFA9881 H-bridge power stages is divided into eight sections. The number of power stage sections activated depends on the level of the incoming audio stream. The thresholds used by the DPSA to determine how many stages are switched on are given in Table 11. The DPSA signal is used as a reference signal for switching power stage sections on and off. The DPSA signal will rise in tandem with the rectified audio input signal. When the rectified audio input signal falls, the DPSA decreases with a negative exponential function, as illustrated in Figure 7.

The DPSA function can be switched off via silence pattern 0xE2. When DPSA is off, all power stage sections are activated in Operating mode.

Table 11. DPSA input levels

Setting	Number of power stage sections active
≤ 0.035 × full scale (–29 dBFS)	1
> 0.035 × full scale (–29 dBFS)	2
> 0.07 × full scale (–23 dBFS)	4
> 0.105 × full scale (–19.5 dBFS)	8

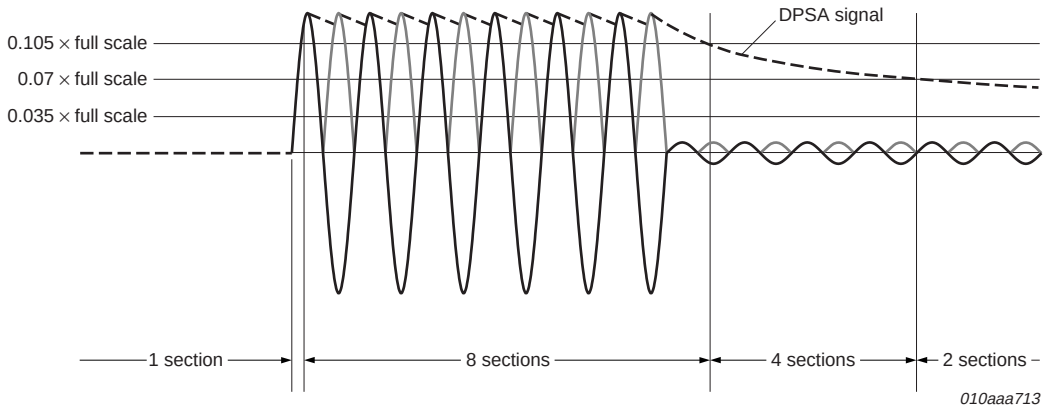


Fig 7. Dynamic Power Stage Activation

8.4.6 Bandwidth extension

The TFA9881 output spectrum has a sigma-delta converter characteristic. Figure 8 illustrates the output power spectrum of the TFA9881 when it is receiving a PDM input stream without audio content and with bandwidth extension off. The quantization noise is shaped above the band of interest. The band of interest (bandwidth) is determined by the

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corner frequency where the noise is increasing. The bandwidth in Figure 8 scales with the clock input frequency. This bandwidth can be extended via the bandwidth extension silence pattern (0xE4; see Section 8.4.1). The PWM switching frequency also scales with the bandwidth extension setting. The bandwidth and the PWM switching frequency when bandwidth extension is on and off are given in Table 12.

Remark: The Bandwidth extension should be switched off when f_{clk} > 4.1 MHz.

Table 12. Bandwidth extension setting

Setting	Bandwidth	Switching frequency
bandwidth extension on	$\frac{f_{clk}}{128}$	$\frac{f_{clk}}{8}$
bandwidth extension off; default setting	$\frac{f_{clk}}{256}$	$\frac{f_{clk}}{16}$

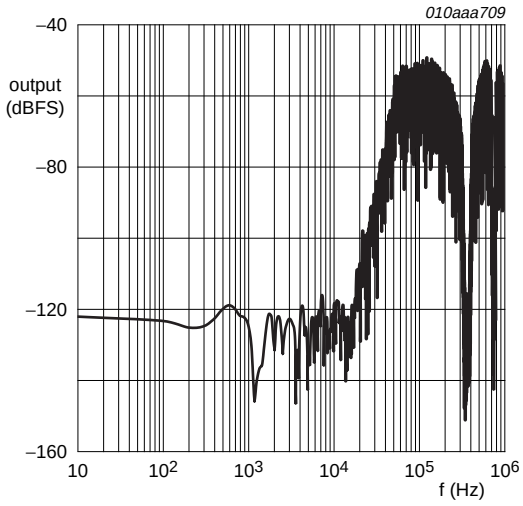


Fig 8. Output power spectrum, f_{clk} = 6.144 MHz

8.4.7 Mute

Mute mode is activated when the mute silence pattern (at least 32 consecutive 0x66 bytes) is applied on the DATA input. The TFA9881 remains in Mute mode as long as the 0x66 pattern is repeated. It will return to Operating mode when a pattern other than 0x66 is received. Transitions to and from Mute mode occur as soon as the relevant pattern is recognized by the TFA9881 (hard mute and hard unmute).

8.4.8 Power-down

Power-down mode is activated when the power-down silence pattern (at least 128 consecutive 0xAC bytes) is applied on the DATA input. The TFA9881 remains in Power-down mode as long as the 0xAC pattern is repeated. It will return to Operating mode when a pattern other than 0xAC is received.

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8.5 High-pass filter

The high-pass filter will block the DC components in the incoming audio stream. The cut-off frequency, $f_{high(-3dB)}$, is determined by the clock frequency, and is defined in Equation 1:

$$f_{high(-3dB)} = \frac{-f_{clk} \cdot ln(8191/8192)}{16 \cdot k \cdot \pi} \quad (1)$$

where k depends on the bandwidth extension setting (see Section 8.4.6):

- k = 2 if bandwidth extension is off
- k = 1 if bandwidth extension is on

$f_{high(-3dB)}$ is about 7.5 Hz at a clock frequency of 6.144 MHz when bandwidth extension is off. The high-pass filter is always enabled.

Remark: Care should be taken when DC dither is applied to the PDM audio input stream. The PDM source should slowly increase this DC-dither to avoid pop noise.

8.6 Protection mechanisms

The following protection circuits are included in the TFA9881:

- Invalid Data Protection (IDP)
- OverTemperature Protection (OTP)
- OverVoltage Protection (OVP)
- UnderVoltage Protection (UVP)
- OverCurrent Protection (OCP)

The reaction of the device to fault conditions differs depending on the protection circuit involved.

8.6.1 Invalid Data Protection (IDP)

IDP is designed to detect the absence of a data input signal. IDP is activated when 128 consecutive 0s or 1s are received on the DATA input.

IDP is disabled when a PDM stream that does not contain 128 consecutive 0s or 1s is received. The output stages are set floating when IDP is active.

Remark: The maximum PDM input modulation depth should be limited to avoid false IDP triggering.

8.6.2 OverTemperature Protection (OTP)

OTP prevents heat damage to the TFA9881. It is triggered when the junction temperature exceeds 130 °C. When this happens, the output stages are set floating. OTP is cleared automatically via an internal timer (100 ms with f_{clk} = 6.144 MHz), after which the output stages will start to operate normally again.

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8.6.3 Supply voltage protection mechanisms (UVP and OVP)

UVP is activated, setting the outputs floating, if V_{DDP} drops below the undervoltage protection threshold, $V_{P(uvp)}$. This transition will be silent, without pop noise. When the supply voltage rises above $V_{P(uvp)}$ again, the system will be restarted after 100 ms with f_{clk} = 6.144 MHz.

OVP is activated, setting the power stages floating, if the supply voltage rises above the overvoltage protection threshold, $V_{P(ovp)}$. The power stages are re-enabled as soon as the supply voltage drops below $V_{P(ovp)}$ again. The system will be restarted after 100 ms with f_{clk} = 6.144 MHz.

Note that a supply voltage > 5.5 V may damage the TFA9881.

8.6.4 OverCurrent Protection (OCP)

OCP will detect a short circuit across the load or between one of the amplifier outputs and one of the supply lines. If the output current exceeds the overcurrent protection threshold ($I_{O(ocp)}$), it will be limited to $I_{O(ocp)}$ while the amplifier outputs are switching (the amplifier is not powered down completely). This is called current limiting. The amplifier can distinguish between an impedance drop at the loudspeaker and a low-ohmic short circuit across the load or to one of the supply lines. The impedance threshold depends on which supply voltage is being used:

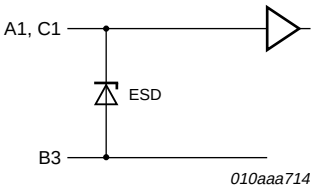
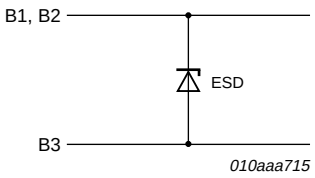
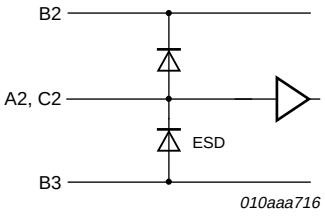
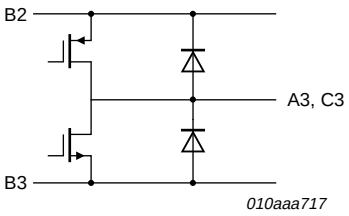
- In the event of a short circuit across the load or a short to one of the supply lines, the audio amplifier is switched off completely. It will try to restart again after approximately 100 ms with f_{clk} = 6.144 MHz. If the short-circuit condition is still present after this time, this cycle will be repeated. Average dissipation will be low because of the short duty cycle.
- In the event of an impedance drop (e.g. due to dynamic behavior of the loudspeaker), the same protection mechanism will be activated. The maximum output current is again limited to $I_{O(ocp)}$, but the amplifier will not switch off completely (thus preventing audio holes from occurring). This will result in a clipped output signal without artifacts.

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9. Internal circuitry

Table 13. Internal circuitry

Pin	Symbol	Equivalent circuit
A1	DATA	
C1	CLK	
B1	V_{DDD}	
B2	V_{DDP}	
A2	LRSEL	
C2	TEST	
A3	OUTB	
C3	OUTA	

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10. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}		–0.3	+5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}		–0.3	+1.95	V
T_j	junction temperature			-	+150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
V_x	voltage on pin x	pins CLK and DATA		–0.3	+3.6	V
		pins OUTA and OUTB		–0.6	V_{DDP} + 0.6	V
		pins TEST and LRSEL		–0.6	V_{DDP}	V
V_{ESD}	electrostatic discharge voltage	according to the Human Body Model (HBM)	[1]			
		pins OUTA and OUTB		–8	+8	kV
		any other pin		–2	+2	kV
		according to the Charge Device Model (CDM)	[1]	–500	+500	V
		according to the Machine Model (MM)	[1]	–200	+200	V

[1] Measurements taken on the TFA9881 in a HVSON10 package (engineering samples) due to handling restrictions with WLCSP9.

11. Thermal characteristics

Table 15. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; natural convection			
		JEDEC test board	[1]	128	K/W
		2-layer application board		97	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		[2]	12	K/W

[1] Measured on a JEDEC high K-factor test board (standard EIA/JESD 51-7).

[2] Value depends on where measurement is taken on package.

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12. Characteristics

12.1 DC characteristics

Table 16. DC characteristics

All parameters are guaranteed for V_{TEST} = V_{DDP} = 3.6 V; V_{DDD} = 1.8 V; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_{clk} = 6.144 MHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}	2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{DDP}	power supply current	Operating mode with load				
		-	-	1.5	1.7	mA
		f_{clk} = 2.048 MHz bandwidth extension on	-	1.38	-	mA
		Mute mode		1.1	1.2	mA
		Power-down mode	-	0.1	1	µA
I_{DDD}	digital supply current	Operating mode				
		-	-	1.35	1.5	mA
		f_{clk} = 2.048 MHz bandwidth extension on	-	0.83	-	mA
		Mute mode				
		-	-	1.25	1.4	mA
		f_{clk} = 2.048 MHz bandwidth extension on	-	0.78	-	mA
		Power-down mode CLK = 0 V, DATA = 0 V	-	2	8	µA
Series resistance output power switches						
R_{DSon}	drain-source on-state resistance	DPSA off	-	125	150	mΩ
Amplifier output pins; pins OUTA and OUTB						
$\lvert V_{O(offset)} \rvert$	output offset voltage	absolute value	-	-	3	mV
DATA, CLK and LRSEL						
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	-	3.6	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDD}$	V
C_i	input capacitance		-	-	3	pF
Protection						
$T_{act(th_prot)}$	thermal protection activation temperature		130	-	150	°C
$V_{P(ovp)}$	overvoltage protection supply voltage		5.5	-	5.9	V
$V_{P(uvp)}$	undervoltage protection supply voltage		2.3	-	2.5	V
$I_{O(ocp)}$	overcurrent protection output current		1.45	-	-	A

[1] R_L = load resistance; L_L = load inductance.

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12.2 AC characteristics

Table 17. AC characteristics

All parameters are guaranteed for $V_{TEST} = V_{DDP} = 3.6$ V; $V_{DDD} = 1.8$ V; $R_L = 4\ \Omega$[1]; $L_L = 20\ \mu H$[1]; $f_i = 1$ kHz; $f_{clk} = 6.144$ MHz; $T_{amb} = 25$ °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output power							
$P_{o(RMS)}$	RMS output power	THD + N = 1 %					
		V_{DDP} = 3.6 V, f_i = 100 Hz		-	1.4	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz		-	2.7	-	W
		THD + N = 1 %; R_L = 8 Ω; L_L = 44 µH					
		V_{DDP} = 3.6 V, f_i = 100 Hz		-	0.75	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz		-	1.45	-	W
		THD + N = 10 %					
		V_{DDP} = 3.6 V, f_i = 100 Hz		-	1.75	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz		-	3.4	-	W
		THD + N = 10 %; R_L = 8 Ω; L_L = 44 µH					
		V_{DDP} = 3.6 V, f_i = 100 Hz		-	0.95	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz		-	1.85	-	W
Performance							
η_{po}	output power efficiency	$P_{o(RMS)}$ = 1.4 W		-	90	-	%
THD+N	total harmonic distortion-plus-noise	$P_{o(RMS)}$ = 100 mW		-	0.02	0.1	%
$V_{n(o)}$	output noise voltage	A-weighted		-	24	-	µV
S/N	signal-to-noise ratio	V_{DDP} = 5 V; V_o = 3.4 V (RMS); A-weighted		-	103	-	dB
PSRR	power supply rejection ratio	V_{ripple} = 200 mV; f_{ripple} = 217 Hz		-	85	-	dB
V_{oM}	peak output voltage	At −6 dBFS (peak) digital input					
		gain = −3 dB; V_{DDP} = 3.6 V R_L = 4 Ω; L_L = 20 µH		-	2.3	-	V
		gain = 0 dB; V_{DDP} = 3.6 V R_L = 4 Ω; L_L = 20 µH		3.1	3.3	3.5	V
		gain = +3 dB; V_{DDP} = 5.0 V R_L = 8 Ω; L_L = 44 µH		-	4.7	-	V
Power-up, power-down and propagation times							
$t_{d(on)}$	turn-on delay time		[2]	-	-	2	ms
$t_{d(off)}$	turn-off delay time		[2]	-	-	5	µs
t_{PD}	propagation delay		[2]	-	-	55	µs

[1] R_L = load resistance; L_L = load inductance.

[2] Inversely proportional to f_{clk}.

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12.3 PDM timing characteristics

Table 18. PDM timing characteristics

All parameters are guaranteed for $V_{TEST} = V_{DDP} = 3.6$ V; $V_{DDD} = 1.8$ V; $R_L = 4\ \Omega$[1]; $L_L = 20\ \mu H$[1]; $f_i = 1$ kHz; $f_{clk} = 6.144$ MHz; $T_{amb} = 25$ °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency		2	-	8	MHz
δ_{clk}	clock duty cycle		40	-	60	%
t_h	hold time	after clock HIGH	7	-	-	ns
		after clock LOW	7	-	-	ns
t_{su}	set-up time	after clock HIGH	10	-	-	ns
		after clock LOW	10	-	-	ns

[1] R_L = load resistance; L_L = load inductance.

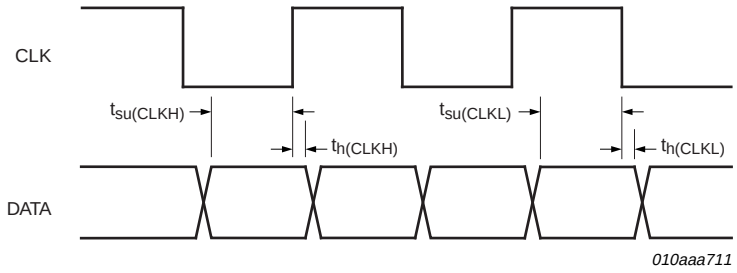


Fig 9. PDM timing

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13. Application information

13.1 ElectroMagnetic Compatibility (EMC)

EMC standards define to what degree a (sub)system is susceptible to externally imposed electromagnetic influences and to what degree a (sub)system is responsible for emitting electromagnetic signals, when in Standby mode or Operating mode.

EMC immunity and emission values are normally measured over a frequency range from 180 kHz up to 3 GHz.

13.1.1 Immunity

A major reason why amplifier devices pick up high frequency signals, and (after detection) manifest these in the device's audio band, is the presence of analog circuits inside the device or in the (sub)system.

The TFA9881 has digital inputs and digital outputs. Comparative tests on a TFA9881-based (sub)system show that the impact of externally imposed electromagnetic signals on the device is negligible in both Standby and Operating modes.

13.1.2 Emissions

Since the TFA9881 is a class-D amplifier with digitally switched outputs in a BTL configuration, it can potentially generate emissions due to the steep edges on the amplifier outputs. External components can be used to suppress these emissions. However, the TFA9881 features built-in slope control to suppress such emissions by reducing the slew rate of the BTL output signals. By reducing the slew rate, the emissions are reduced by 10 dB when compared with full-speed operation.

13.2 Supply decoupling and filtering

A ceramic decoupling capacitor of between 4.7 μF and 10 μF should be placed close to the TFA9881 for decoupling the V_{DDP} supply. This minimizes the size of the high-frequency current loop, thereby optimizing EMC performance. The TEST bump can be used to route the V_{DDP} bump connection (without using a PCB via).

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13.3 Typical application diagram (simplified)

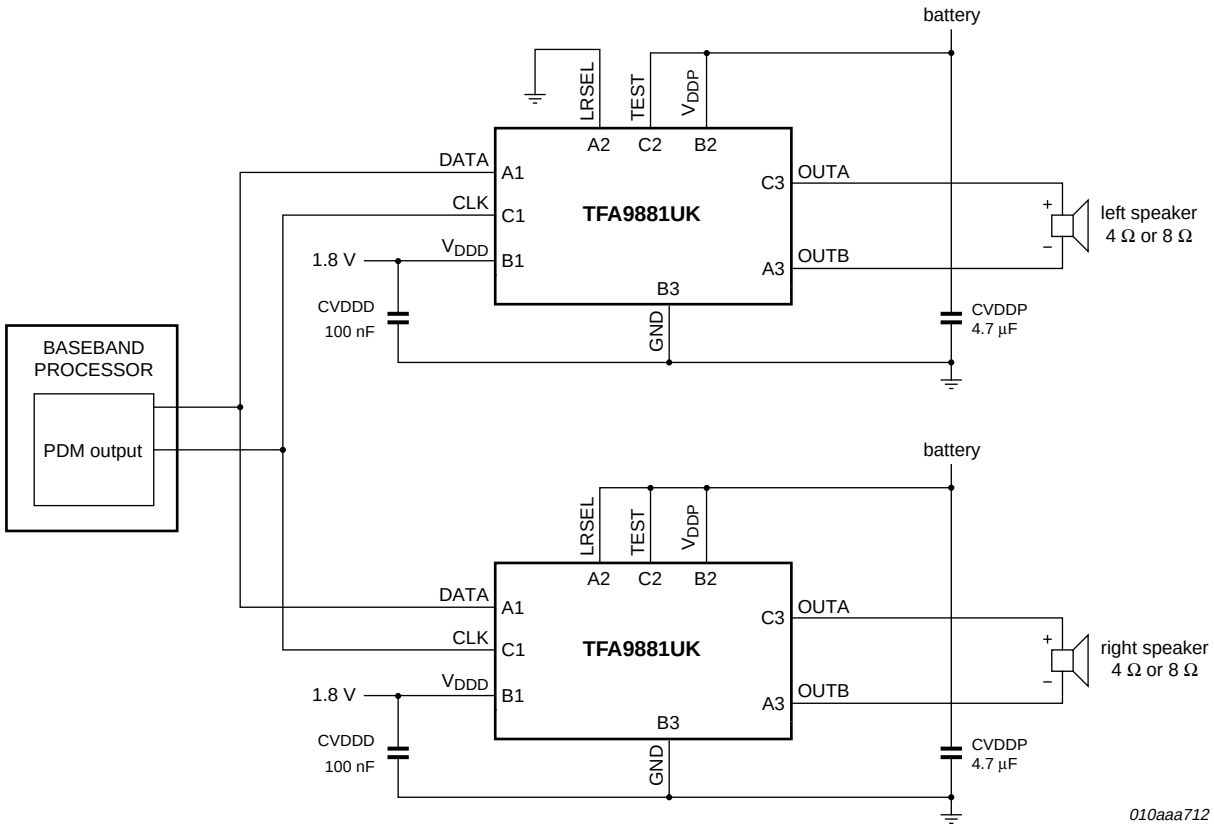


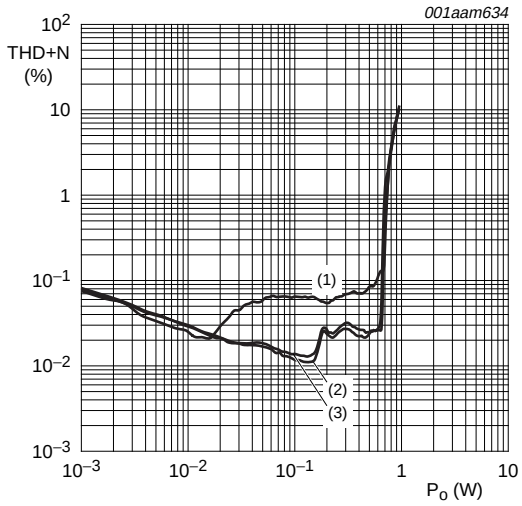
Fig 10. Typical stereo application (simplified)

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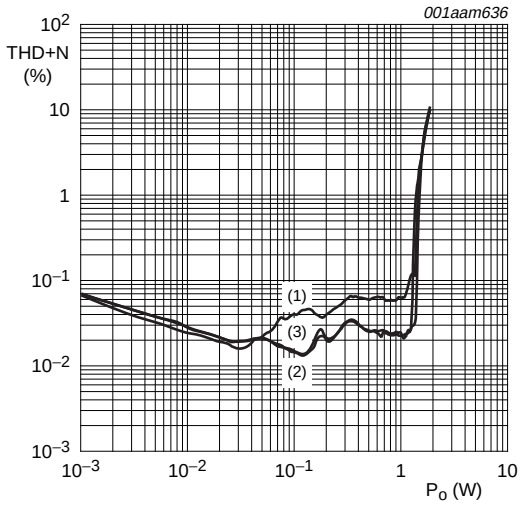
13.4 Curves measured in reference design (demonstration board)

All measurements were taken with V_{DDD} = 1.8 V, f_{clk} = 6.144 MHz, clip control off, DPSA off and slope normal, unless otherwise specified.



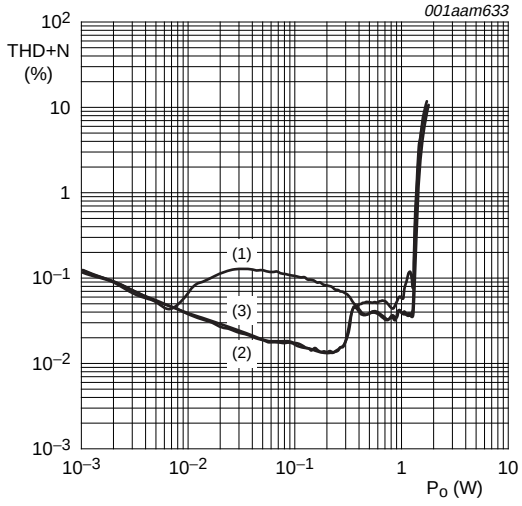
(1) f_i = 6 kHz.
(2) f_i = 1 kHz.
(3) f_i = 100 Hz.

a. V_{DDP} = 3.6 V, R_L = 8 Ω, L_L = 44 μH



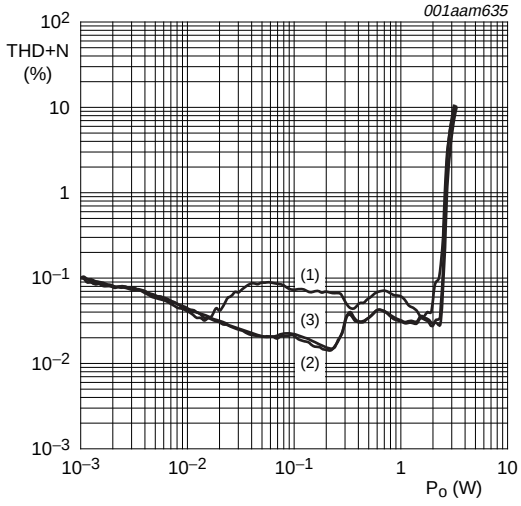
(1) f_i = 6 kHz.
(2) f_i = 1 kHz.
(3) f_i = 100 Hz.

b. V_{DDP} = 5 V, R_L = 8 Ω, L_L = 44 μH



(1) f_i = 6 kHz.
(2) f_i = 1 kHz.
(3) f_i = 100 Hz.

c. V_{DDP} = 3.6 V, R_L = 4 Ω, L_L = 20 μH



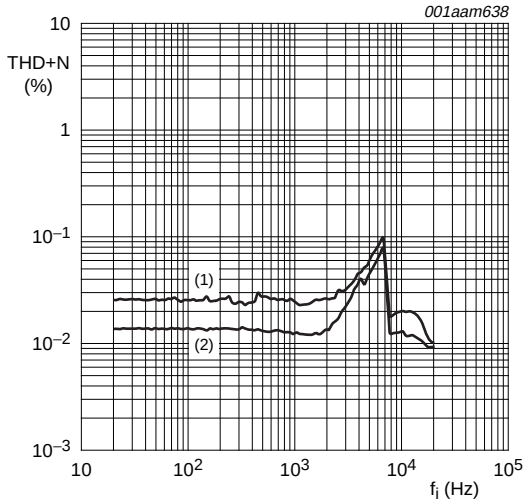
(1) f_i = 6 kHz.
(2) f_i = 1 kHz.
(3) f_i = 100 Hz.

d. V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 μH

Fig 11. THD+N as a function of output power

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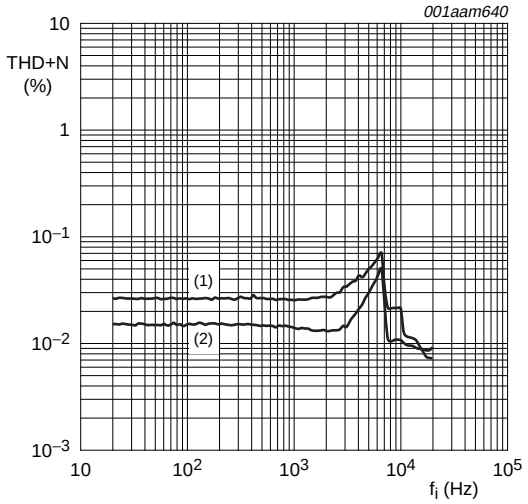
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(1) P_o = 500 mW.

(2) P_o = 100 mW.

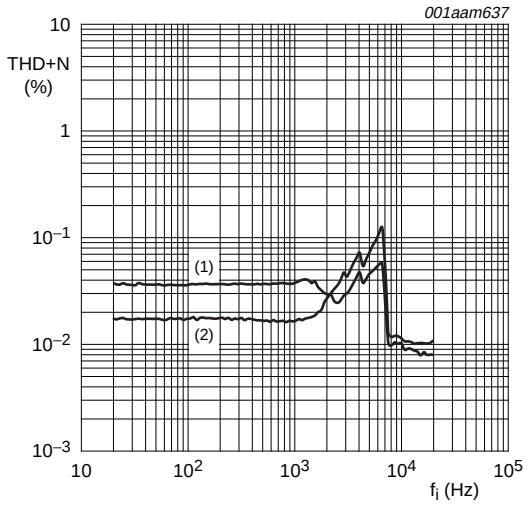
a. V_{DDP} = 3.6 V, R_L = 8 Ω, L_L = 44 μH



(1) P_o = 500 mW.

(2) P_o = 100 mW.

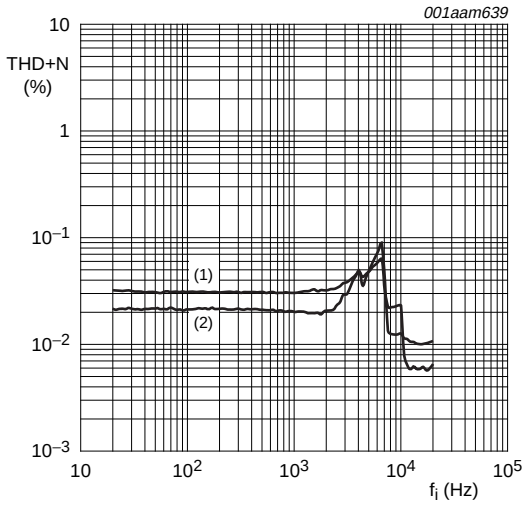
b. V_{DDP} = 5 V, R_L = 8 Ω, L_L = 44 μH



(1) P_o = 1 W.

(2) P_o = 100 mW.

c. V_{DDP} = 3.6 V, R_L = 4 Ω, L_L = 20 μH



(1) P_o = 1 W.

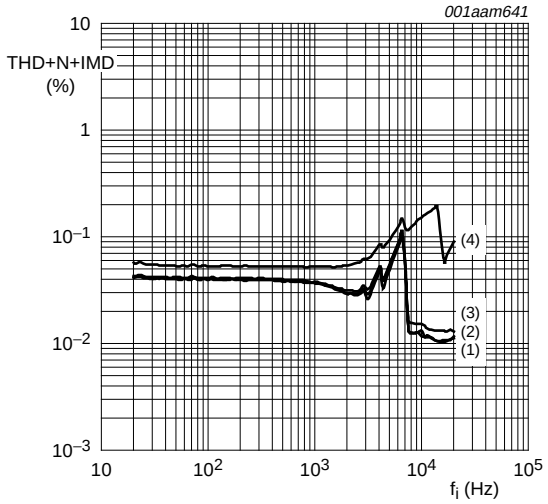
(2) P_o = 100 mW.

d. V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 μH

Fig 12. THD+N as a function of frequency

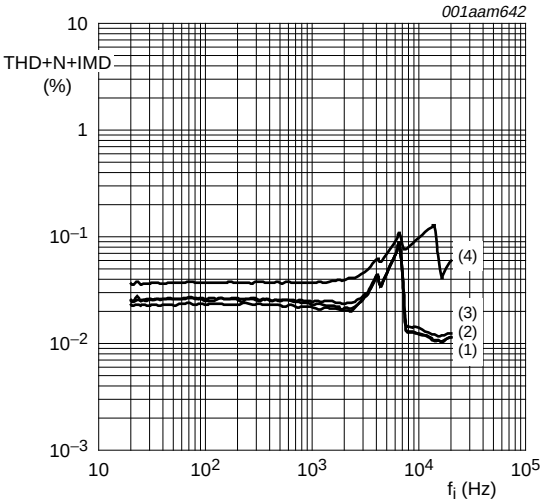
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(1) V_{ripple} = 0 V (f_{ripple} = 0 Hz).
(2) f_{ripple} = 217 Hz.
(3) f_{ripple} = 1 kHz.
(4) f_{ripple} = 6 kHz.

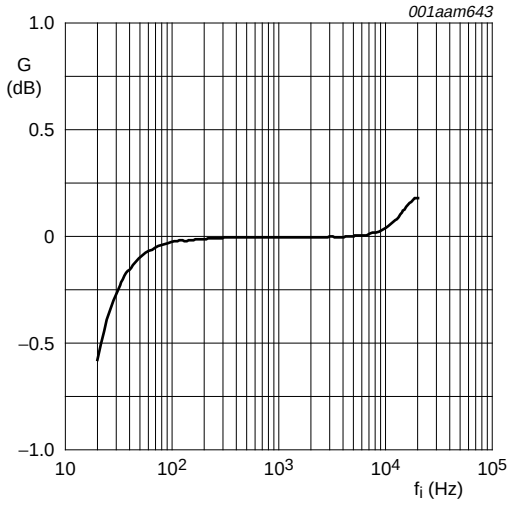
a. V_{DDP} = 3.6 V, R_L = 4 Ω, L_L = 20 μH, P_o = 100 mW
V_{ripple} = 200 mV (RMS)



(1) V_{ripple} = 0 V (f_{ripple} = 0 Hz).
(2) f_{ripple} = 217 Hz.
(3) f_{ripple} = 1 kHz.
(4) f_{ripple} = 6 kHz.

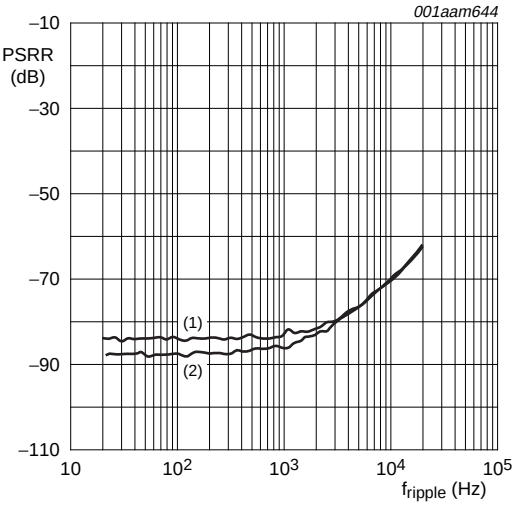
b. V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 μH, P_o = 100 mW
V_{ripple} = 200 mV (RMS)

Fig 13. THD+N + power supply intermodulation distortion as a function of frequency



V_{DDP} = 3.6 V, R_L = 4 Ω, L_L = 20 μH, P_o = 500 mW.

Fig 14. Normalized gain as a function of frequency



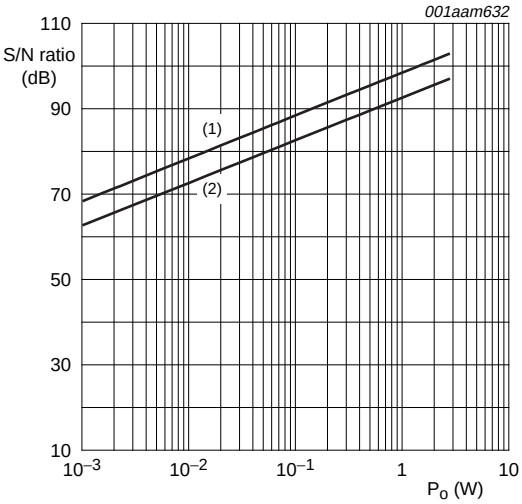
(1) V_{DDP} = 3.6 V.
(2) V_{DDP} = 5 V.

R_L = 4 Ω, L_L = 20 μH, V_{ripple} = 200 mV (RMS).

Fig 15. PSRR as a function of ripple frequency

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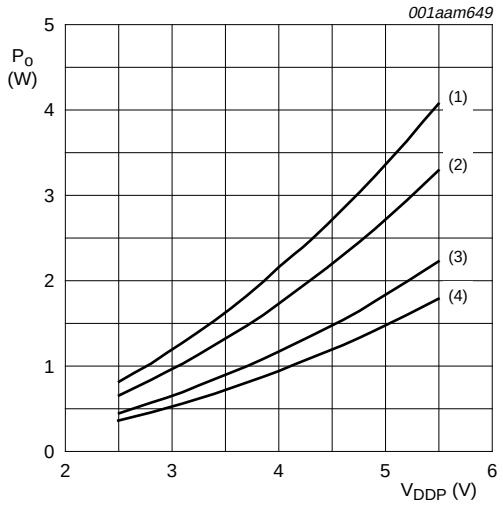


(1) A-weighted.

(2) 20 kHz brickwall filter.

V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 μH, reference signal: 3.4 V (RMS).

Fig 16. S/N ratio as a function of output power



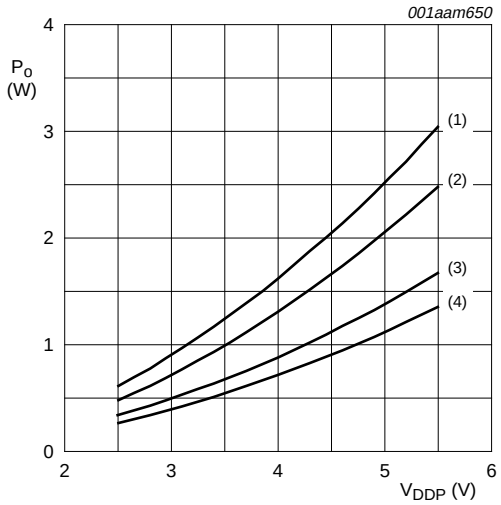
(1) THD+N = 10 %, R_L = 4 Ω, L_L = 20 μH.

(2) THD+N = 1 %, R_L = 4 Ω, L_L = 20 μH.

(3) THD+N = 10 %, R_L = 8 Ω, L_L = 44 μH.

(4) THD+N = 1 %, R_L = 8 Ω, L_L = 44 μH.

a. f_i = 100 Hz, clip control off



(1) THD+N = 10 %, R_L = 4 Ω, L_L = 20 μH.

(2) THD+N = 1 %, R_L = 4 Ω, L_L = 20 μH.

(3) THD+N = 10 %, R_L = 8 Ω, L_L = 44 μH.

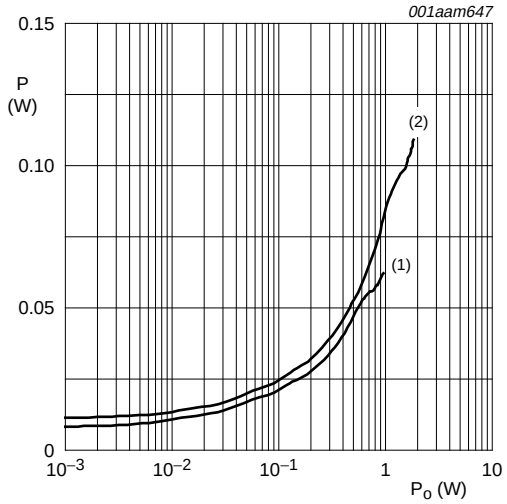
(4) THD+N = 1 %, R_L = 8 Ω, L_L = 44 μH.

b. f_i = 100 Hz, clip control on

Fig 17. Output power as a function of supply voltage

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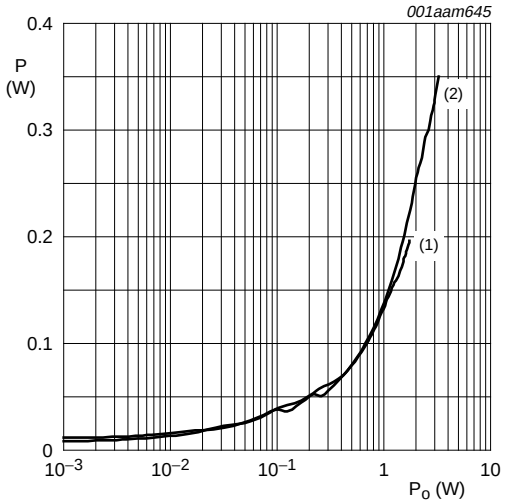
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(1) V_{DDP} = 3.6 V.

(2) V_{DDP} = 5 V.

a. R_L = 8 Ω, L_L = 44 μH, f_i = 1 kHz, DPSA on

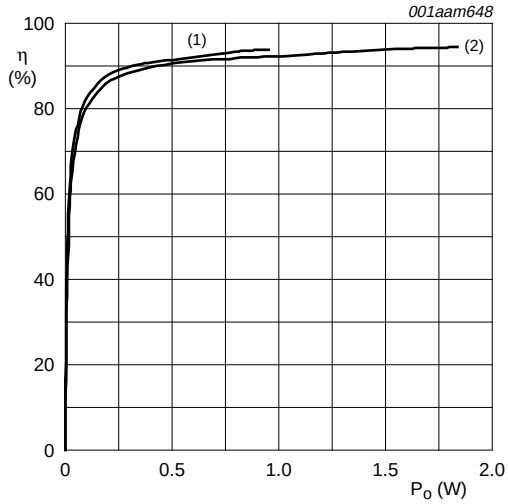


(1) V_{DDP} = 3.6 V.

(2) V_{DDP} = 5 V.

b. R_L = 4 Ω, L_L = 20 μH, f_i = 1 kHz, DPSA on

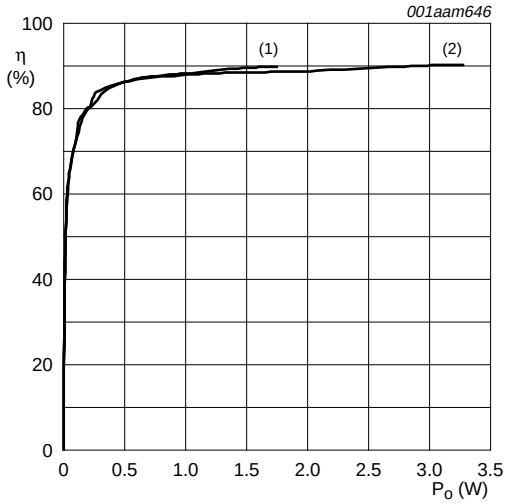
Fig 18. Power dissipation as a function of output power



(1) V_{DDP} = 3.6 V.

(2) V_{DDP} = 5 V.

a. R_L = 8 Ω, L_L = 44 μH, f_i = 1 kHz, DPSA on



(1) V_{DDP} = 3.6 V.

(2) V_{DDP} = 5 V.

b. R_L = 4 Ω, L_L = 20 μH, f_i = 1 kHz, DPSA on

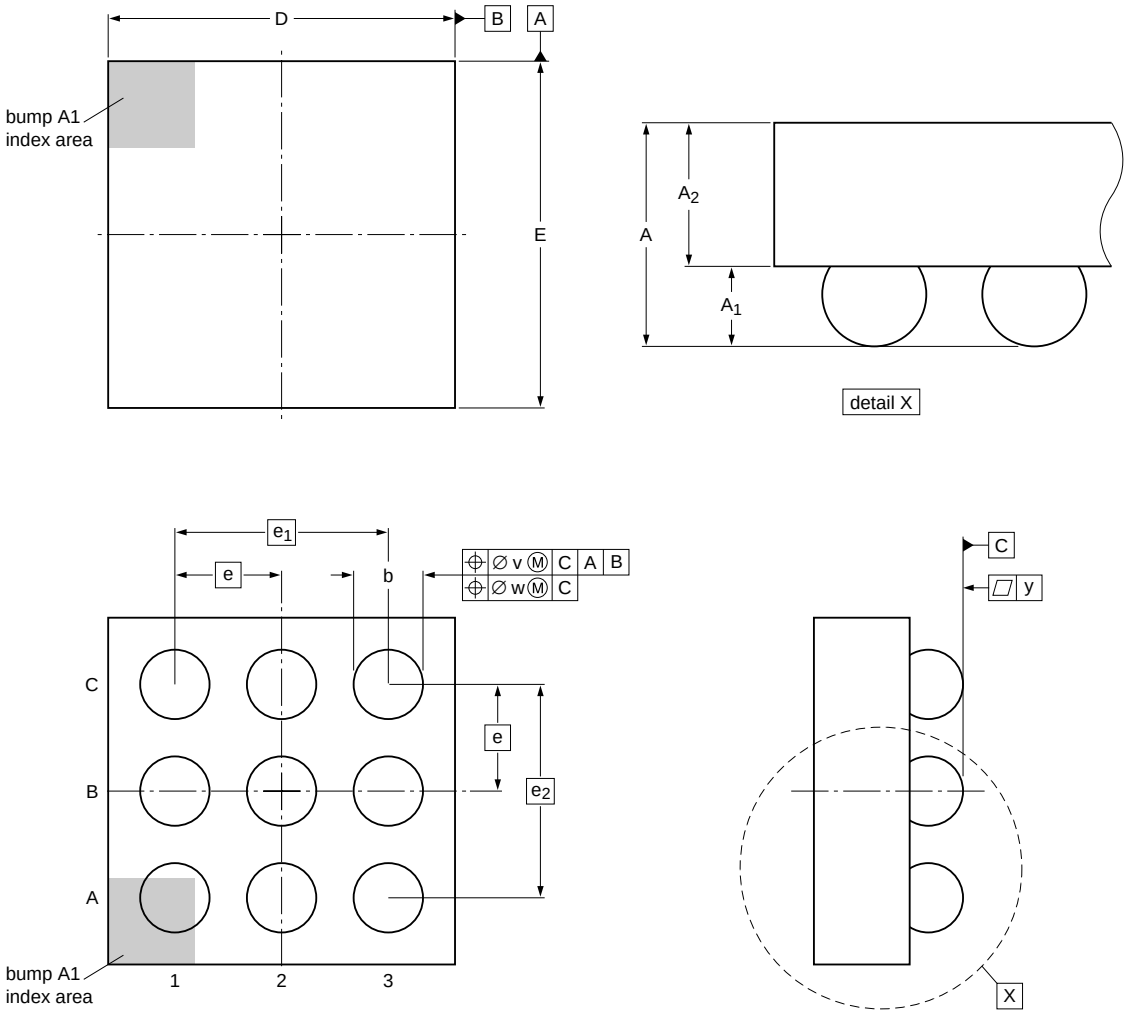
Fig 19. Efficiency as a function of output power

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14. Package outline

WLCSP9: wafer level chip-size package; 9 bumps; 1.3 x 1.3 x 0.6 mm **TFA9881UK**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.6	0.22	0.38	0.28	1.3	1.3						
	nom							0.4	0.8	0.8	0.01	0.04	0.02
	min		0.18	0.34	0.24	1.2	1.2						

tfa9881uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
TFA9881UK						~~10-10-06~~ 10-12-16

Fig 20. Package outline TFA9881UK (WLCSP9)

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15. Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19.

Table 19. Lead-free process (from J-STD-020C)

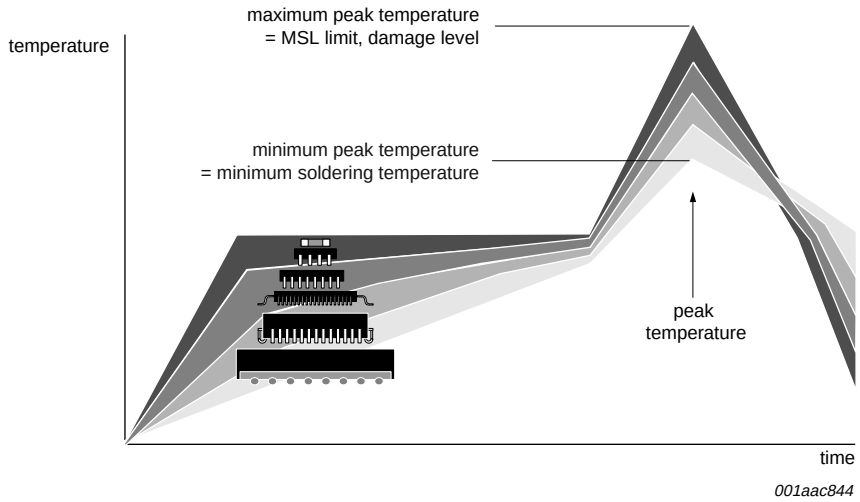
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.

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MSL: Moisture Sensitivity Level

Fig 21. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

15.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

15.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

15.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

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Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

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16. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9881 v.1	20110105	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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