HARRIS Semiconductor

RFM7N35, RFM7N40, RFP7N35, RFP7N40

7A, 350V and 400V, 0.75 Ohm, N-Channel Power MOSFETs

July 1998

Features

- **7A, 350V and 400V**
- **$r_{DS(ON)}$ = 0.75Ω**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Majority Carrier Device**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFM7N35	TO-204AA	RFM7N35
RFM7N40	TO-204AA	RFM7N40
RFP7N35	TO-220AB	RFP7N35
RFP7N40	TO-220AB	RFP7N40

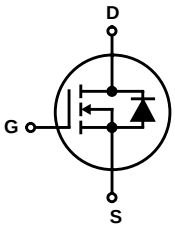
NOTE: When ordering, use the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

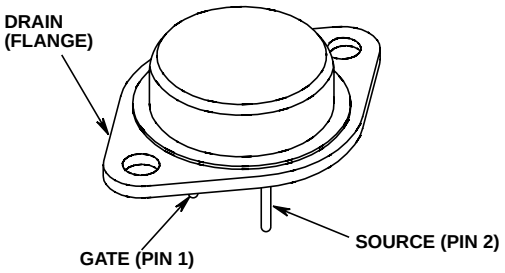
Formerly developmental type TA17424.

Symbol

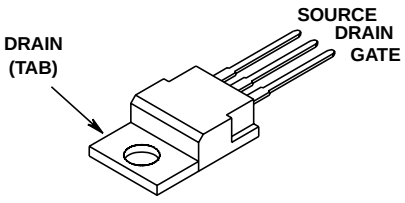


Packaging

JEDEC TO-204AA



JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **1536.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFM7N35	RFM7N40	RFP7N35	RFP7N40	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	350	400	350	400	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1)	V_{DGR}	350	400	350	400	V
Continuous Drain Current	I_D	7	7	7	7	A
Pulsed Drain Current (Note 3)	I_{DM}	15	15	15	15	A
Gate to Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation	P_D	100	100	75	75	W
Linear Derating Factor (Above 25^oC)		0.8	0.8	0.6	0.6	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering						
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	300	300	^oC
Package Body for 10s, See Techbrief 334 (for TO-220)	T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V				
RFM7N35, RFP7N35			350	-	-	V
RFM7N40, RFP7N40			400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $T_C = 25^oC$	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, $T_C = 125^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 7A, V_{GS} = 10V (Figures 6, 7)	-	-	0.75	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 7A, V_{GS} = 10V	-	-	5.25	V
Turn-On Delay Time	$t_{d(ON)}$	V_{DS} = 200V, $I_D \approx$ 3.5A, R_G = 50Ω, R_L = 56Ω, V_{GS} = 10V (Figures 10, 11, 12)	-	16	45	ns
Rise Time	t_r		-	54	75	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	170	250	ns
Fall Time	t_f		-	62	100	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 9)	-	-	1600	pF
Output Capacitance	C_{OSS}		-	-	300	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	200	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFM7N35, RFM7N40	-	-	1.25	$^oC/W$
		RFP7N35, RFP7N40	-	-	1.67	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 7A	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_{SD} = 7A, dI_{SD}/dt = 100A/μs	-	870	-	ns

NOTES:

2. Pulse Test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

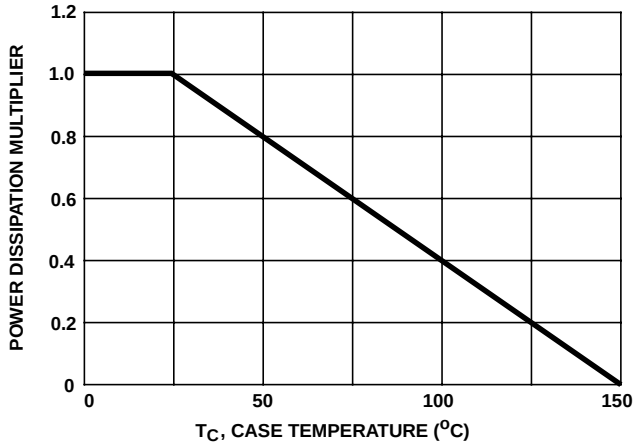


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

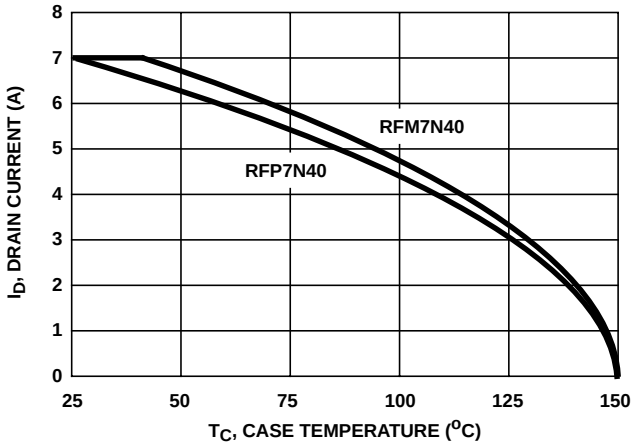


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

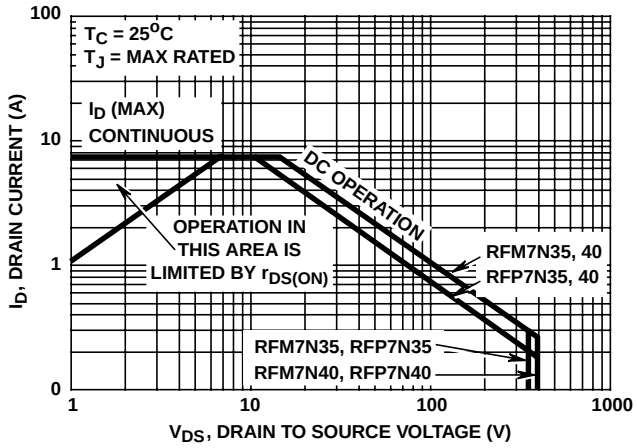


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

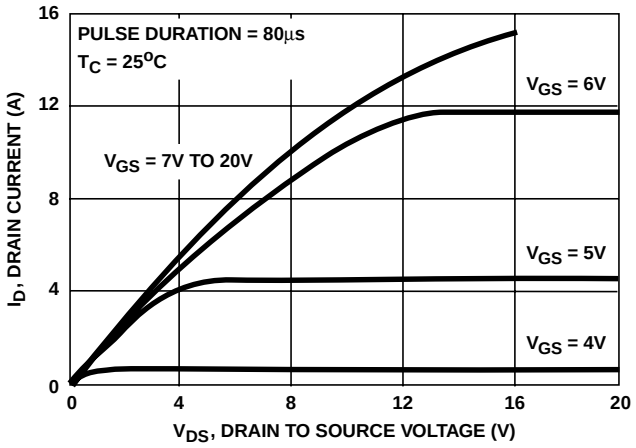


FIGURE 4. SATURATION CHARACTERISTICS

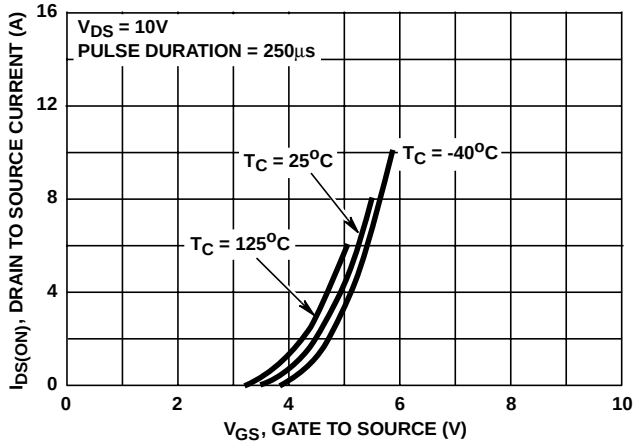


FIGURE 5. TRANSFER CHARACTERISTICS

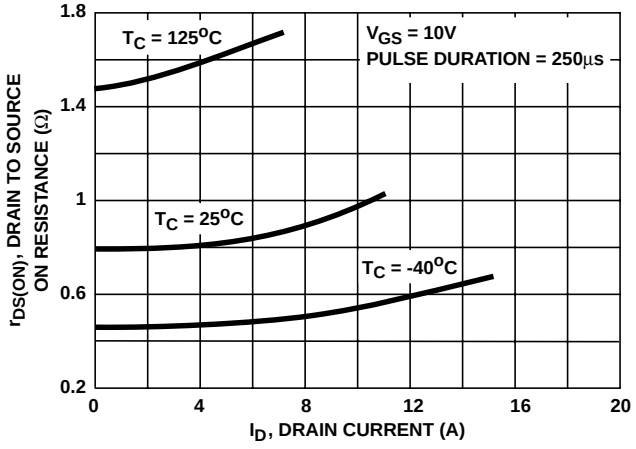


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

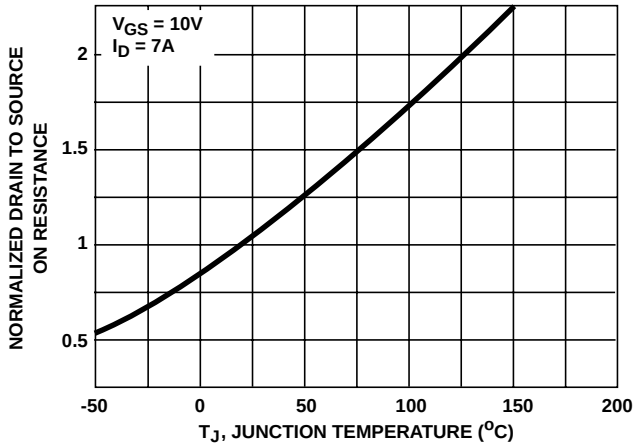


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

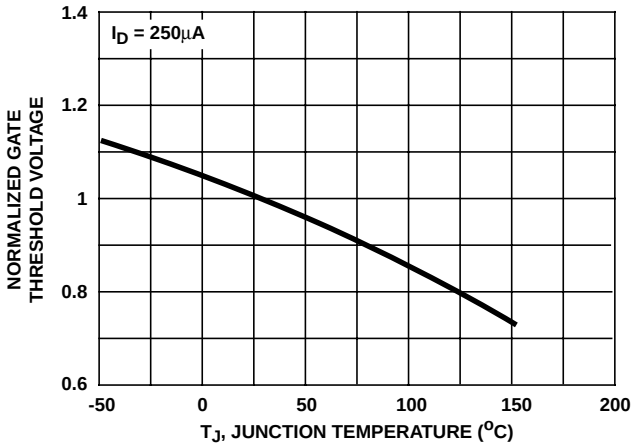


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

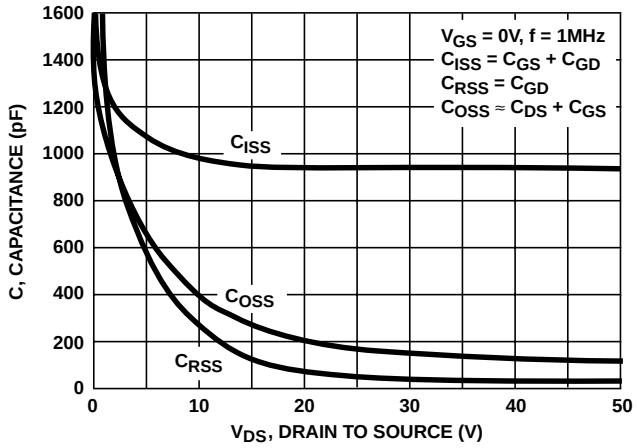
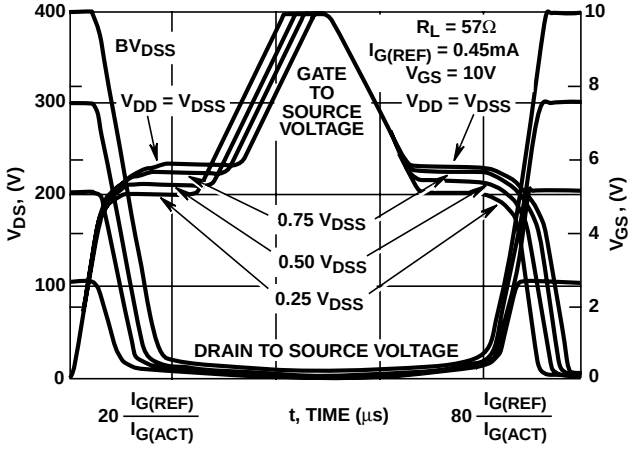


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

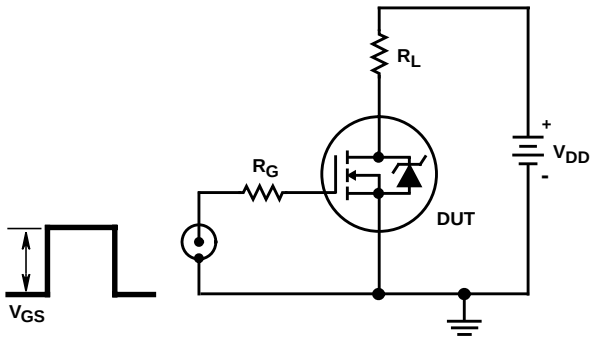


FIGURE 11. SWITCHING TIME TEST CIRCUIT

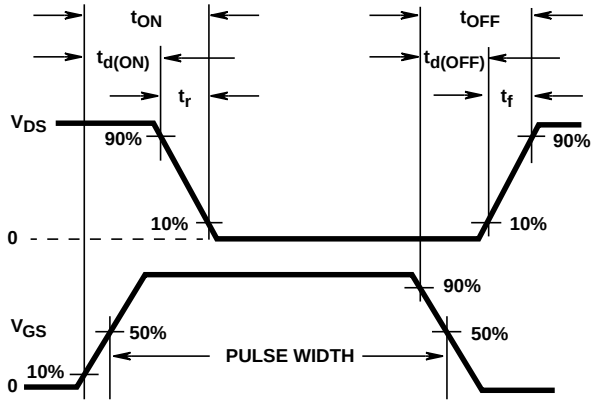


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS