Features

- **Programmable 4,194,304 x 1 and 8,388,608 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **3.3V Output Capability**
- **5V Tolerant I/O Pins**
- **Program Support using the Atmel ATDH2200E System or Industry Third Party Programmers**
- **In-System Programmable (ISP) via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT40K and AT94K Devices, Altera® FLEX®, Excalibur™, Stratix®, Cyclone™ and APEX™ Devices**
- **Cascadable Read-back to Support Additional Configurations or Higher-density Arrays**
- **Low-power CMOS FLASH Process**
- **Available in 8-lead LAP, 20-lead PLCC and 32-lead TQFP Packages**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Low-power Standby Mode**
- **Single Device Capable of Holding 4 Bit Stream Files Allowing Simple System Reconfiguration**
- **Fast Serial Download Speeds up to 33 MHz**
- **Endurance: 5,000 Write Cycles Typical**
- **Green (Lead/Halide-free/ROHS compliant) Packages**

FPGA Configuration Flash Memory

AT17F040A
AT17F080A

1. Description

The AT17FxxxA Series of In-System Programmable Configuration PROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17FxxxA Series device is packaged in the 8-lead LAP, 20-lead PLCC and 32-lead TQFP, see Table 1-1. The AT17FxxxA Series Configurator uses a simple serial-access procedure to configure one or more FPGA devices.

The AT17FxxxA Series Configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

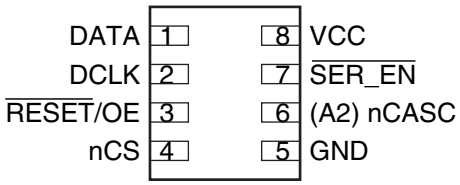
Table 1-1. AT17FxxxA Series Packages

Package	AT17F040A	AT17F080A
8-lead LAP	Yes	Yes
20-lead PLCC	Yes	Yes
32-lead TQFP	Yes	Yes

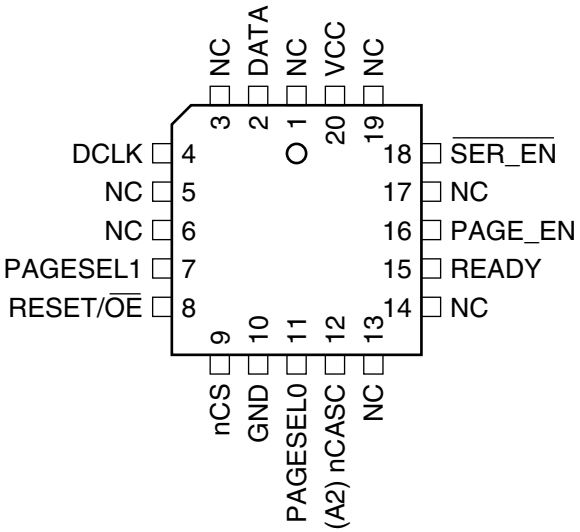
2823D–CNFG–2/08

2. Pin Configuration

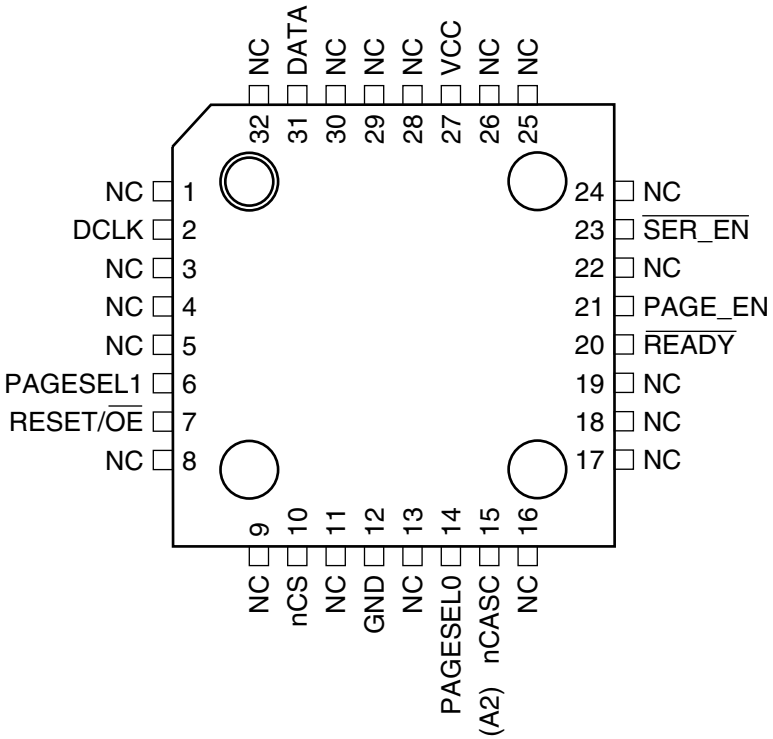
8-lead LAP



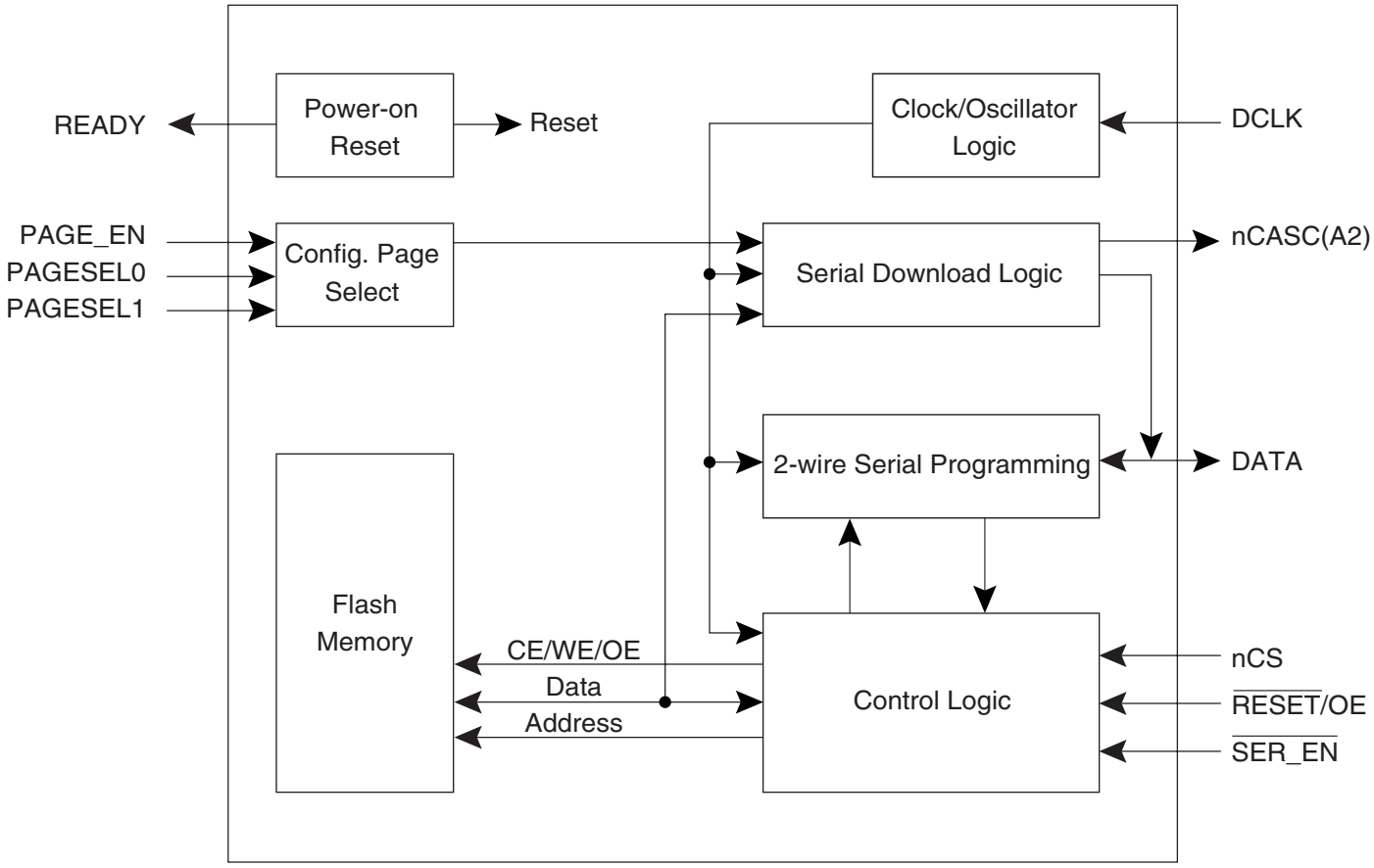
20-lead PLCC



32-lead TQFP



3. Block Diagram



4. Device Description

The control signals for the configuration memory device (nCS, $\overline{\text{RESET}}$/OE and DCLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration device without requiring an external intelligent controller.

The $\overline{\text{RESET}}$/OE and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter. When $\overline{\text{RESET}}$/OE is driven Low, the configuration device resets its address counter and tri-states its DATA pin. The nCS pin also controls the output of the AT17FxxxA Series Configurator. If nCS is held High after the $\overline{\text{RESET}}$/OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When OE is subsequently driven High, the counter and the DATA output pin are enabled. When $\overline{\text{RESET}}$/OE is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of nCS.

When the configurator has driven out all of its data and nCASC is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

5. Pin Description

Table 5-1. Pin Description

Name	I/O	AT17F040A/080A	
		20 PLCC	32 TQFP
DATA	I/O	2	31
DCLK	I	4	2
PAGE_EN	I	16	21
PAGESEL0	I	11	14
PAGESEL1	I	7	6
$\overline{\text{RESET}}$/OE	I	8	7
nCS	I	9	10
GND	–	10	12
nCASC	O	12	15
A2	I		
READY	O	15	20
$\overline{\text{SER_EN}}$	I	18	23
V_{CC}	–	20	27

5.1 DATA[1]

Three-state DATA output for FPGA configuration. Open-collector bi-directional pin for configuration programming.

5.2 DCLK[1]

Three-state clock. Functions as an input when the Configurator is in programming mode (i.e. SER_EN is Low) and as an output during FPGA configuration.

5.3 PAGE_EN[2]

Input used to enable page download mode. When PAGE_EN is high the configuration download address space is partitioned into 4 equal pages. This gives users the ability to easily store and retrieve multiple configuration bitstreams from a single configuration device. This input works in conjunction with the PAGESEL inputs. PAGE_EN must be remain low if paging is not desired. When SER_EN is Low (ISP mode) this pin has no effect.

Notes: 1. This pin has an internal 20 kΩ pull-up resistor.
2. This pin has an internal 30 kΩ pull-down resistor.

5.4 PAGESEL[1:0](2)

Page select inputs. Used to determine which of the 4 memory pages are targeted during a serial configuration download. The address space for each of the pages is shown in Table 5-2. When $\overline{\text{SER_EN}}$ is Low (ISP mode) these pins have no effect.

Table 5-2. Address Space

Paging Decodes	AT17F040A (4 Mbits)	AT17F080A (8 Mbits)
PAGESEL = 00, PAGE_EN = 1	00000 – 0FFFFh	00000 – 1FFFFh
PAGESEL = 01, PAGE_EN = 1	10000 – 1FFFFh	20000 – 3FFFFh
PAGESEL = 10, PAGE_EN = 1	20000 – 2FFFFh	40000 – 5FFFFh
PAGESEL = 11, PAGE_EN = 1	30000 – 3FFFFh	60000 – 7FFFFh
PAGESEL = XX, PAGE_EN = 0	00000 – 3FFFFh	00000 – 7FFFFh

5.5 $\overline{\text{RESET}}$/OE(1)

Output Enable (active High) and RESET (active Low) when $\overline{\text{SER_EN}}$ is High. A Low level on $\overline{\text{RESET}}$/OE resets both the address and bit counters. A High level (with nCS Low) enables the data output driver.

5.6 nCS(1)

Chip Enable input (active Low). A Low level (with OE High) allows DCLK to increment the address counter and enables the data output driver. A High level on nCS disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the 2-wire Serial Programming mode ($\overline{\text{SER_EN}}$ Low).

5.7 GND

Ground pin. A 0.2 µF decoupling capacitor between V_{CC} and GND is recommended.

5.8 nCASC

Cascade Select Output (when $\overline{\text{SER_EN}}$ is High). This output goes Low when the internal address counter has reached its maximum value. If the PAGE_EN input is set High, the maximum value is the highest address in the selected partition. The PAGESEL[1:0] inputs are used to make the 4 partition selections. If the PAGE_EN input is set Low, the device is not partitioned and the address maximum value is the highest address in the device, see Table 5-2 on page 5. In a daisy chain of AT17FxxxA Series devices, the nCASC pin of one device must be connected to the nCS input of the next device in the chain. It will stay Low as long as nCS is Low and OE is High. It will then follow nCS until OE goes Low; thereafter, nCASC will stay High until the entire EEPROM is read again.

5.9 A2(1)

Device selection input, (when $\overline{\text{SER_EN}}$ Low). The input is used to enable (or chip select) the device during programming (i.e., when $\overline{\text{SER_EN}}$ is Low). Refer to the AT17FxxxA Programming Specification available on the Atmel web site for additional details.

Notes: 1. This pin has an internal 20 k pull-up resistor.
2. This pin has an internal 30 kΩ pull-down resistor.

5.10 READY

Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (recommended 4.7 kΩ pull-up on this pin if used).

5.11 $\overline{\text{SER_EN}}$[1]

The serial enable input must remain High during FPGA configuration operations. Bringing $\overline{\text{SER_EN}}$ Low enables the 2-Wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER_EN}}$ should be tied to V_{CC}.

5.12 V_{CC}

+3.3V (±10%).

Notes: 1. This pin has an internal 20 kΩ pull-up resistor.

6. FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17FxxxA Serial Configuration PROM has been designed for compatibility with the Master Serial mode.

This document discusses the Atmel AT40K, AT40KAL and AT94KAL applications as well as Altera applications.

7. Control of Configuration

Most connections between the FPGA device and the AT17FxxxA Serial Configurator PROM are simple and self-explanatory.

- The DATA output of the AT17FxxxA Series Configurator drives DIN of the FPGA devices.
- The DCLK output of the AT17FxxxA device drives the DCLK input data of the FPGA.
- The nCASC output of a AT17FxxxA Series Configurator drives the nCS input of the next Configurator in a cascade chain of configurator devices.
- $\overline{\text{SER_EN}}$ must be at logic High level (internal pull-up resistor provided) except during ISP.
- The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.
- PAGE_EN must REMAIN Low if download paging is not desired. If paging is desired, PAGE_EN must be High and the PAGESEL pins must be set to High or Low such that the desired page is selected, see Table 5-2 on page 5.

8. Cascading Serial Configuration Devices

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the clock signal to the configurator asserts its nCASC output Low and disables its DATA line driver. The second configurator recognizes the Low level on its nCS input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the $\overline{\text{RESET}}$/OE on each configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the $\overline{\text{RESET}}$/OE input can be tied to its inactive (High) level.

9. Programming Mode

The programming mode is entered by bringing $\overline{\text{SER_EN}}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. The AT17FxxxA parts are read/write at 3.3V nominal. Refer to the AT17FxxxA Programming Specification available on the Atmel web site (www.atmel.com) for more programming details. AT17FxxxA devices are supported by the Atmel ATDH2200 programming system along with many third party programmers.

10. Standby Mode

The AT17FxxxA Series Configurators enter a low-power standby mode whenever $\overline{\text{SER_EN}}$ is High and nCS is asserted High. In this mode, the AT17FxxxA Configurator typically consumes less than 1 mA of current at 3.3V. The output remains in a high-impedance state regardless of the state of the OE input.

11. Absolute Maximum Ratings*

Operating Temperature	-40° C to +85° C
Storage Temperature	-65° C to +150° C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +4.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260° C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

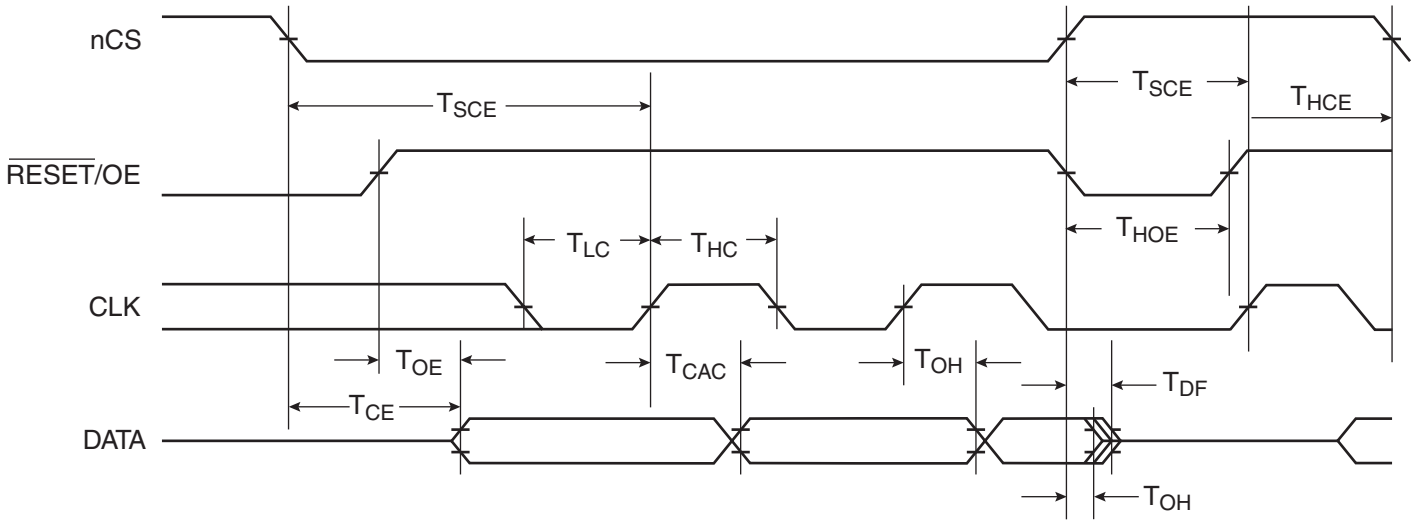
12. Operating Conditions

Symbol	Description		AT17FxxxA Series Configurator Min	AT17FxxxA Series Configurator Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0° C to +70° C	2.97	3.63	V
	Industrial	Supply voltage relative to GND -40° C to +85° C	2.97	3.63	V

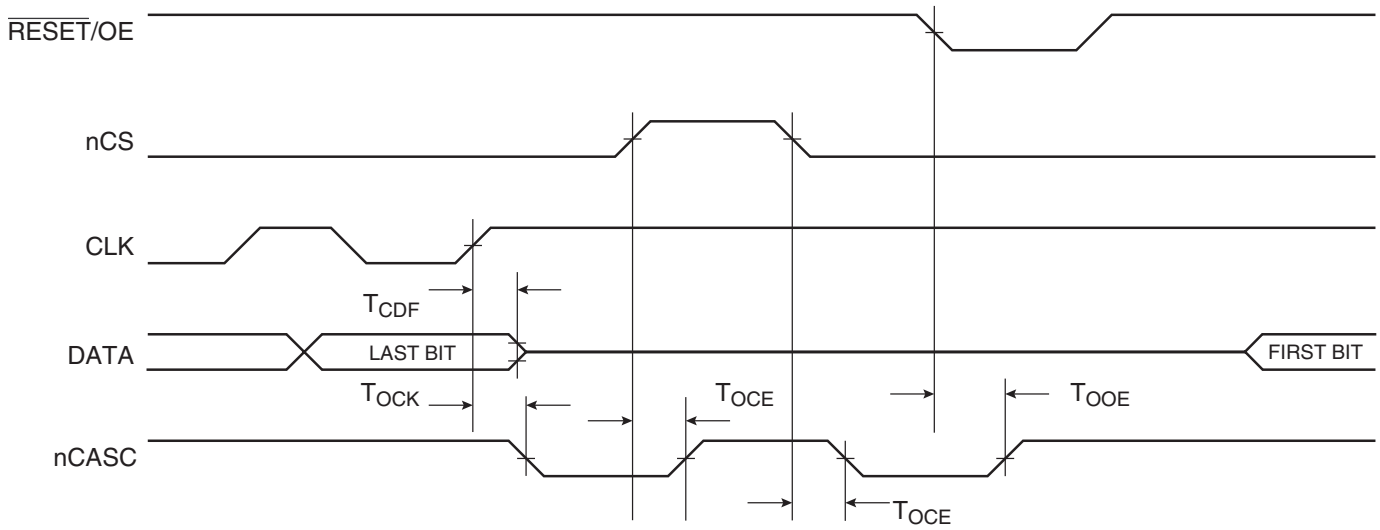
13. DC Characteristics

Symbol	Description		AT17F040A Min	AT17F040A Max	AT17F080A Min	AT17F080A Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)	Commercial		0.4		0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)	Industrial		0.4		0.4	V
I_{CCA}	Supply Current, Active Mode at Freq. Max.			50		50	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		3		3	mA
		Industrial		3		3	mA

14. AC Characteristics



15. AC Characteristics when Cascading



16. AC Characteristics

Symbol	Description		AT17F040A/080A			Units
			Min	Typ	Max	
T_{OE}[2]	OE to Data Delay	Commercial			50	ns
		Industrial[1]			55	ns
T_{CE}[2]	nCS to Data Delay	Commercial			55	ns
		Industrial[1]			60	ns
T_{CAC}[2]	DCLK to Data Delay	Commercial			30	ns
		Industrial[1]			30	ns
T_{OH}	Data Hold from nCS, OE, or DCLK	Commercial	0			ns
		Industrial[1]	0			ns
T_{DF}[3]	nCS or OE to Data Float Delay	Commercial			15	ns
		Industrial[1]			15	ns
T_{LC}	DCLK Low Time	Commercial	15			ns
		Industrial[1]	15			ns
T_{HC}	DCLK High Time	Commercial	15			ns
		Industrial[1]	15			ns
T_{SCE}	nCS Setup Time to DCLK (to guarantee proper counting)	Commercial	20			ns
		Industrial[1]	25			ns
T_{HCE}	nCS Hold Time from DCLK (to guarantee proper counting)	Commercial	0			ns
		Industrial[1]	0			ns
T_{HOE}	$\overline{\text{RESET}}$/OE Low Time (guarantees counter is reset)	Commercial	20			ns
		Industrial[1]	20			ns
F_{MAX}	Maximum Input Clock Frequency $\overline{\text{SEREN}}$ = 0	Commercial			10	MHz
		Industrial[1]			10	MHz
T_{WR}	Write Cycle Time[4]	Commercial		12		µs
		Industrial[1]		12		µs
T_{EC}	Erase Cycle Time[4]	Commercial		13		s
		Industrial[1]		13		s

Notes:
1. Preliminary specifications for military operating range only.
2. AC test lead = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.
4. See the AT17FxxxA Programming Specfication for procedural information.

16.1 AC Characteristics When Cascading

Symbol	Description		AT17F040A		AT17F080A		Units
			Min	Max	Min	Max	
T_{CDF}[3]	DCLK to Data Float Delay	Commercial		50		50	ns
		Industrial		50		50	ns
T_{OCK}[2]	DCLK to nCASC Delay	Commercial		50		50	ns
		Industrial		55		55	ns
T_{OCE}[2]	$\overline{nCS}$ to nCASC Delay	Commercial		35		35	ns
		Industrial		40		40	ns
T_{OOE}[2]	$\overline{RESET}$/OE to nCASC Delay	Commercial		35		35	ns
		Industrial		25		35	ns

Notes: 1. AC test lead = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

17. Thermal Resistance Coefficients

Package Type			AT17F040A	AT17F080A
20J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]		–
		θ_{JA} [°C/W][1]		–
32A	Thin Plastic Quad Flat Package (TQFP)	θ_{JC} [°C/W]	17	17
		θ_{JA} [°C/W][1]	62	62

Note: 1. Airflow = 0 ft/min.

18. Ordering Information

Memory Size	Ordering Code	Package[1]	Operation Range
4-Mbit	AT17F040A-30QC	32A - 32 TQFP	Commercial (0° C to 70° C)
	AT17F040A-30QI	32A - 32 TQFP	Industrial (-40° C to 85° C)
8-Mbit	AT17F080A-30QC	32A - 32 TQFP	Commercial (0° C to 70° C)
	AT17F080A-30QI	32A - 32 TQFP	Industrial (-40° C to 85° C)

Notes: 1. For the -30JC and -30JI package, customers may migrate to the AT17FxxxA-30JU.

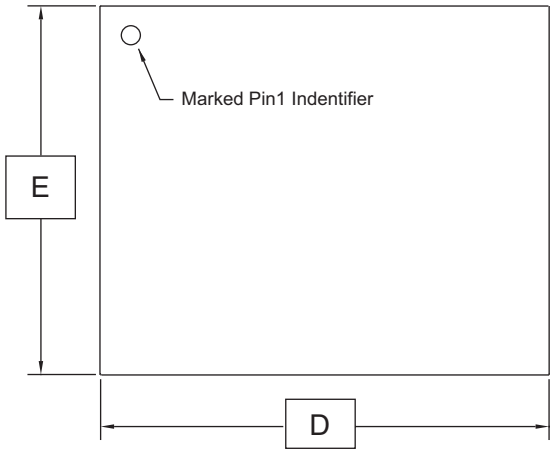
19. Green Package Options (Pb/Halide-free/RoHS Compliant)

Memory Size	Ordering Code	Package	Operation Range
4-Mbit	AT17F040A-30CU AT17F040A-30JU	8CN4 -8 LAP 20J - 20 PLCC	Industrial (-40° C to 85° C
8-Mbit	AT17F080A-30CU AT17F080A-30JU	8CN4 -8 LAP 20J - 20 PLCC	

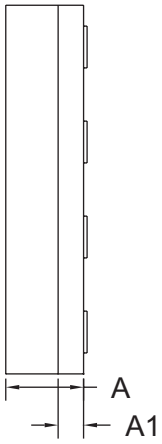
Package Type	
8CN4	8-lead, 6 mm x 6 mm x 1.04 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOIC Packages
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP)

20. Packaging Information

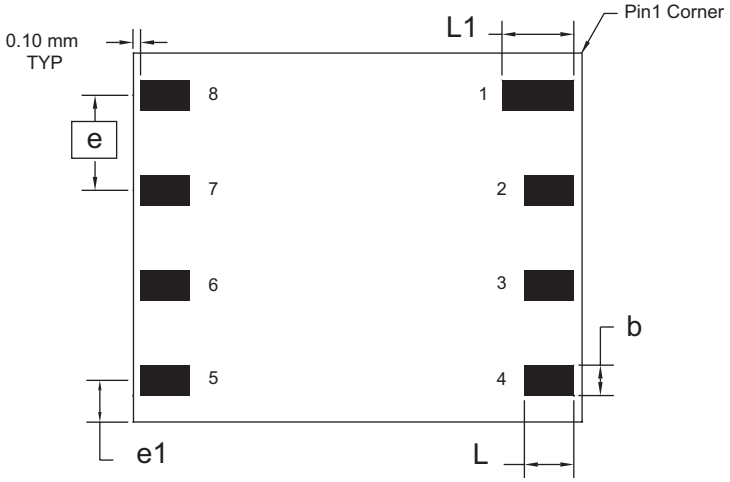
20.1 8CN4 – LAP



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

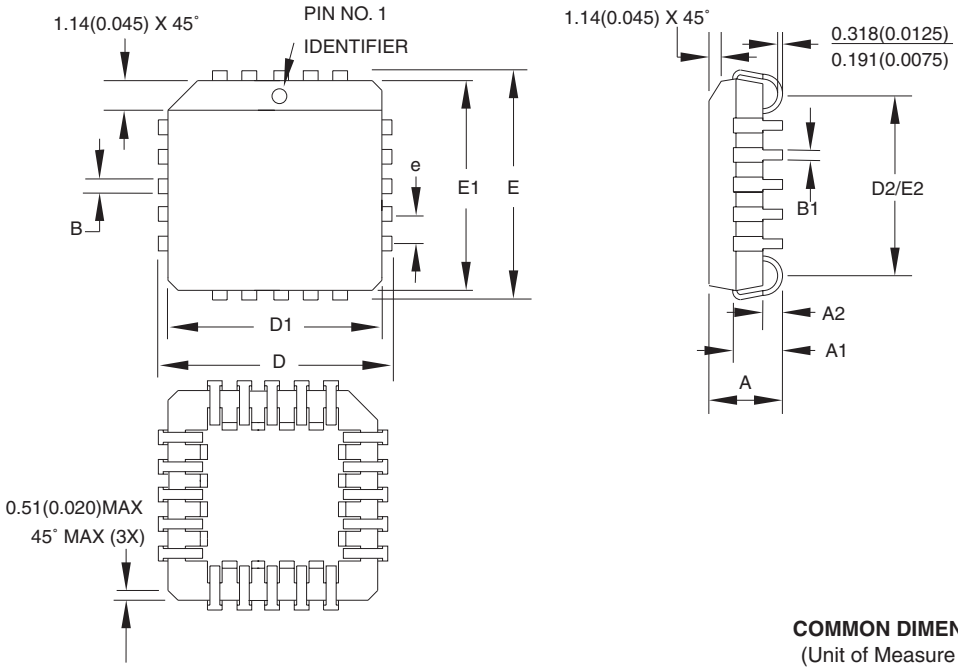
SYMBOL	MIN	NOM	MAX	NOTE
A	0.94	1.04	1.14	
A1	0.30	0.34	0.38	
b	0.45	0.50	0.55	1
D	5.89	5.99	6.09	
E	5.89	5.99	6.09	
e		1.27 BSC		
e1		1.10 REF		
L	0.95	1.00	1.05	1
L1	1.25	1.30	1.35	1

Note: 1. Metal Pad Dimensions.
2. All exposed metal area shall have the following finished platings.
Ni: 0.0005 to 0.015 mm
Au: 0.0005 to 0.001 mm

2/15/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8CN4**, 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27mm, Leadless Array Package (LAP)	DMH	8CN4	D

20.2 20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

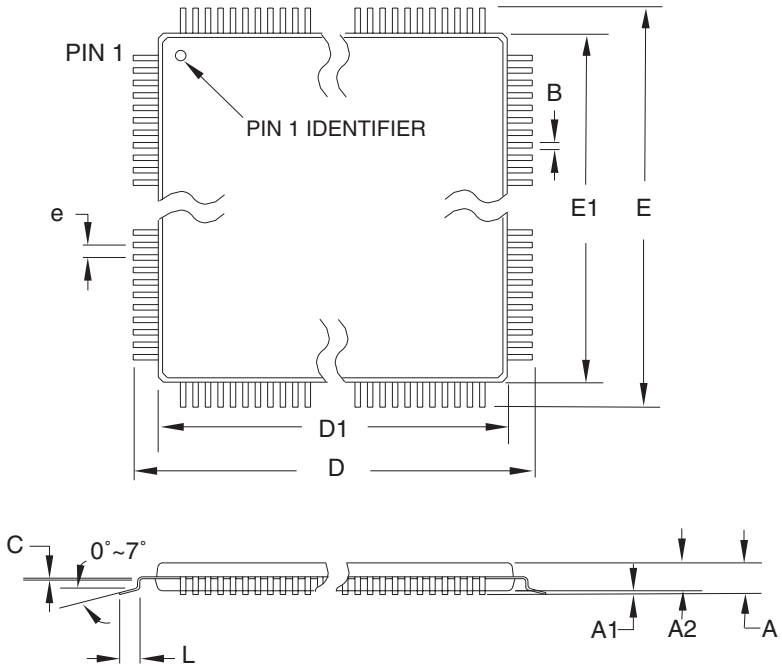
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

20.3 32A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32A,** 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	32A	B

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