Dual 8-Bit Buffered Multiplying CMOS D/A Converter

PM-7628

FEATURES

- On-Chip Latches for Both DACs
- +5V to +15V Single Supply Operation
- DACs Matched to 1%
- Four-Quadrant Multiplication
- TTL/CMOS Compatible from +5V To +15V
- 8-Bit Endpoint Linearity (±1/2 LSB)
- Full Temperature Operation
- Low Power Consumption
- Microprocessor Compatible (60ns Write Time)
- Improved ESD and Latch-Up Resistance
- Automatically Insertable CerDIP and Plastic Packages
- Available in Surface Mount SO, PLCC, and LCC Packages
- Improved AD7628
- Available in Die Form

APPLICATIONS

- Disk Drives
- Digital Gain/Attenuation Control
- Digitally-Controlled Filter Parameters
- Digitally-Controlled Audio Circuits
- X-Y Graphics
- Digital/Synchro Conversion
- Robotics
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION †

		PACKAGE: 20-Pin DIP	
RELATIVE ACCURACY	GAIN ERROR T_A = +25°C	MILITARY* TEMPERATURE −55°C TO +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C TO +85°C
±1/2LSB	±2LSB	PM7628AR	PM7628ER
±1/2LSB	±2LSB	PM7628ARC/883	PM7628FP
±1/2LSB	±2LSB	–	PM-7628FPC††
±1/2LSB	±2LSB	–	PM7628FS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The PM-7628 is an improved version of the AD7628 offering TTL compatibility from +5 to +15 volts and faster AC timing. It contains two 8-bit multiplying CMOS digital-to-analog converters that are fabricated in a single chip. This monolithic construction offers excellent DAC-to-DAC matching and tracking over temperature.

The PM-7628 consists of two thin-film R-2R resistor-ladder networks, two tracking span resistors, two data latches, one input buffer, and control logic circuitry.

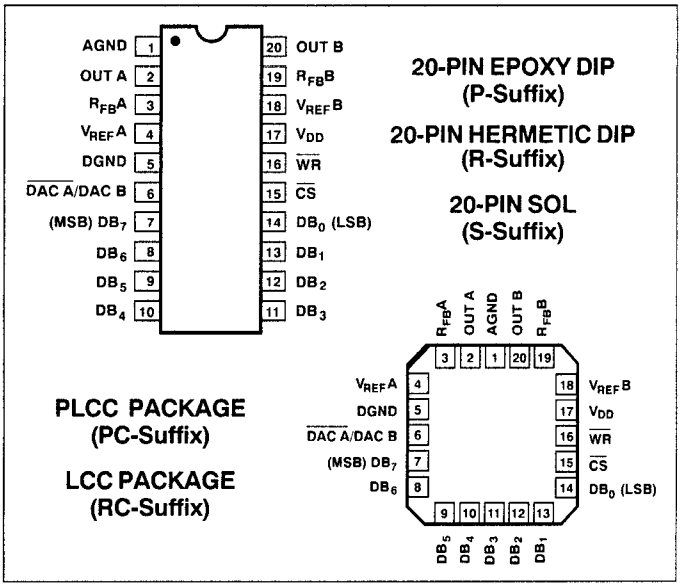
The PM-7628's digital inputs are bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. Data loading is similar to that of a RAM's write cycle. Digital input data is directed into one of the DAC data latches determined by the DAC selection control line DAC A/DAC B.

Operating from a single +5V to +15V power supply, the PM-7628 dissipates only 12mW of power in a space saving 20-pin 0.3" DIP, and 20-terminal surface mount packages. The PM-7628 features circuitry designed to protect against damage from electrostatic discharges.

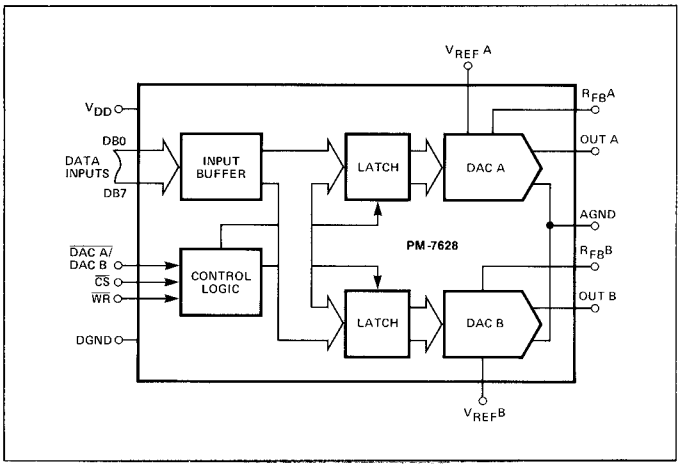
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7628AR PM7628ARC/883	AD7628TQ AD7628TE	MIL
PM7628ER	AD7628BQ	IND
PM7628FP PM7628FPC	AD7628KN AD7628KP	COM

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V to +17V
AGND to DGND ..... 0V, V_{DD} + 0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} + 0.3V
V_{PIN2}, V_{PIN20} to AGND ..... –0.3V, V_{DD}
$V_{REF}A$, $V_{REF}B$ to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V
Operating Temperature Range
AR, ARC Versions ..... –55°C to +125°C
ER, FP, FPC, FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
20-Pin Hermetic DIP (R)	80	15	°C/W
20-Pin Plastic DIP (P)	74	32	°C/W
20-Contact LCC (RC)	89	27	°C/W
20-Contact PLCC (PC)	76	36	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener-protected; however, permanent damag- may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready for use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper antistatic handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS: at V_{DD} = +5V ± 5%; $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$ = $I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2)	INL		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full-Scale Gain Error (Note 4)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	– –	±0.5 ±1.0	±2 ±3	LSB
Gain Temperature Coefficient (Δ Gain / Δ Temperature) (Notes 4, 10)	TCG_{FS}		–	–	±0.007	%/°C
Output Leakage Current $I_{OUT}A$ (Pin 2) $I_{OUT}B$ (Pin 20) (Note 5)	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	– –	±5 –	±50 ±200	nA
Input Resistance ($V_{REF}A$, $V_{REF}B$) (Note 6)	R_{IN}		8	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%

ELECTRICAL CHARACTERISTICS: at V_{DD} = +5V ± 5%; $V_{REF}A = V_{REF}B$ = +10V; $I_{OUT}A = I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}		2.4	–	–	V
Digital Input Low (Note 8)	V_{INL}		–	–	0.8	V
Input Current (Note 7)	I_{IN}	T_A = +25°C T_A = Full Temp. Range	– –	±.001 –	±1 ±10	µA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$ /DAC B	– –	– –	10 15	pF
SWITCHING CHARACTERISITCS (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}		100	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		100	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		100	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		90	–	–	ns
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Input = V_{INH} or V_{INL}	–	–	1	mA
		All Digital Input = 0V or V_{DD} T_A = +25°C T_A = Full Temp. Range	 – –	 – –	 0.5 1.0	mA

ELECTRICAL CHARACTERISTICS: at V_{DD} = +5V ± 5%; $V_{REF}A = V_{REF}B$ = +10V; $I_{OUT}A = I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
AC PERFORMANCE CHARACTERISTIC (Note 12)						
DC Supply Rejection Ratio (Δ Gain / ΔV_{DD}) (Note 13)	PSRR	T_A = +25°C T_A = Full Temp. Range	– –	– –	0.02 0.04	%/%
Current Settling Time (Notes 10, 15, 16, 20)	t_S	T_A = Full Temp. Range	–	–	300	ns
Digital Charge Injection (Note 17)	Q	T_A = +25°C	–	100	–	nVs
Output Capacitance	$C_{OUT}A$ $C_{OUT}B$	DAC Latches Loaded with 0000 0000	– –	– –	25 25	pF
	$C_{OUT}A$ $C_{OUT}B$	DAC Latches Loaded with 1111 1111	– –	– –	60 60	
AC Feedthrough (Note 18)	FT_A	$V_{REF}A$ to $I_{OUT}A$: T_A = +25°C T_A = Full Temp. Range	 – –	 – –	 –70 –65	dB
	FT_B	$V_{REF}B$ to $I_{OUT}B$: T_A = +25°C T_A = Full Temp. Range	 – –	 – –	 –70 –65	
Channel-to-Channel Isolation (Note 19)	CCI_{BA}	$V_{REF}A$ to $I_{OUT}B$: $V_{REF}A = 20V_{p-p}$ Sinewave @ f = 10kHz $V_{REF}B$ = 0V; T_A = +25°C	–	–80	–	dB
	CCI_{AB}	$V_{REF}B$ to $I_{OUT}A$; $V_{REF}B = 20V_{p-p}$ Sinewave @ f = 10kHz $V_{REF}A$ = 0V; T_A = +25°C	–	–80	–	
Digital Crosstalk	Q	For Code Transition from 0000 0000 to 1111 1111 T_A = +25°C	–	30	–	nVs
Harmonic Distortion	THD	V_{IN} = 6Vrms @ f = 1kHz T_A = +25°C	–	–85	–	dB

ELECTRICAL CHARACTERISTICS: at V_{DD} = +10.8V and +15.75V; $V_{REF}A = V_{REF}B$ = +10V; $I_{OUT}A = I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2)	INL		–	–	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Full Scale Gain Error (Note 4)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	– –	±0.5 ±1	±2 ±3	LSB
Gain Temperature Coefficient (Δ Gain / Δ Temperature) (Notes 4, 10)	TCG_{FS}		–	–	±0.0035	%/°C
Output Leakage Current $I_{OUT}A$ (Pin 2) $I_{OUT}B$ (Pin 20) (Note 5)	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	– –	±5 –	±50 ±200	nA
Input Resistance ($V_{REF}A$, $V_{REF}B$) (Note 6)	R_{IN}		8	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}		2.4	–	–	V
Digital Input Low (Note 8)	V_{INL}		–	–	0.8	V
Input Current (Note 7)	I_{IN}	T_A = +25°C T_A = Full Temp. Range	– –	±.001 –	±1 ±10	µA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$, DAC A /DAC B	– –	– –	10 15	pF

ELECTRICAL CHARACTERISTICS: at V_{DD} = +10.8V and +15.75V; $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$ = $I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
SWITCHING CHARACTERISITCS (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		70	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		60	–	–	ns
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Input = V_{INH} or V_{INL}				
		T_A = +25°C	–	–	2	mA
		T_A = Full Temp. Range	–	–	2.5	
		All Digital Input = 0V or +5V to V_{DD}				
		T_A = +25°C	–	–	0.5	mA
		T_A = Full Temp. Range	–	–	1.0	
AC PERFORMANCE CHARACTERISTIC (Note 12)						
DC Supply Rejection Ratio (Δ Gain / Δ V_{DD}) (Note 13)	PSRR	T_A = +25°C	–	–	0.01	%/%
		T_A = Full Temp. Range	–	–	0.02	
Current Settling Time (Notes 10, 15, 16, 20)	t_S	T_A = Full Temp. Range	–	–	200	ns
Digital Charge Injection (Note 17)	Q	T_A = +25°C	–	160	–	nVs
Output Capacitance	$C_{OUT}A$	DAC Latches Loaded	–	–	25	pF
	$C_{OUT}B$	with 0000 0000	–	–	25	
	$C_{OUT}A$	DAC Latches Loaded	–	–	60	
	$C_{OUT}B$	with 1111 1111	–	–	60	

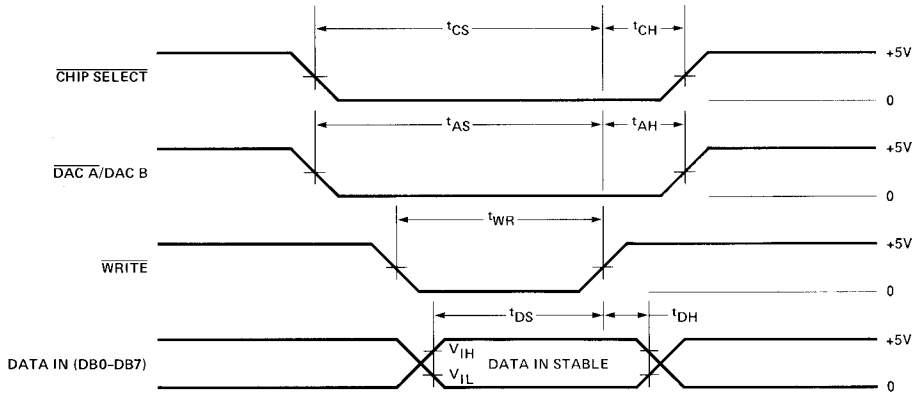
ELECTRICAL CHARACTERISTICS: at V_{DD} = +10.8V and +15.75V; $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$ = $I_{OUT}B$ = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7628 MIN	PM-7628 TYP	PM-7628 MAX	UNITS
AC Feedthrough (Note 18)	FT_A	$V_{REF}A$ to $I_{OUT}A$: T_A = +25°C T_A = Full Temp. Range	– –	– –	–70 –65	dB
	FT_B	$V_{REF}B$ to $I_{OUT}B$: T_A = +25°C T_A = Full Temp. Range	– –	– –	–70 –65	
Channel-to-Channel Isolation (Note 19)	CCI_{BA}	$V_{REF}A$ to $I_{OUT}B$: $V_{REF}A$ = $20V_{p-p}$ Sinewave @ f = 10kHz $V_{REF}B$ = 0V; T_A = +25°C	–	–80	–	dB
	CCI_{AB}	$V_{REF}B$ to $I_{OUT}A$; $V_{REF}B$ = $20V_{p-p}$ Sinewave @ f = 10kHz $V_{REF}A$ = 0V; T_A = +25°C	–	–80	–	
Digital Crosstalk	Q	For Code Transition from 0000 0000 to 1111 1111 T_A = +25°C	–	50	–	nVs
Harmonic Distortion	THD	V_{IN} = 6Vrms @ f = 1kHz T_A = +25°C	–	–85	–	dB

NOTES:

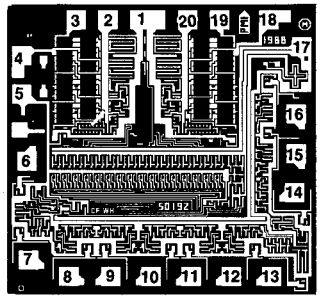
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All grades guaranteed to be monotonic over the full operating temperature range.
4. Measured using internal $R_{FB}A$ and $R_{FB}B$. Both DAC latches loaded with 1111 1111.
5. DAC loaded with 0000 0000.
6. Input resistance TC = 300 ppm/°C.
7. V_{IN} = 0V or V_{DD}.
8. For all data bits DB0-DB7, $\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$ /DAC B.
9. Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
10. Guaranteed and not tested.
11. See timing diagram.
12. These characteristics are for design guidance only and are not subject to test.
13. ΔV_{DD} = ±5%.
14. From digital input to 90% of final analog-output current.
15. $V_{REF}A$ = $V_{REF}B$ = +10V; $I_{OUT}A$, $I_{OUT}B$ load = **100Ω**, C_{EXT} = 13pF.
16. $\overline{WR}$, $\overline{CS}$ = 0V, DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
17. For code transition 0000 0000 to 1111 1111.
18. $V_{REF}A$, $V_{REF}B$ = $20V_{p-p}$ Sinewave @ f = 10kHz.
19. Both DAC latches loaded with 1111 1111.
20. Extrapolated: t_S (1/2 LSB) = t_{PD} + 6.2τ, where τ = the measured first time constant of the final RC decay.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% ARE t_r = t_f = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

DICE CHARACTERISTICS



DIE SIZE 0.082 x 0.078 inch, 6,396 sq. mils (2.08 x 1.98 mm, 4.126 sq. mm)

1. ANALOG GROUND (AGND)
2. OUTPUT A (OUT A)
3. DAC A FEEDBACK RESISTOR ($R_{FB}A$)
4. DAC A REFEREMCE INPUT ($V_{REF}A$)
5. DIGITAL GROUND (DGND)
6. DIGITAL SELECTION ($\overline{DAC\ A}$/DAC B)
7. DIGITAL INPUT DB_7 (MSB)
8. DIGITAL INPUT DB_6
9. DIGITAL INPUT DB_5
10. DIGITAL INPUT DB_4
11. DIGITAL INPUT DB_3
12. DIGITAL INPUT DB_2
13. DIGITAL INPUT DB_1
14. DIGITAL INPUT DB_0 (LSB)
15. CHIP SELECT ($\overline{CS}$)
16. WRITE ($\overline{WR}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT ($V_{REF}B$)
19. DAC B FEEDBACK RESISTOR ($R_{FB}B$)
20. OUTPUT B (OUT B)

Substrate (die Backside) is internally connected to V_{DD}.

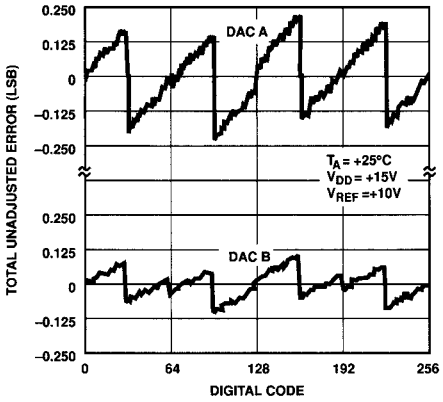
WAFER TEST LIMITS at V_{DD} = +5V, +10.8V or +15.75V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7628G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111	±2	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 0000 0000 Pad 2 and 20	±50	nA MAX
Input Resistance	R_{IN}	Pad 4 and 18	8/15	kΩ MIN/ kΩ MAX
$V_{REF}A/V_{REF}B$ Input Resistance Match	$\Delta V_{REF}A$, B		±1	% MAX
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	µA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or +5V to V_{DD}	2 0.5	mA MAX
DC Supply Rejection (Δ Gain / ΔV_{DD})	PSRR	V_{DD} = ±5%	0.01	%/% MAX

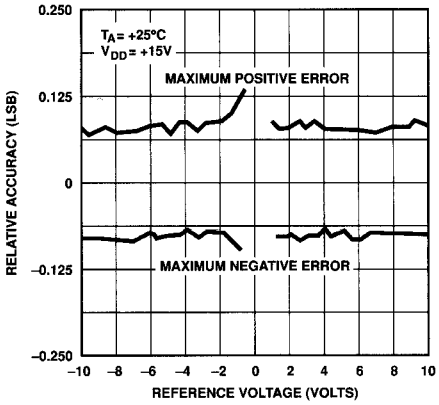
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

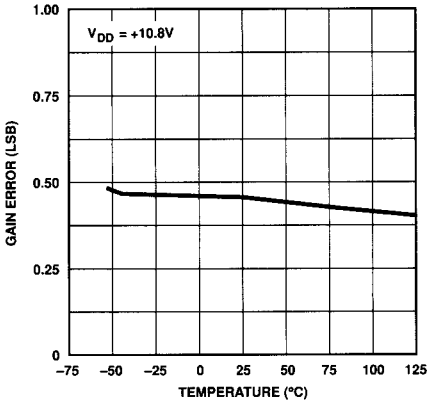
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT



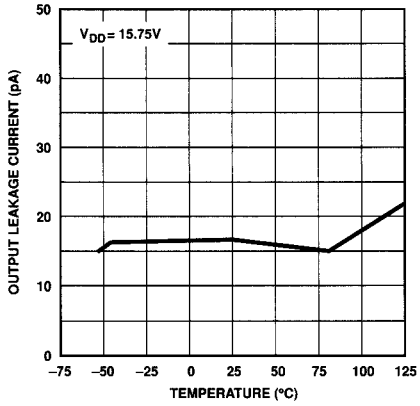
RELATIVE ACCURACY vs REFERENCE VOLTAGE



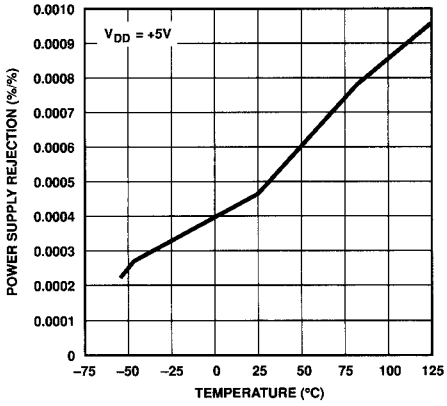
FULL-SCALE GAIN ERROR vs TEMPERATURE



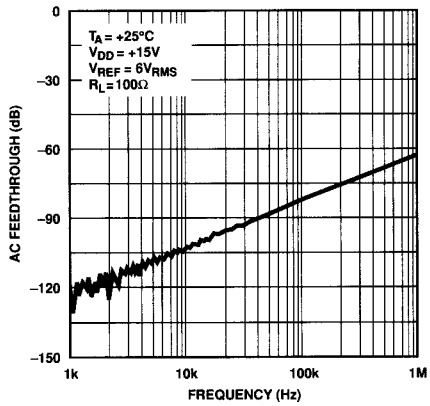
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



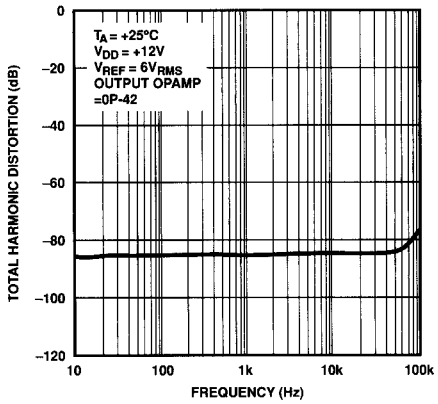
POWER SUPPLY REJECTION vs TEMPERATURE



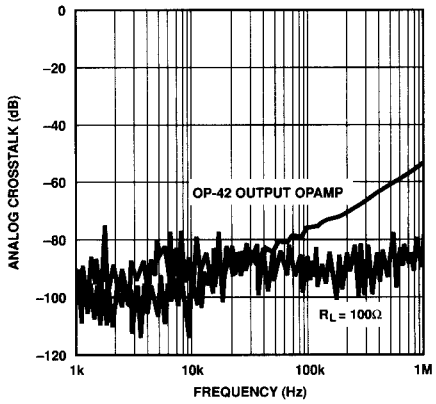
AC FEEDTHROUGH vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

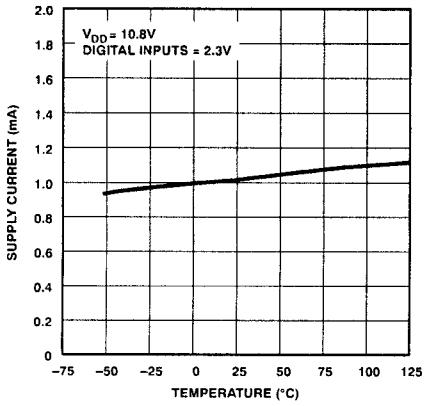


ANALOG CROSSTALK vs FREQUENCY

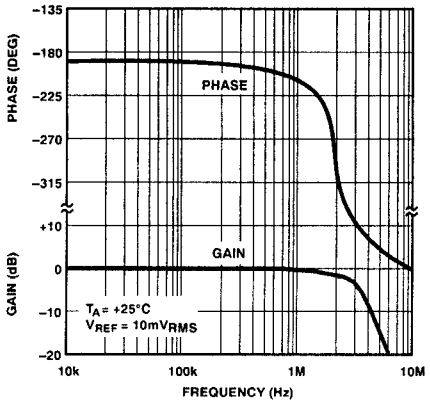


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

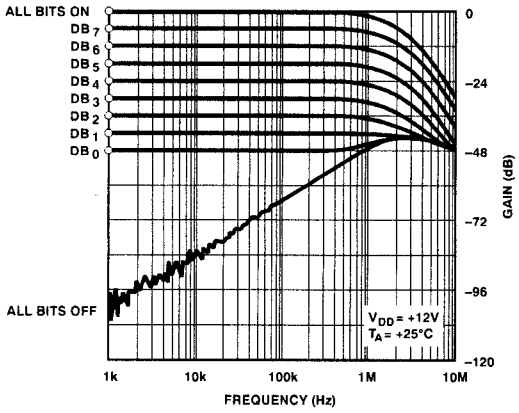
SUPPLY CURRENT (I_{DD}) vs TEMPERATURE



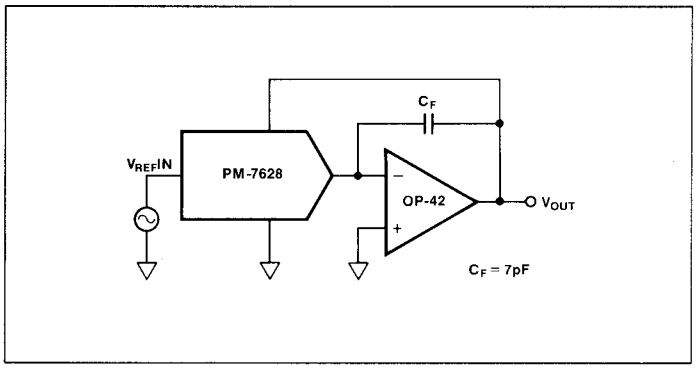
GAIN AND PHASE SHIFT vs FREQUENCY WITH OP-42 OUTPUT AMPLIPHIER



GAIN (V_{OUT}/V_{REF}) vs FREQUENCY

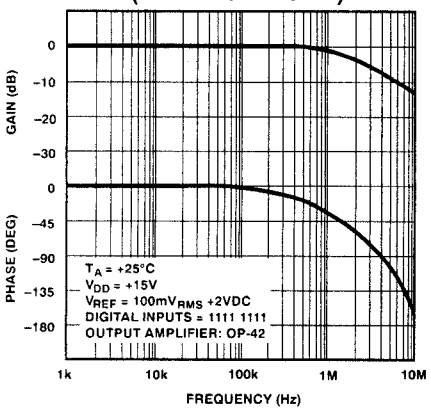


TEST CIRCUIT FOR GAIN vs FREQUENCY

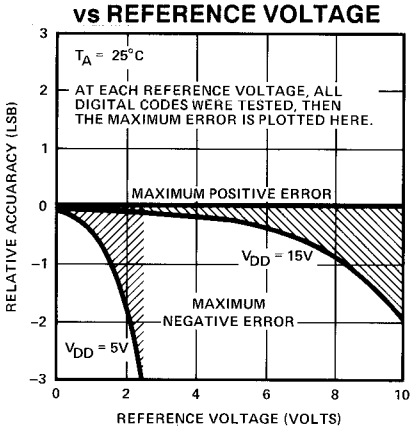


VOLTAGE SWITCHING MODE CHARACTERISTICS

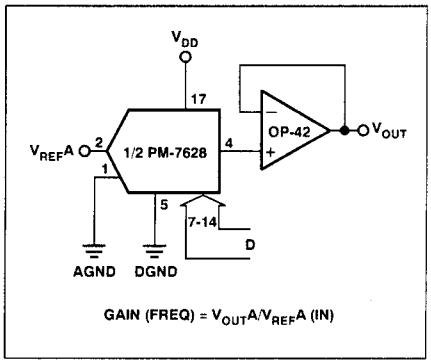
GAIN AND PHASE vs FREQUENCY (VOLTAGE MODE)



RELATIVE ACCURACY vs REFERENCE VOLTAGE



VOLTAGE SWITCHING MODE TEST CIRCUIT



PARAMETER DEFINITIONS

RELATIVE ACCURACY OR INTEGRAL NONLINEARITY (INL)

This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed as a percent of full-scale range or in terms of LSBs.

Refer to PMI 1988 Data Book, Section 11, for additional digital-to-analog converter definitions.

INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

MODE SELECTION

The inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data on the data bit line DB0-DB7.

HOLD MODE

The selected DAC latch retains the data which was present on the data lines just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

CIRCUIT INFORMATION

D/A SECTION

There is a normally closed switch in series with the internal feedback resistor (R_{FB}) as shown in Figure 1. This switch improves linearity performance over temperature and power supply rejection; however, when the circuit is not powered up, the switch assumes an open state.

See the PM-7528 data sheet for additional circuit information and applications.

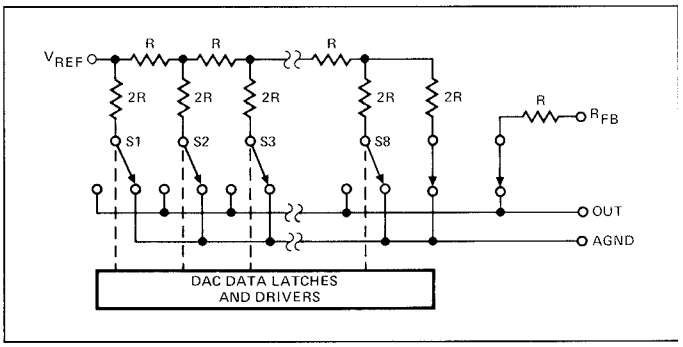


FIGURE 1: *Simplified Functional Circuit for DAC A or DAC B*

DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed such that TTL input levels are converted into internal CMOS logic levels; they are used to drive the internal circuitry. A simple 5V regulator is used to ensure TTL compatibility at V_{DD} = 12V to 15V (see Figure 2).

The PM-7628's digital inputs are TTL compatible between the V_{DD} range of +5V to +16.5V. The digital inputs affect the amount of quiescent supply current as shown in Figure 3. Peak supply current occurs as the digital input (V_{IN}) passes through the transition region. Maintaining the digital input voltages as close as possible to the supplies (V_{DD} and DGND) minimizes supply current consumption.

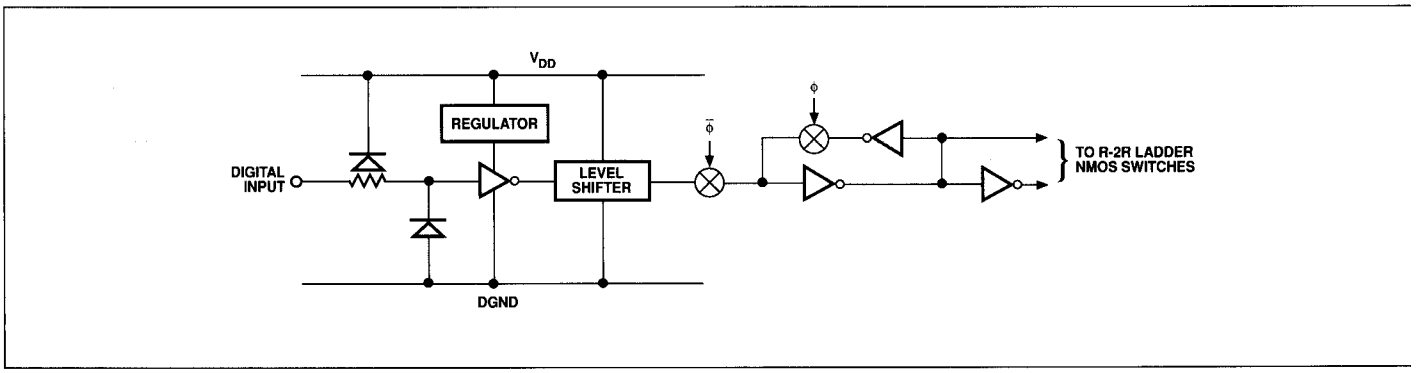


FIGURE 2: *Simplified Schematic of Digital Inputs*

There are several fast logic families that are used to buffer the DAC's digital inputs. These buffers, if not properly terminated, will cause reflections that can exhibit 1.5 to 3V of negative overshoot. This overshoot, when applied to the digital inputs, will cause an internal diode to become forward biased as shown in Figure 4. If sufficient current is generated, most CMOS devices will latchup resulting in a catastrophic failure. The PM-7628 features circuitry designed to reduce the susceptibility of electrostatic discharges and latchup (see Figure 5). As shown, a series resistor has been incorporated into each digital input so that the input appears resistive to a negative voltage and prevents latchup (see Figure 6).

The PM-7628's rugged construction also resists latchup during power supply sequencing; the digital inputs can be powered up before V_{DD} without the device latching up.

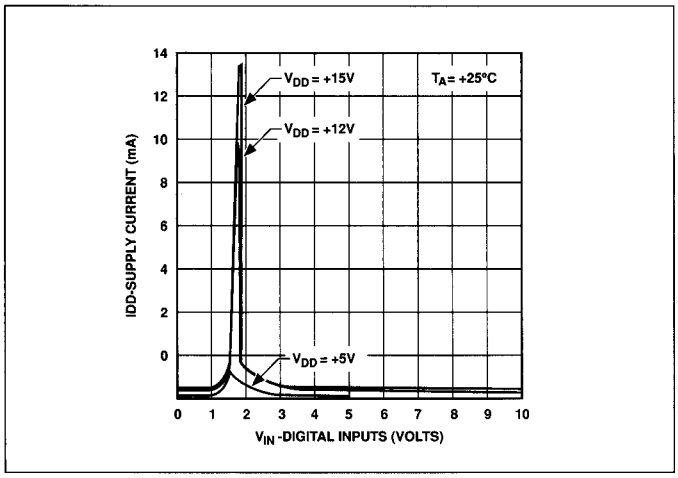


FIGURE 3: *Digital Inputs vs. I_{DD}*

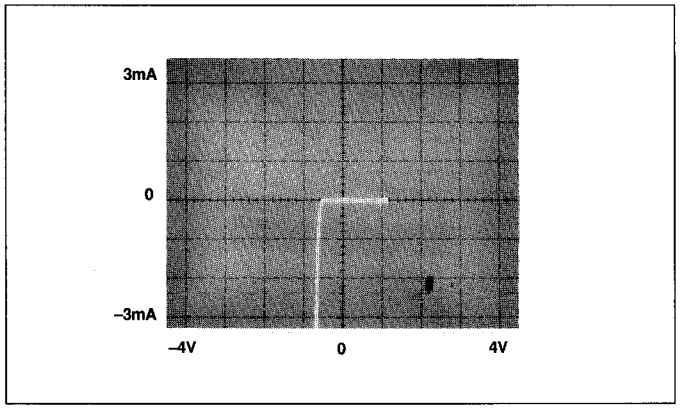


FIGURE 4: *Digital Input Characteristic*

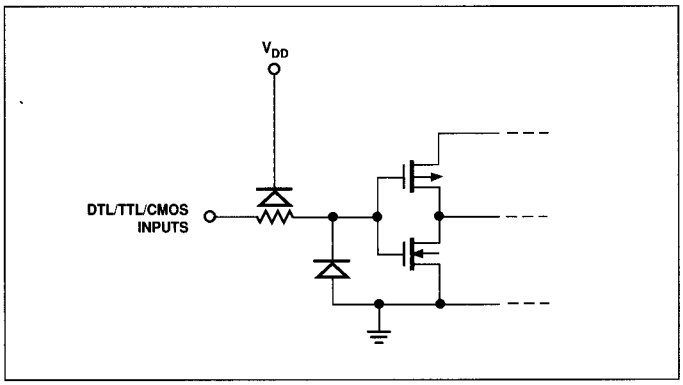


FIGURE 5: *Digital Input Protection*

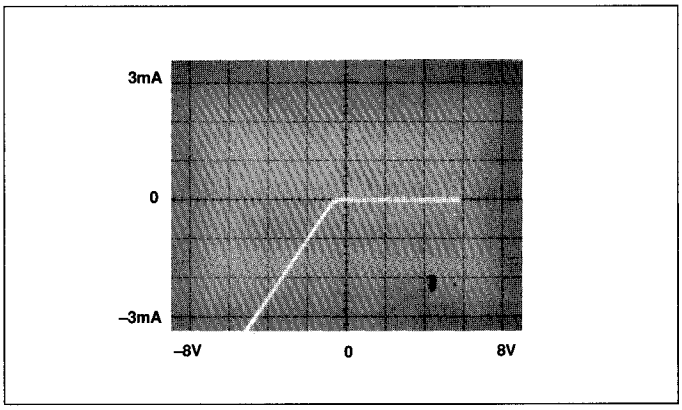
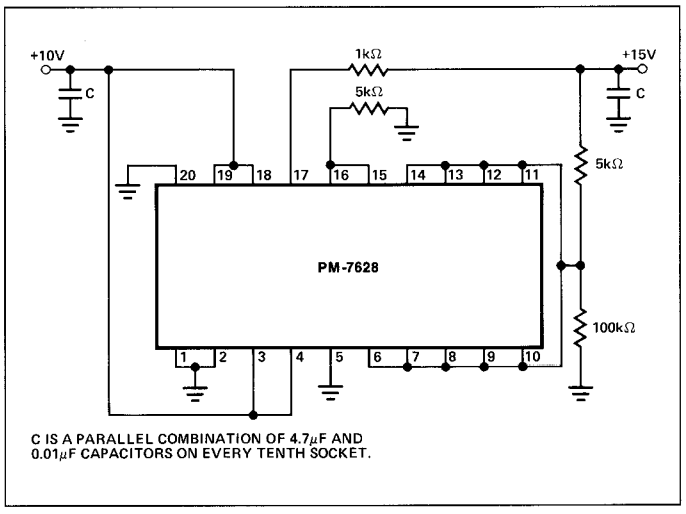


FIGURE 6: *PM-7628 Digital Input Characteristic*

BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The most common application of the PM-7628 is in the voltage output mode. Unipolar output operation provides a 0 to 10 volt output swing when connected, as shown in Figure 7. The maximum output voltage polarity is the inverse of the input reference voltage, since the op amp inverts the input currents. The transfer equation for unipolar operation is $V_{OUT} = -V_{IN} \times D/256$, where D is the decimal value of the data bit inputs DB_0 thru DB_7 and V_{IN} is the reference input voltage. The transfer equation highlights another popular application of CMOS DAC's, multiplication. The output voltage is the product of the reference voltage and the digital input code. The reference input voltage can be any value in the range of ±25 volts for both DC or AC signals. The circuit in Figure 7 performs two-quadrant multiplication. Table 1 provides example analog outputs for the given digital input codes.

For bipolar output operation, connect the PM-7628 as shown in Figure 8. This circuit configuration provides an offset current, derived from the reference, to enable the output op amp to swing in both polarities. The digital input coding becomes offset binary. Table 2 provides some example analog outputs for various digital inputs (D). The transfer equation for bipolar operation is $V_{OUT} = V_{IN} \times (D/128 - 1)$, where D is the decimal value of the data bit inputs DB_0 thru DB_7. This circuit provides full four-quadrant multiplication, able to accept ± polarities on both inputs as well as the circuit output.

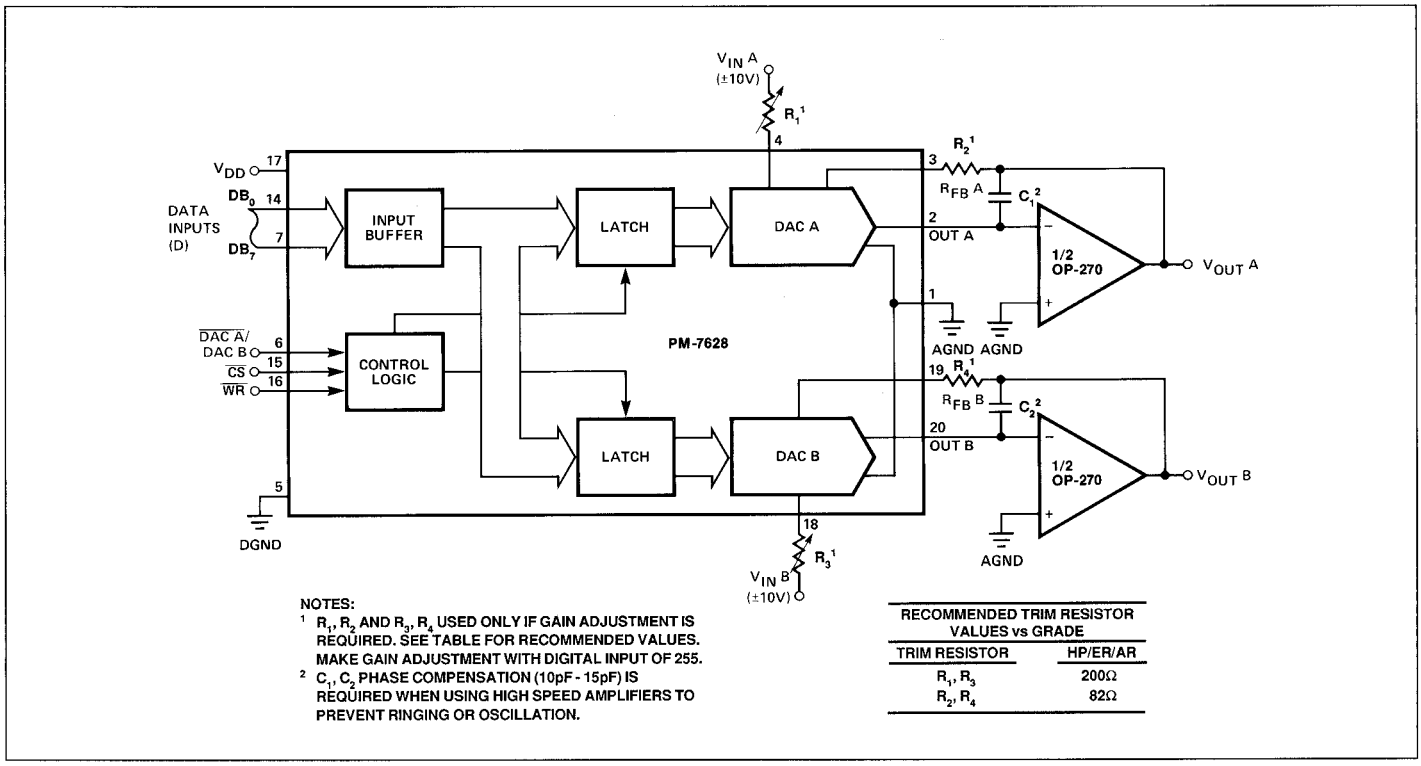


FIGURE 7: *Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.*

TABLE 1: Unipolar Binary Code Table. See Figure 7.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
1111 1111	$-V_{IN}\left(\frac{255}{256}\right)$
1000 0001	$-V_{IN}\left(\frac{129}{256}\right)$
1000 0000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
0111 1111	$-V_{IN}\left(\frac{127}{256}\right)$
0000 0001	$-V_{IN}\left(\frac{1}{256}\right)$
0000 0000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

NOTE: 1 LSB = (2^{-8}) $(V_{IN}) = \frac{1}{256}(V_{IN})$

TABLE 2: Bipolar (Offset Binary) Code Table. See Figure 8.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
1111 1111	$+V_{IN}\left(\frac{127}{128}\right)$
1000 0001	$+V_{IN}\left(\frac{1}{128}\right)$
1000 0000	0
0111 1111	$-V_{IN}\left(\frac{1}{128}\right)$
0000 0001	$-V_{IN}\left(\frac{127}{128}\right)$
0000 0000	$-V_{IN}\left(\frac{128}{128}\right)$

NOTE: 1 LSB = (2^{-7}) $(V_{IN}) = \frac{1}{128}(V_{IN})$

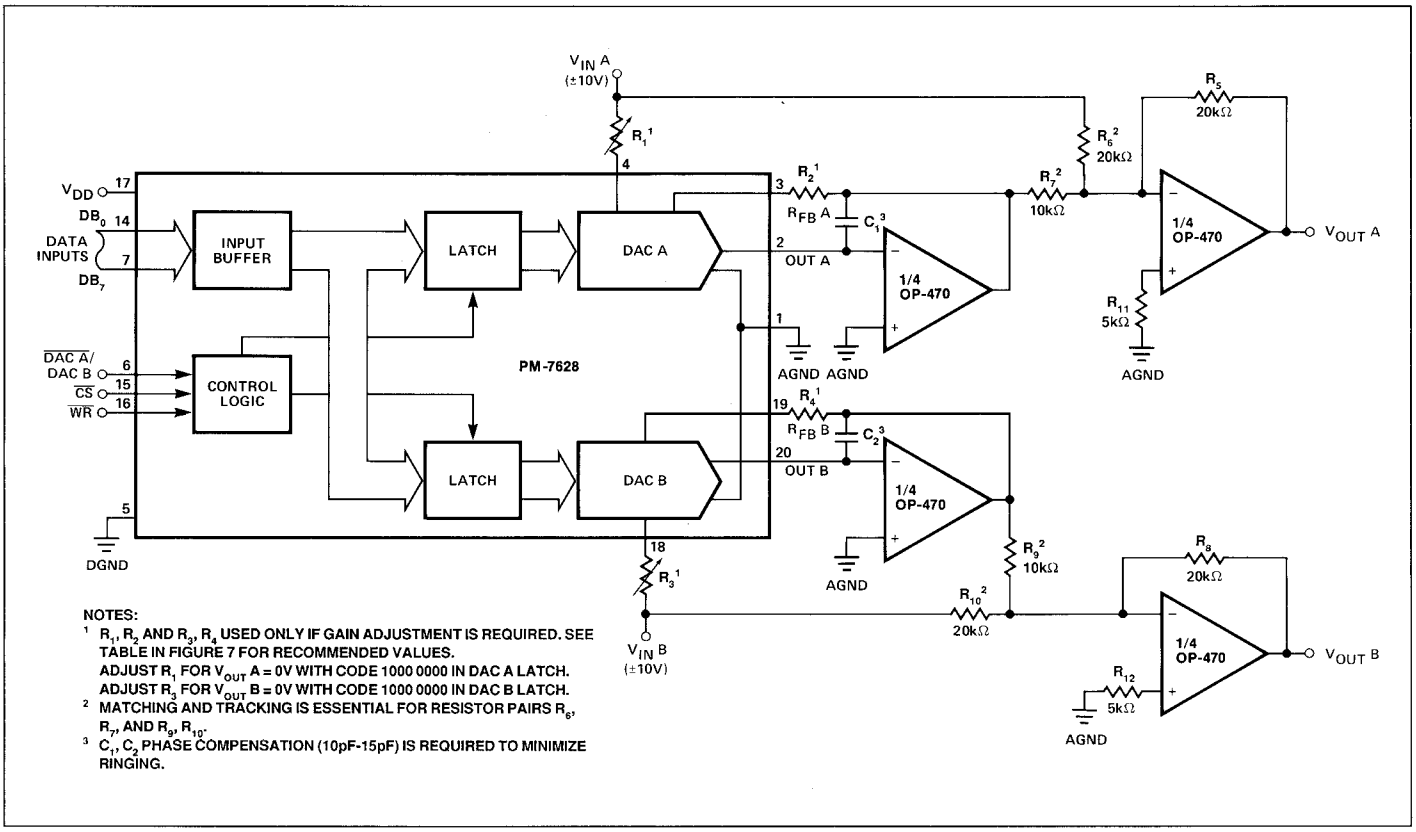


FIGURE 8: *Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.*

APPLICATION HINTS

To ensure system performance consistent with PM-7628 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the PM-7628 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal, is to tie AGND and DGND together at the PM-7628. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that Schottky diodes (HP5082-2835 or equivalent) be connected in inverse parallel between the PM-7628 AGND and DGND pins.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output with a maximum magnitude of 0.67 V_{OS} (V_{OS} is amplifier input-offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
3. HIGH-FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open-loop response; this can cause ringing or oscillation. Stability can be restored by adding a small phase-compensation capacitor in parallel with the feedback resistor.
4. DYNAMIC PERFORMANCE: The dynamic performance of the two DACs in the PM-7628 will depend upon the gain and phase characteristics of the output amplifiers, together with the optimum choice of the PC board layout and decoupling components.
5. CIRCUIT LAYOUT SUGGESTIONS: Analog and digital ground traces should be routed between package pins to isolate the digital inputs from the analog circuitry. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, 4-5 to minimize reference feedthrough to the output in multiplying applications. A power supply bypass capacitor (0.1μF in parallel with a 1μF or 10μF) is recommended across V_{DD} to DGND.

SINGLE SUPPLY OPERATION, VOLTAGE SWITCHING

With the PM-7628 connected in the voltage switching mode of operation (Figure 9) only one power supply is necessary. There is no voltage inversion between the reference input polarity and the output in the voltage switching mode.

Two characteristic curves in the typical performance characteristics section were generated using this voltage switching mode of operation. The first graph, relative accuracy versus input reference voltage, shows that to maintain a ±1/2 LSB maximum linearity error, V_{REF} should be less than 1.5 volts for V_{DD} = 5 volts or less than 6 volts for V_{DD} = 15 volts. The gain-phase response graph shows dominant pole response for single supply applications where the reference input is an AC signal. In this application the reference input should remain between 1.5 volts and ground when V_{DD} = 5 volts. Additionally, settling time measures 400 to 500 nanoseconds for a digital input change of 255 to 0 when V_{DD} = 5V.

The output terminal in the voltage switching mode has a constant output resistance (≈11kΩ) independent of the digital input code. The output should be buffered with a voltage follower when driving low impedance loads.

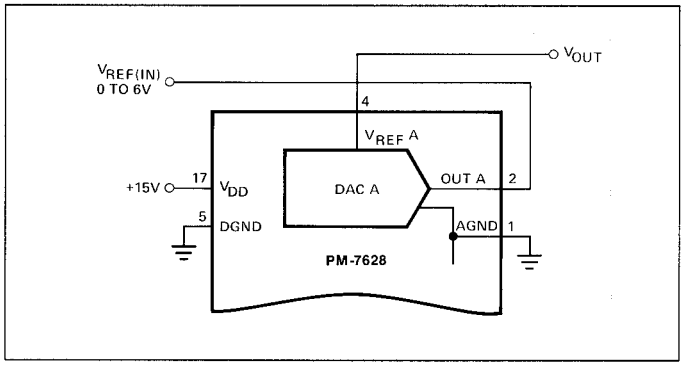


FIGURE 9: *PM-7628 in Single Supply, Voltage-Switching Mode*

SINGLE SUPPLY, CURRENT SWITCHING

An alternate single-supply operating mode for the PM-7628 results when offsetting the analog ground. Figure 10 shows the circuit. The advantage of this configuration is the ability to set the output voltage level in the center of the supply voltage. This allows use of lower cost op amps that would not work in single-supply voltage-switching applications.

The transfer equation in this mode of operation is:

$$V_{OUT}(D) = D/256\ (AGND - V_{REF}) + AGND;$$

where D is the whole number binary input.

A popular connection in the current-steering single-supply mode consists of a 2.5 volt reference connected to AGND, the V_{REF} input grounded, V_{DD} connected to +12 volts, and the external (V+) op amp tied to +12 volts. This hookup results in the following transfer equation:

$$V_{OUT}(D) = 2.5\ (1 + D/256);$$

where $V_{OUT}(255) = 2.5\ (1 + 255/256) = 5V$
$V_{OUT}(0) = 2.5V.$

To maintain best linearity keep AGND equal to or less than 7 volts when V_{DD} is +12 volts.

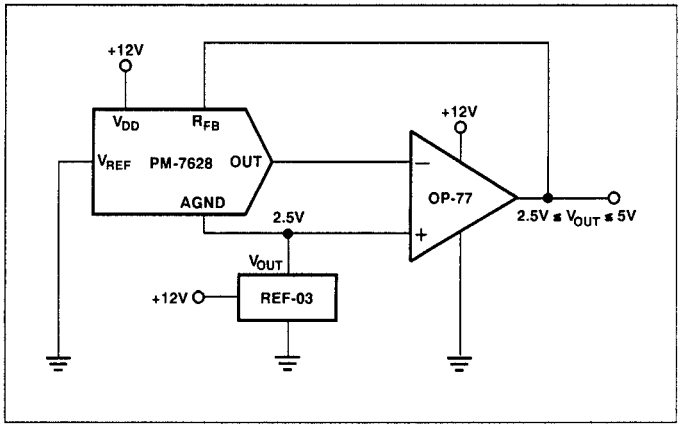


FIGURE 10: *PM-7628 in Single Supply, Current-Steering Mode*